TPS3701 36-V Window Comparator With Internal Reference for Over- and Undervoltage Detection

1 Features

- Wide Supply Voltage Range: 1.8 V to 36 V
- Adjustable Threshold: Down to 400 mV
- Open-Drain Outputs for Over- and Undervoltage Detection
- Low Quiescent Current: 7 µA (Typical)
- High Threshold Accuracy:
  - 0.75% Over Temperature
  - 0.25% (Typical)
- Internal Hysteresis: 5.5 mV (Typical)
- Temperature Range: –40°C to 125°C
- Package:
  - SOT-6

2 Applications

- Industrial Control Systems
- Embedded Computing Modules
- DSPs, Microcontrollers, and Microprocessors
- Notebook and Desktop Computers
- Portable- and Battery-Powered Products
- FPGA and ASIC Systems

3 Description

The TPS3701 wide-supply voltage window comparator operates over a 1.8-V to 36-V range. The device has two precision comparators with an internal 400-mV reference and two open-drain outputs (OUTA and OUTB) rated to 25 V for over- and undervoltage detection. Use the TPS3701 as a window comparator or as two independent voltage monitors; set the monitored voltage with the use of external resistors.

OUTA is driven low when the voltage at the INA pin drops below the negative threshold, and goes high when the voltage returns above the positive threshold. OUTB is driven low when the voltage at the INB pin rises above the positive threshold, and goes high when the voltage drops below the negative threshold. Both comparators in the TPS3701 include built-in hysteresis for noise rejection, thereby ensuring stable output operation without false triggering.

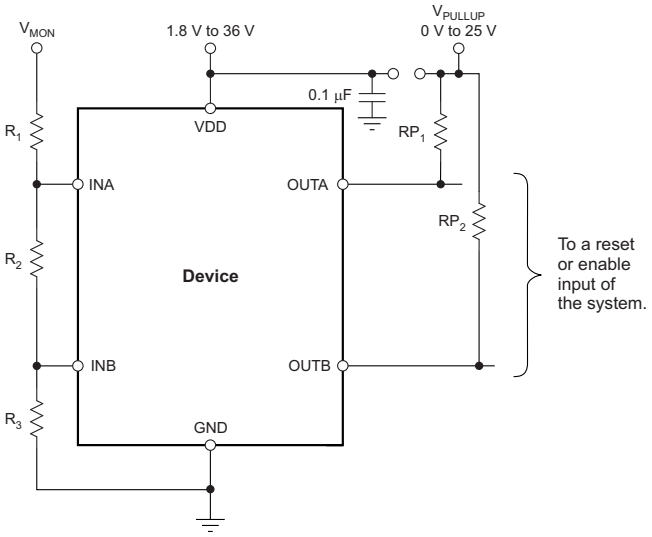
The TPS3701 is available in a SOT-6 package and is specified over the junction temperature range of –40°C to 125°C.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPS3701	SOT (6)	2.90 mm × 1.60 mm

(1) For all available packages, see the package option addendum at the end of the data sheet.

Typical Application



Typical Error vs Junction Temperature

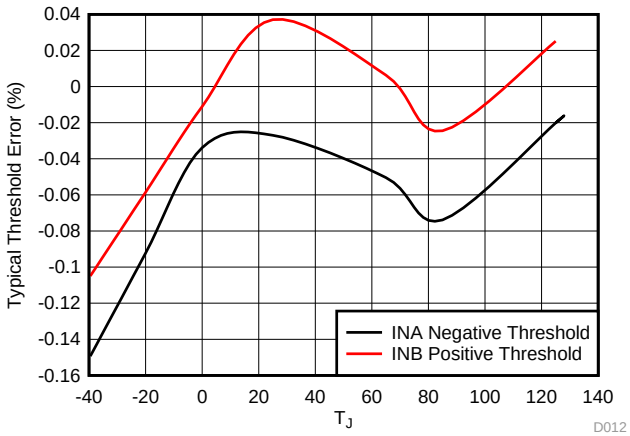


Table of Contents

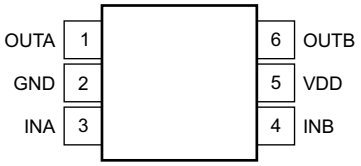
4 Revision History

Changes from Original (November 2014) to Revision A **Page**

- Changed input pin voltage maximum from: 1.7 V to: 6.5 V ... 4
- Added a tablenote for the input pin voltage maximum ... 4
- Changed Figure 19 ... 12

5 Pin Configuration and Functions

DDC Package
6-Pin SOT
(Top View)



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
GND	2	—	Ground
INA	3	I	Comparator A input. This pin is connected to the voltage to be monitored with the use of an external resistor divider. When the voltage at this terminal drops below the threshold voltage $V_{IT–(INA)}$, OUTA is driven low.
INB	4	I	Comparator B input. This pin is connected to the voltage to be monitored with the use of an external resistor divider. When the voltage at this terminal exceeds the threshold voltage $V_{IT+(INB)}$, OUTB is driven low.
OUTA	1	O	INA comparator open-drain output. OUTA is driven low when the voltage at this comparator is less than $V_{IT–(INA)}$. The output goes high when the sense voltage rises above $V_{IT+(INA)}$.
OUTB	6	O	INB comparator open-drain output. OUTB is driven low when the voltage at this comparator exceeds $V_{IT+(INB)}$. The output goes high when the sense voltage falls below $V_{IT–(INB)}$.
VDD	5	I	Supply voltage input. Connect a 1.8-V to 36-V supply to VDD to power the device. It is good analog design practice to place a 0.1-µF ceramic capacitor close to this pin.

6 Specifications

6.1 Absolute Maximum Ratings

Over operating junction temperature range, unless otherwise noted.(1)

		MIN	MAX	UNIT
Voltage(2)	V_{DD}	–0.3	+40	V
	V_{OUTA}, V_{OUTB}	–0.3	+28	
	V_{INA}, V_{INB}	–0.3	+7	
Current	Output pin current		40	mA
Temperature	Operating junction, T_J	–40	+125	°C
	Storage temperature, T_{stg}	–65	+150	

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages are with respect to network ground terminal.

6.2 ESD Ratings

		VALUE	UNIT
$V_{(ESD)}$ Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
	Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating junction temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{DD}	Supply pin voltage	1.8		36	V
V_{INA}, V_{INB}	Input pin voltage	0		6.5(1)	V
V_{OUTA}, V_{OUTB}	Output pin voltage	0		25	V
I_{OUTA}, I_{OUTB}	Output pin current	0		10	mA
T_J	Junction temperature	–40	+25	+125	°C

(1) Operating V_{INA} or V_{INB} at 2.4 V or higher and at 125°C continuously for 10 years or more would cause a degradation of accuracy spec to 1.5% maximum

6.4 Thermal Information

THERMAL METRIC(1)		TPS3701 DDC (SOT) 6 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	201.6	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	47.8	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	51.2	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.7	°C/W
ψ_{JB}	Junction-to-board characterization parameter	50.8	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report (SPRA953).

6.5 Electrical Characteristics

Over the operating temperature range of T_J = –40°C to +125°C, 1.8 V ≤ V_{DD} < 36 V, and pullup resistors $RP_{1,2}$ = 100 kΩ, unless otherwise noted. Typical values are at T_J = 25°C and V_{DD} = 12 V.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{DD}	Supply voltage range		1.8		36	V
$V_{(POR)}$	Power-on reset voltage(1)	V_{OL} ≤ 0.2 V			0.8	V
$V_{IT–(INA)}$	INA pin negative input threshold voltage	V_{DD} = 1.8 V to 36 V	397	400	403	mV
$V_{IT+(INA)}$	INA pin positive input threshold voltage	V_{DD} = 1.8 V to 36 V	400	405.5	413	mV
$V_{HYS(INA)}$	INA pin hysteresis voltage ($HYS = V_{IT+(INA)} – V_{IT–(INA)}$)		2	5.5	12	mV
$V_{IT–(INB)}$	INB pin negative input threshold voltage	V_{DD} = 1.8 V to 36 V	387	394.5	400	mV
$V_{IT+(INB)}$	INB pin positive input threshold voltage	V_{DD} = 1.8 V to 36 V	397	400	403	mV
$V_{HYS(INB)}$	INB pin hysteresis voltage ($HYS = V_{IT+(INB)} – V_{IT–(INB)}$)		2	5.2	12	mV
V_{OL}	Low-level output voltage	V_{DD} = 1.8 V, I_{OUT} = 3 mA		130	250	mV
		V_{DD} = 5 V, I_{OUT} = 5 mA		150	250	mV
I_{IN}	Input current (at INA, INB pins)	V_{DD} = 1.8 V and 36 V, V_{INA}, V_{INB} = 6.5 V	–25	+1	+25	nA
		V_{DD} = 1.8 V and 36 V, V_{INA}, V_{INB} = 0.1 V	–15	+1	+15	nA
$I_{D(leak)}$	Open-drain output leakage current	V_{DD} = 1.8 V and 36 V, V_{OUT} = 25 V		10	300	nA
I_{DD}	Supply current	V_{DD} = 1.8 V – 36 V		8	11	µA
UVLO	Undervoltage lockout(2)	V_{DD} falling	1.3	1.5	1.7	V

(1) The lowest supply voltage (V_{DD}) at which output is active; $t_{r(VDD)}$ > 15 µs/V. If less than $V_{(POR)}$, the output is undetermined.
(2) When V_{DD} falls below UVLO, OUTA is driven low and OUTB goes to high impedance. The outputs cannot be determined if less than $V_{(POR)}$.

6.6 Timing Requirements

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
$t_{pd(HL)}$	High-to-low propagation delay(1)	V_{DD} = 24 V, ±10-mV input overdrive, R_L = 100 kΩ, V_{OH} = 0.9 × V_{DD}, V_{OL} = 250 mV		9.9		µs
$t_{pd(LH)}$	Low-to-high propagation delay(1)	V_{DD} = 24 V, ±10-mV input overdrive, R_L = 100 kΩ, V_{OH} = 0.9 × V_{DD}, V_{OL} = 250 mV		28.1		µs
$t_{d(start)}$(2)	Startup delay	V_{DD} = 5 V		155		µs
t_r	Output rise time	V_{DD} = 12 V, 10-mV input overdrive, R_L = 100 kΩ, C_L = 10 pF, V_O = (0.1 to 0.9) × V_{DD}		2.7		µs
t_f	Output fall time	V_{DD} = 12 V, 10-mV input overdrive, R_L = 100 kΩ, C_L = 10 pF, V_O = (0.9 to 0.1) × V_{DD}		0.12		µs

(1) High-to-low and low-to-high refers to the transition at the input pins (INA and INB).
(2) During power on, V_{DD} must exceed 1.8 V for at least 150 µs (typical) before the output state reflects the input condition.

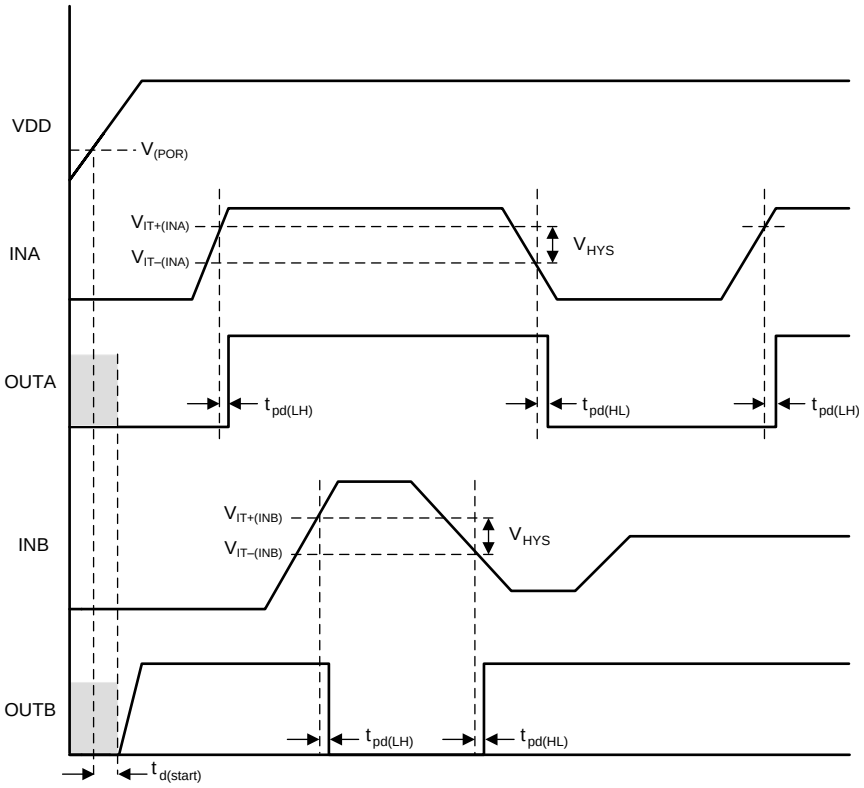


Figure 1. Timing Diagram

6.7 Typical Characteristics

At T_J = 25°C and V_{DD} = 12 V, unless otherwise noted.

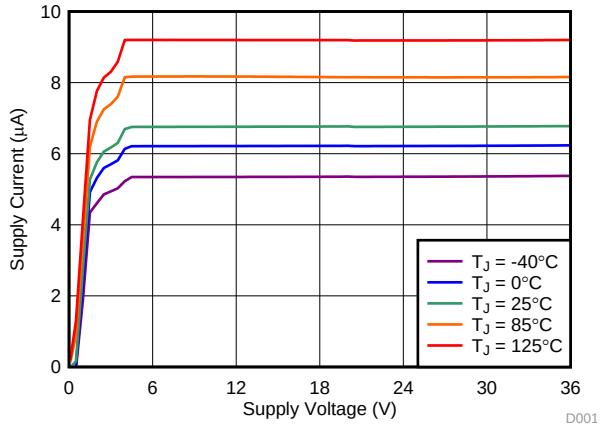
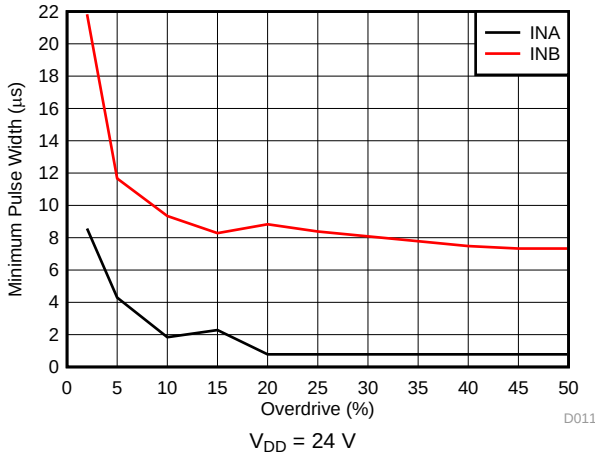


Figure 2. Supply Current vs Supply Voltage



V_{DD} = 24 V

Figure 3. Minimum Pulse Duration vs Threshold Overdrive Voltage(1) (1)

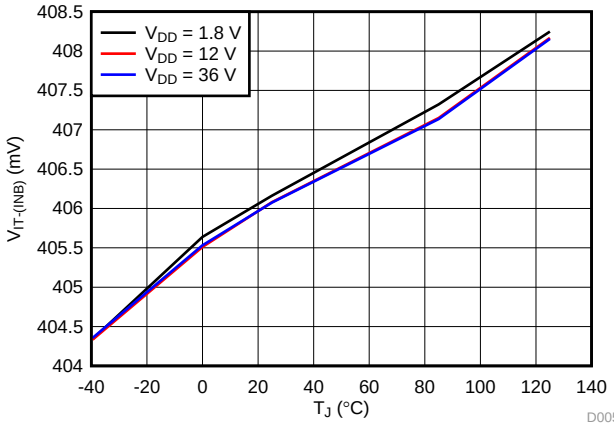


Figure 4. INA Positive Input Threshold Voltage ($V_{IT+(INA)}$) vs Temperature

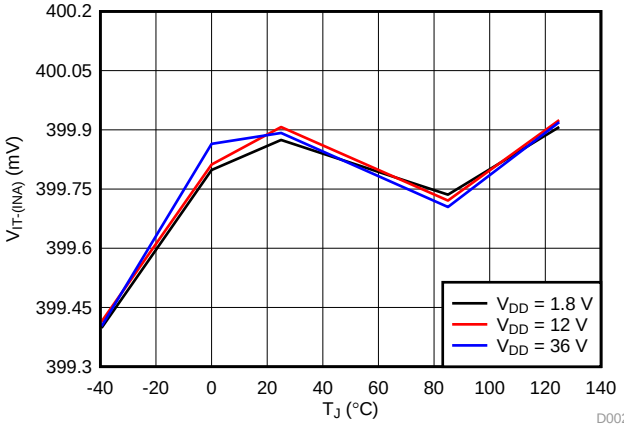


Figure 5. INA Negative Input Threshold Voltage ($V_{IT-(INA)}$) vs Temperature

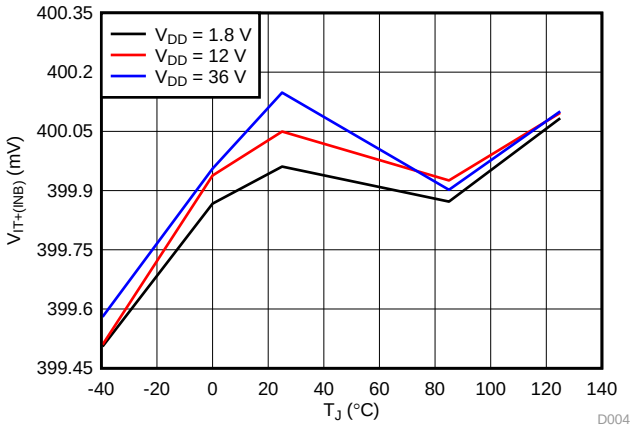


Figure 6. INB Positive Input Threshold Voltage ($V_{IT+(INB)}$) vs Temperature

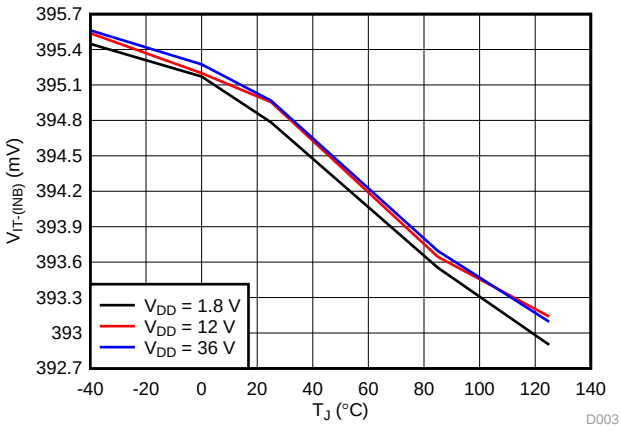


Figure 7. INB Negative Input Threshold Voltage ($V_{IT-(INB)}$) vs Temperature

(1) Minimum pulse duration required to trigger output high-to-low transition. INA = negative spike below V_{IT-} and INB = positive spike above V_{IT+}.

Typical Characteristics (continued)

At T_J = 25°C and V_{DD} = 12 V, unless otherwise noted.

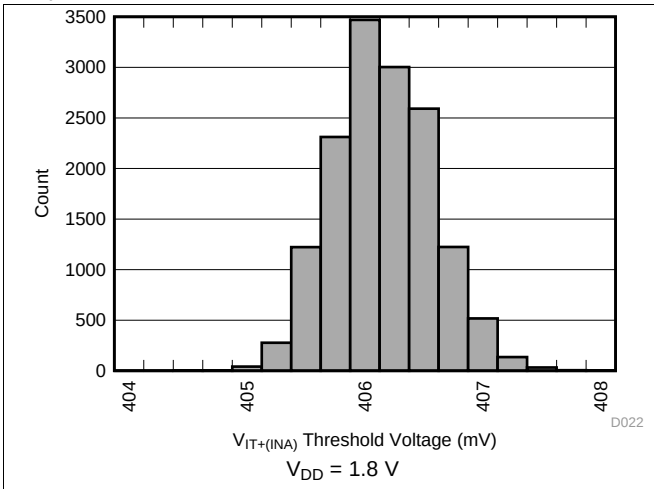


Figure 8. INA Positive Input Threshold Voltage ($V_{IT+(INA)}$) Distribution

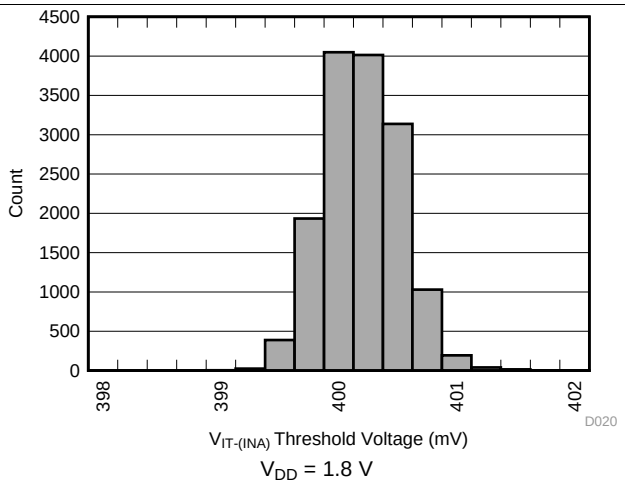


Figure 9. INA Negative Input Threshold Voltage ($V_{IT–(INA)}$) Distribution

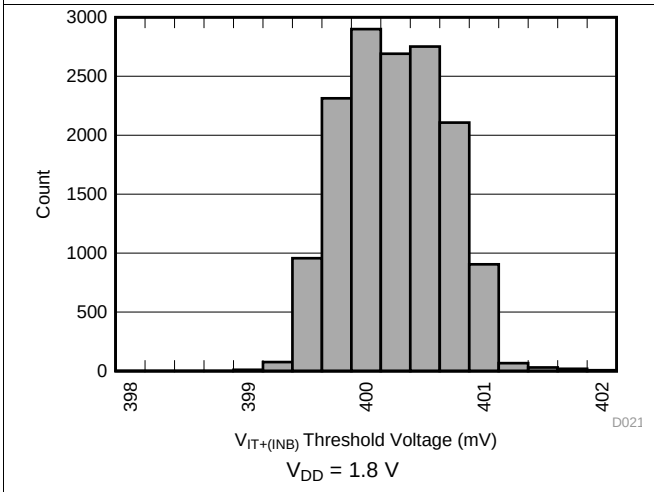


Figure 10. INB Positive Input Threshold Voltage ($V_{IT+(INB)}$) Distribution

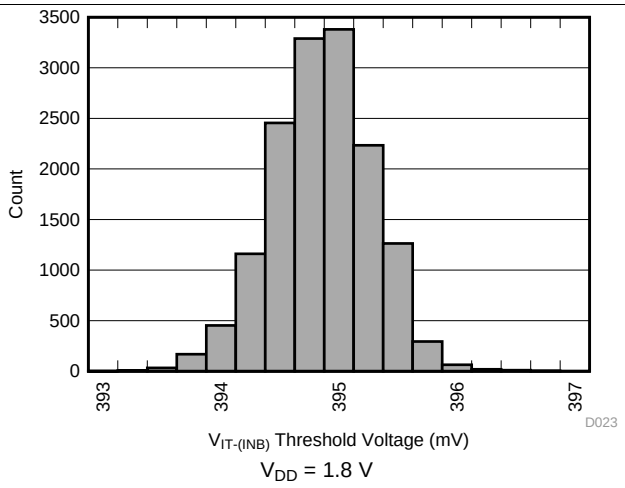


Figure 11. INB Negative Input Threshold Voltage ($V_{IT–(INB)}$) Distribution

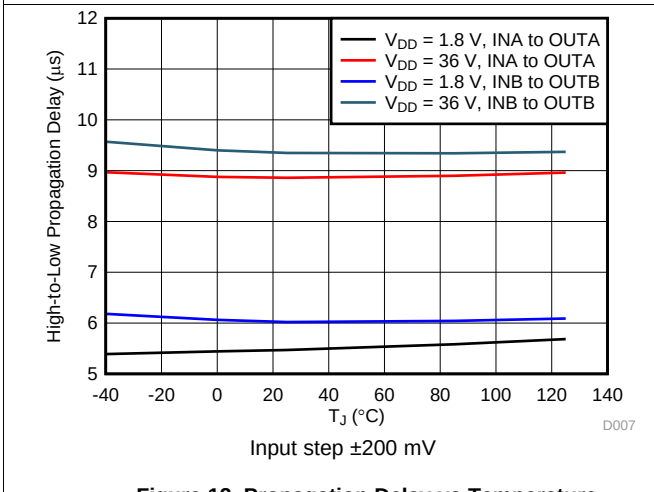


Figure 12. Propagation Delay vs Temperature (High-to-Low Transition at the Inputs)

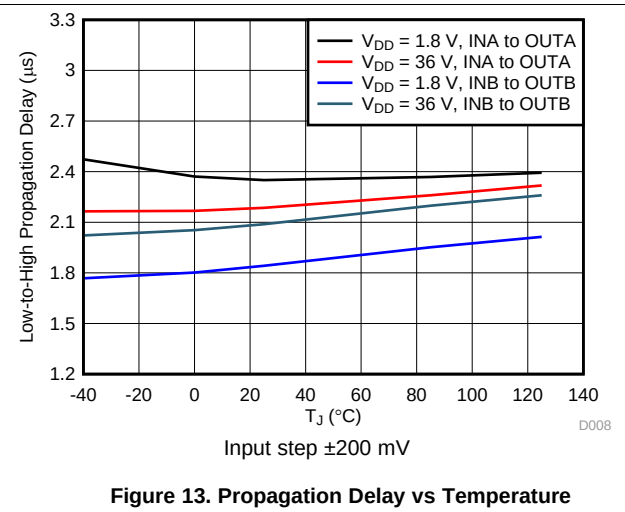
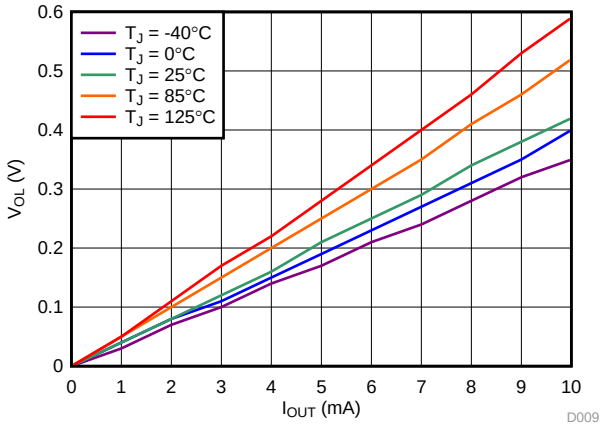


Figure 13. Propagation Delay vs Temperature (Low-to-High Transition at the Inputs)

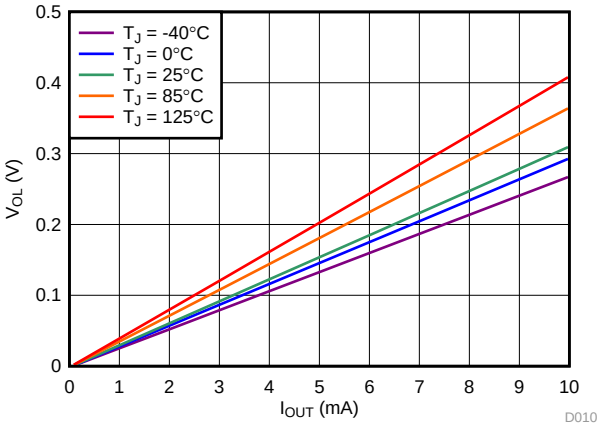
Typical Characteristics (continued)

At T_J = 25°C and V_{DD} = 12 V, unless otherwise noted.



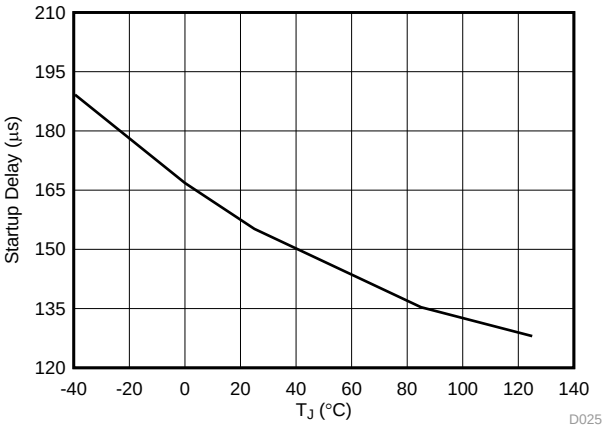
V_{DD} = 1.8 V

Figure 14. Output Voltage Low vs Output Sink Current



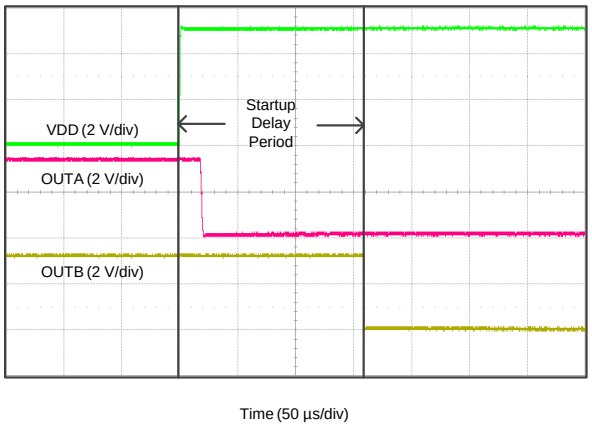
V_{DD} = 12 V

Figure 15. Output Voltage Low vs Output Sink Current



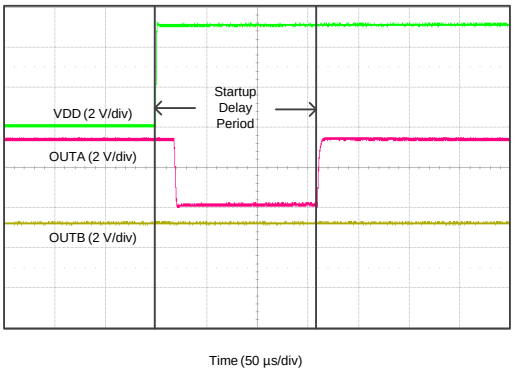
V_{DD} = 5 V

Figure 16. Start-Up Delay vs Temperature



V_{DD} = 5 V, V_{INA} = 390 mV, V_{INB} = 410 mV, V_{PULLUP} = 3.3 V

Figure 17. Start-Up Delay



V_{DD} = 5 V, V_{INA} = 410 mV, V_{INB} = 390 mV, V_{PULLUP} = 3.3 V

Figure 18. Start-Up Delay

7 Detailed Description

7.1 Overview

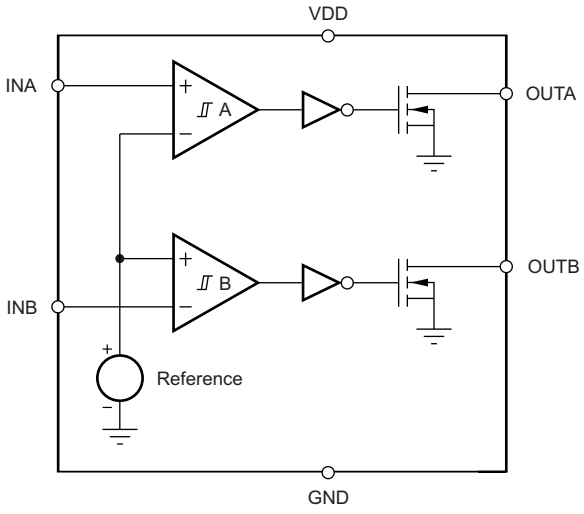
The TPS3701 combines two comparators (referred to as A and B) and a precision reference for over- and undervoltage detection. The TPS3701 features a wide supply voltage range (1.8 V to 36 V) and high-accuracy window threshold voltages of 400 mV (0.75% over temperature) with built-in hysteresis. The outputs are rated to 25 V and can sink up to 10 mA.

Set each input pin (INA, INB) to monitor any voltage above 0.4 V by using an external resistor divider network. Each input pin has very low input leakage current, allowing the use of large resistor dividers without sacrificing system accuracy. To form a window comparator, use the two input pins and three resistors (see the *Window Comparator Considerations* section). In this configuration, the TPS3701 is designed to assert the output signals when the monitored voltage is within the window band. Each input can also be used independently. The relationship between the inputs and the outputs is shown in Table 1. Broad voltage thresholds are supported that enable the device to be used in a wide array of applications.

Table 1. Truth Table

CONDITION	OUTPUT	STATUS
INA > $V_{IT+(INA)}$	OUTA high	Output A high impedance
INA < $V_{IT–(INA)}$	OUTA low	Output A asserted
INB > $V_{IT+(INB)}$	OUTB low	Output B asserted
INB < $V_{IT–(INB)}$	OUTB high	Output B asserted

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Inputs (INA, INB)

The TPS3701 combines two comparators with a precision reference voltage. Each comparator has one external input; the other input is connected to the internal reference. The rising threshold on INB and the falling threshold on INA are designed and trimmed to be equal to the reference voltage (400 mV). This configuration optimizes the device accuracy when used as a window comparator. Both comparators also have built-in hysteresis that proves immunity to noise and ensures stable operation.

The comparator inputs swings from ground to 1.7 V (7.0 V absolute maximum), regardless of the device supply voltage used. Although not required in most cases, it is good analog design practice to place a 1-nF to 10-nF bypass capacitor at the comparator input for noisy applications in order to reduce sensitivity to transient voltage changes on the monitored signal.

For comparator A, the corresponding output (OUTA) is driven to logic low when the input INA voltage drops below $V_{IT-(INA)}$. When the voltage exceeds $V_{IT+(INA)}$, OUTA goes to a high-impedance state; see Figure 1.

For comparator B, the corresponding output (OUTB) is driven to logic low when the voltage at input INB exceeds $V_{IT+(INB)}$. When the voltage drops below $V_{IT-(INB)}$ OUTB goes to a high-impedance state; see Figure 1. Together, these two comparators form a window-detection function as described in the *Window Comparator Considerations* section.

7.3.2 Outputs (OUTA, OUTB)

In a typical TPS3701 application, the outputs are connected to a reset or enable input of the processor [such as a digital signal processor (DSP), application-specific integrated circuit (ASIC), or other processor type] or the outputs are connected to the enable input of a voltage regulator [such as a DC-DC converter or low-dropout regulator (LDO)].

The TPS3701 provides two open-drain outputs (OUTA and OUTB); use pullup resistors to hold these lines high when the output goes to a high-impedance state. Connect pullup resistors to the proper voltage rails to enable the outputs to be connected to other devices at correct interface voltage levels. The TPS3701 outputs can be pulled up to 25 V, independent of the device supply voltage. To ensure proper voltage levels, give some consideration when choosing the pullup resistor values. The pullup resistor value is determined by V_{OL}, output capacitive loading, and output leakage current ($I_{D(leak)}$). These values are specified in the *Electrical Characteristics* table. Use wired-OR logic to merge OUTA and OUTB into one logic signal.

Table 1 and the *Inputs (INA, INB)* section describe how the outputs are asserted or high impedance. See Figure 1 for a timing diagram that describes the relationship between threshold voltages and the respective output.

7.4 Device Functional Modes

7.4.1 Normal Operation (V_{DD} > UVLO)

When the voltage on VDD is greater than 1.8 V for at least 155 µs, the OUTA and OUTB signals correspond to the voltage on INA and INB as listed in Table 1.

7.4.2 Undervoltage Lockout ($V_{(POR)} < V_{DD} <$ UVLO)

When the voltage on VDD is less than the device UVLO voltage, and greater than the power-on-reset voltage, $V_{(POR)}$, the OUTA and OUTB signals are asserted and high impedance, respectively, regardless of the voltage on INA and INB.

7.4.3 Power-On-Reset ($V_{DD} < V_{(POR)}$)

When the voltage on VDD is lower than the required voltage to internally pull the asserted output to GND ($V_{(POR)}$), both outputs are in a high-impedance state.

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The TPS3701 is used as a precision dual-voltage supervisor in several different configurations. The monitored voltage (V_{MON}), VDD voltage, and output pullup voltage can be independent voltages or connected in any configuration. The following sections show the connection configurations and the voltage limitations for each configuration.

8.1.1 Window Comparator Considerations

The inverting and noninverting configuration of the comparators forms a window-comparator detection circuit using a resistor divider network, as shown in Figure 19 and Figure 20. The input pins can monitor any system voltage above 400 mV with the use of a resistor divider network. INA and INB monitor for undervoltage and overvoltage conditions, respectively.

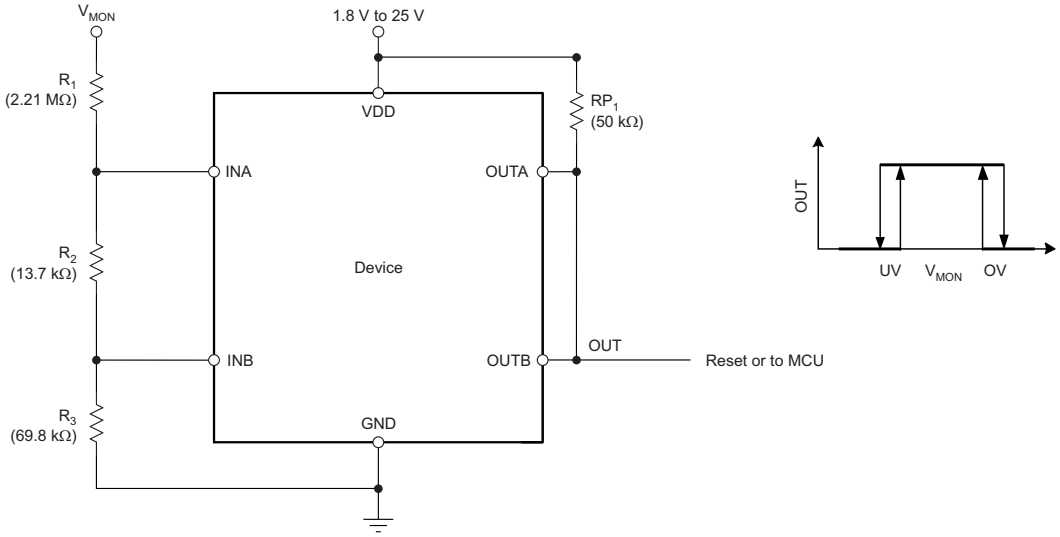


Figure 19. Window Comparator Block Diagram

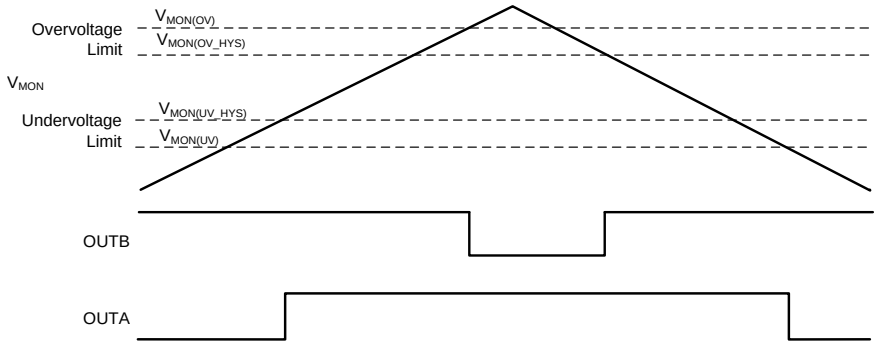


Figure 20. Window Comparator Timing Diagram

Application Information (continued)

The TPS3701 flags the overvoltage or undervoltage condition with the greatest accuracy. The highest accuracy threshold voltages are $V_{IT-(INA)}$ and $V_{IT+(INB)}$, and correspond with the falling undervoltage flag, and the rising overvoltage flag, respectively. These thresholds represent the accuracy when the monitored voltage is within the valid window (both OUTA and OUTB are in a high-impedance state), and correspond to the $V_{MON(UV)}$ and $V_{MON(OV)}$ trigger voltages, respectively. If the monitored voltage is outside of the valid window (V_{MON} is less than the undervoltage limit, $V_{MON(UV)}$, or greater than overvoltage limit, $V_{MON(OV)}$), then the input threshold voltages to re-enter the valid window are $V_{IT+(INA)}$ or $V_{IT-(INB)}$, and correspond with the $V_{MON(UV\_HYS)}$ and $V_{MON(OV\_HYS)}$ monitored voltages, respectively.

The resistor divider values and target threshold voltage can be calculated by using Equation 1 through Equation 4:

$$R_{TOTAL} = R_1 + R_2 + R_3 \quad (1)$$

Choose an R_{TOTAL} value so that the current through the divider is approximately 100 times higher than the input current at the INA and INB pins. Resistors with high values minimize current consumption; however, the input bias current degrades accuracy if the current through the resistors is too low. See application report *SLVA450, Optimizing Resistor Dividers at a Comparator Input* (SLVA450), for details on sizing input resistors.

R_3 is determined by Equation 2:

$$R_3 = \frac{R_{TOTAL}}{V_{MON(OV)}} \bullet V_{IT+(INB)} \quad (2)$$

where

- $V_{MON(OV)}$ is the target voltage at which an overvoltage condition is detected.

R_2 is determined by either Equation 3 or Equation 4:

$$R_2 = \left(\frac{R_{TOTAL}}{V_{MON(UV\_HYS)}} \bullet V_{IT+(INA)} \right) - R_3 \quad (3)$$

where

- $V_{MON(UV\_HYS)}$ is the target voltage at which an undervoltage condition is removed as V_{MON} rises.

$$R_2 = \left(\frac{R_{TOTAL}}{V_{MON(UV)}} \bullet V_{IT-(INA)} \right) - R_3 \quad (4)$$

where

- $V_{MON(UV)}$ is the target voltage at which an undervoltage condition is detected.

8.1.2 Input and Output Configurations

Figure 21 to Figure 24 show examples of the various input and output configurations.

Application Information (continued)

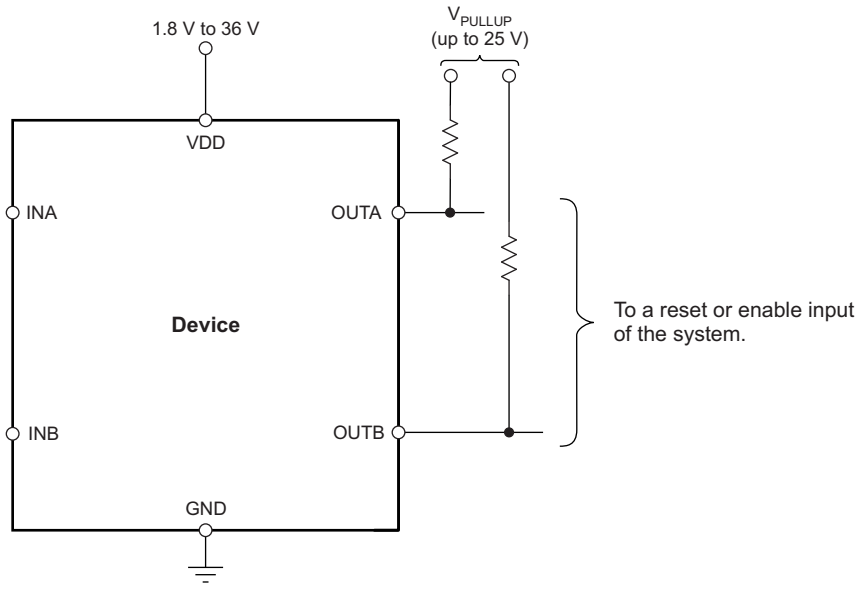


Figure 21. Interfacing to Voltages Other than V_{DD}

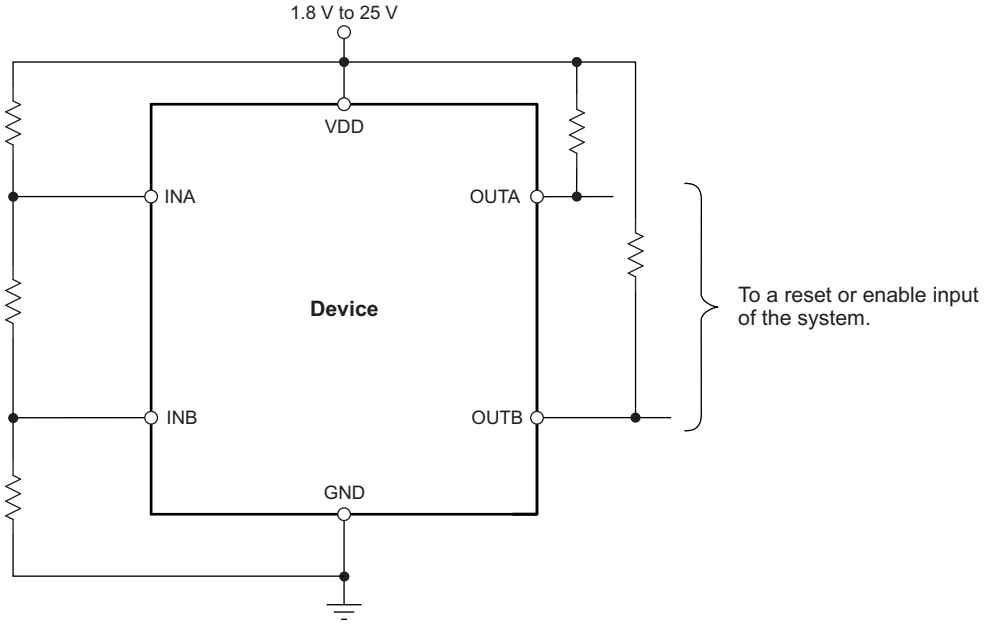
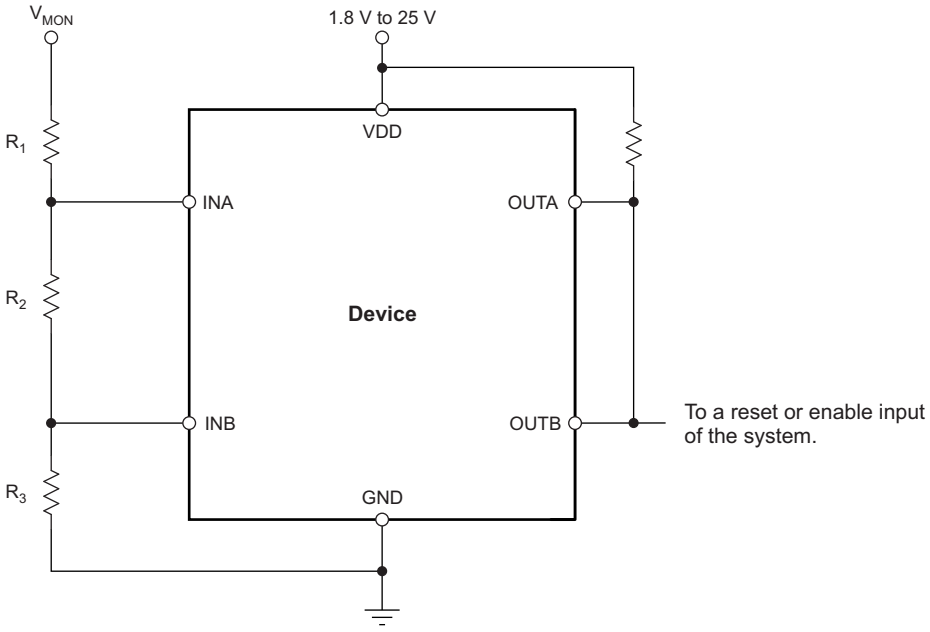


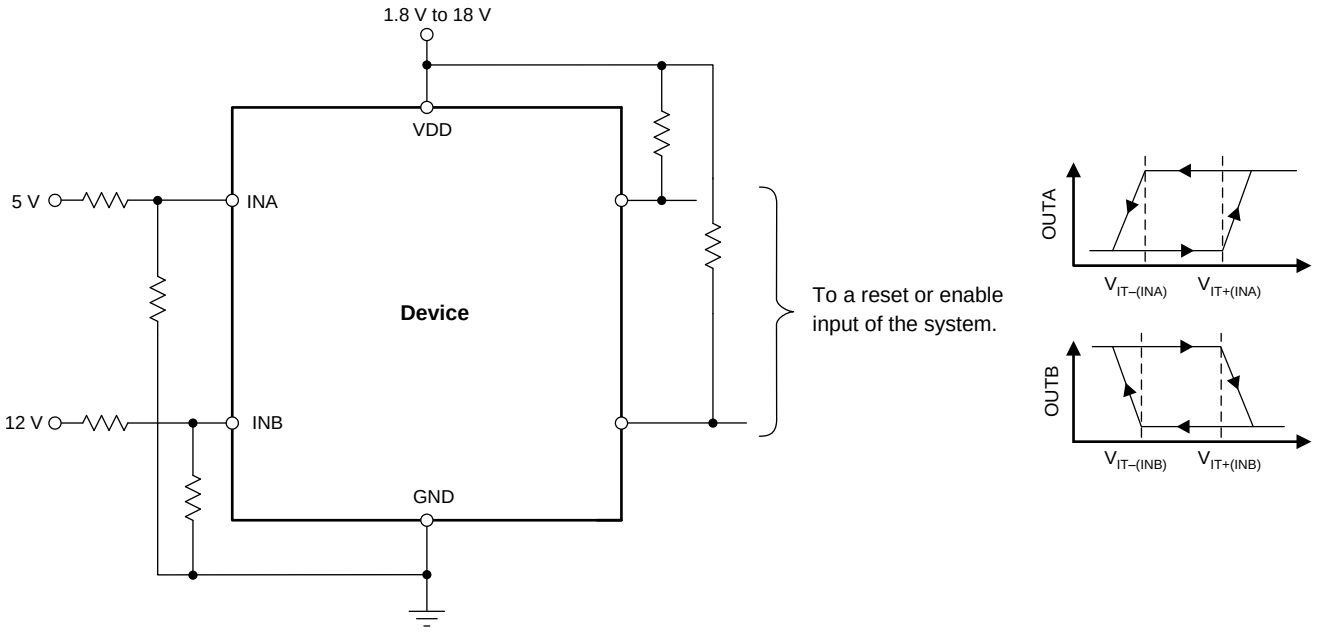
Figure 22. Monitoring the Same Voltage as V_{DD}

Application Information (continued)



NOTE: The inputs can monitor a voltage higher than V_{DD} (max) with the use of an external resistor divider network.

Figure 23. Monitoring a Voltage Other than V_{DD}



NOTE: In this case, OUTA is driven low when an undervoltage condition is detected at the 5-V rail and OUTB is driven low when an overvoltage condition is detected at the 12-V rail.

Figure 24. Monitoring Overvoltage for One Rail and Undervoltage for a Different Rail

8.1.3 Immunity to Input Pin Voltage Transients

The TPS3701 is immune to short voltage transient spikes on the input pins. Sensitivity to transients depends on both transient duration and amplitude; see Figure 3, *Minimum Pulse Duration vs Threshold Overdrive Voltage*.

8.2 Typical Application

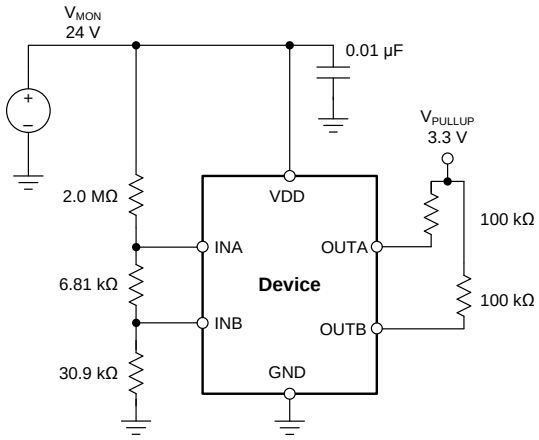


Figure 25. 24-V, 10% Window Comparator

8.2.1 Design Requirements

Table 2 lists the design parameters for this example.

Table 2. Design Parameters

PARAMETER	DESIGN REQUIREMENT	DESIGN RESULT
Monitored voltage	24-V nominal, rising ($V_{MON(OV)}$) and falling ($V_{MON(UV)}$) threshold ±10% nominal (26.4 V and 21.6 V, respectively)	$V_{MON(OV)}$ = 26.4 V ±2.7%, $V_{MON(UV)}$ = 21.6 V ±2.7%
Output logic voltage	3.3-V CMOS	3.3-V CMOS
Maximum current consumption	30 µA	24 µA

8.2.2 Detailed Design Procedure

1. Determine the minimum total resistance of the resistor network necessary to achieve the current consumption specification by using Equation 1. For this example, the current flow through the resistor network was chosen to be 13 µA; a lower current can be selected. However, take care to avoid leakage currents that are artifacts of the manufacturing process. Leakage currents significantly impact the accuracy if they are greater than 1% of the resistor network current.

$$R_{TOTAL} = \frac{V_{MON(OV)}}{I} = \frac{26.4\ V}{13\ \mu A} = 2.03\ M\Omega \quad (5)$$

where

- $V_{MON(OV)}$ is the target voltage at which an overvoltage condition is detected as V_{MON} rises.
- I is the current flowing through the resistor network.

2. After R_{TOTAL} is determined, R_3 can be calculated using Equation 6. Select the nearest 1% resistor value for R_3. In this case, 30.9 kΩ is the closest value.

$$R_3 = \frac{R_{TOTAL}}{V_{MON(OV)}} \bullet V_{IT+(INB)} = \frac{2.03\ M\Omega}{26.4\ V} \bullet 0.4\ V = 30.7\ k\Omega \quad (6)$$

3. Use Equation 7 to calculate R2. Select the nearest 1% resistor value for R_2. In this case, 6.81 kΩ is the closest value.

$$R_2 = \frac{R_{TOTAL}}{V_{MON(UV)}} \bullet V_{IT-(INA+)} - R_3 = \frac{2.03\ M\Omega}{21.6\ V} \bullet 0.4\ V - 30.9\ k\Omega = 6.69\ k\Omega \quad (7)$$

4. Use Equation 8 to calculate R1. Select the nearest 1% resistor value for R_1. In this case, 2 MΩ is the closest value.

$$R_1 = R_{TOTAL} - R_2 - R_3 = 2.03\ M\Omega - 6.81\ k\Omega - 30.9\ k\Omega = 1.99\ M\Omega \quad (8)$$

5. The worst-case tolerance can be calculated by referring to Equation 13 in application report *Optimizing Resistor Dividers at a Comparator Input* (SLVA450). An example of the rising threshold error, $V_{MON(OV)}$, is given in Equation 9:

$$\%\ ACC = \%\ TOL(V_{IT+(INB)}) + 2 \bullet \left(1 - \frac{V_{IT+(INB)}}{V_{MON(OV)}}\right) \bullet \%\ TOL_R = 0.75\ \% + 2 \bullet \left(1 - \frac{0.4}{26.4}\right) \bullet 1\% = 2.72\ \% \quad (9)$$

where

- % TOL($V_{IT+(INB)}$) is the tolerance of the INB positive threshold.
- % ACC is the total tolerance of the $V_{MON(OV)}$ voltage.
- % TOL_R is the tolerance of the resistors selected.

6. When the outputs switch to the high-Z state, the rise time of the OUTA or OUTB node depends on the pullup resistance and the capacitance on the node. Choose pullup resistors that satisfy the downstream timing requirements; 100-kΩ resistors are a good choice for low-capacitive loads.

8.2.3 Application Curve

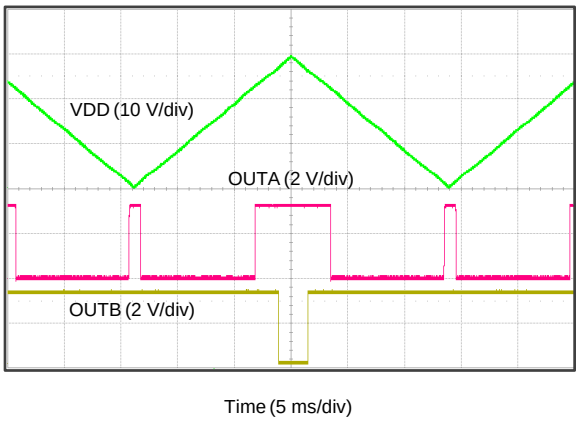


Figure 26. 24-V Window Monitor Output Response

9 Power Supply Recommendations

The TPS3701 has a 40-V absolute maximum rating on the VDD pin, with a recommended operating condition of 36 V. If the voltage supply that is providing power to VDD is susceptible to any large voltage transient that may exceed 40 V, or if the supply exhibits high voltage slew rates greater than 1 V/µs, take additional precautions. Place an RC filter between the supply and VDD to filter any high-frequency transient surges on the VDD pin. A 100-Ω resistor and 0.01-µF capacitor is required in these cases, as shown in Figure 27.

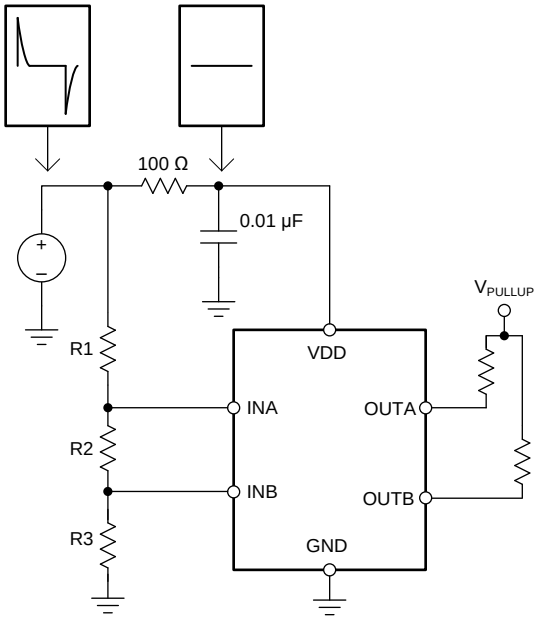


Figure 27. Using an RC Filter to Remove High-Frequency Disturbances on VDD

10 Layout

10.1 Layout Guidelines

- Place R_1, R_2, and R_3 close to the device to minimize noise coupling into the INA and INB nodes.
- Place the VDD decoupling capacitor close to the device.
- Avoid using long traces for the VDD supply node. The VDD capacitor (C_{VDD}), along with parasitic inductance from the supply to the capacitor, may form an LC tank and create ringing with peak voltages above the maximum VDD voltage. If this is unavoidable, see Figure 27 for an example of filtering VDD.

10.2 Layout Example

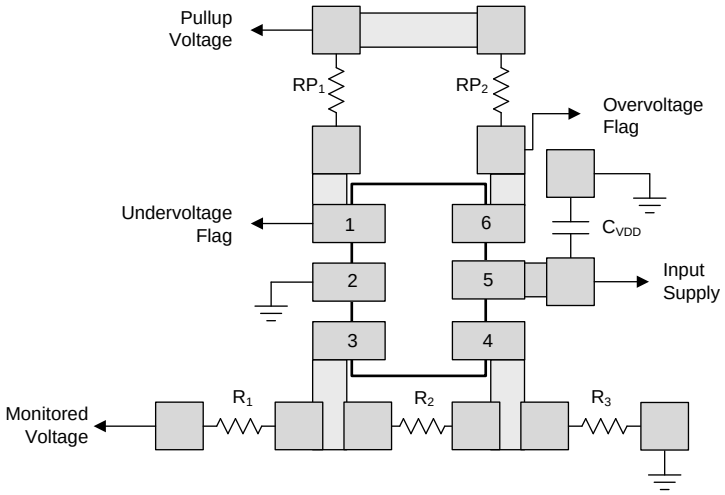


Figure 28. Recommended Layout

11 Device and Documentation Support

11.1 Documentation Support

11.1.1 Related Documentation

For related documentation see the following application reports and user guide (available through the TI website):

- Application report *Using the TPS3700 as a Negative Rail Over- and Undervoltage Detector* (SLVA600).
- Application report *Optimizing Resistor Dividers at a Comparator Input* (SLVA450).
- User guide *TPS3700EVM-114 Evaluation Module* (SLVU683).

11.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.4 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

11.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS3701DDCR	ACTIVE	SOT-23-THIN	DDC	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ZABO	Samples
TPS3701DDCT	ACTIVE	SOT-23-THIN	DDC	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR		ZABO	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

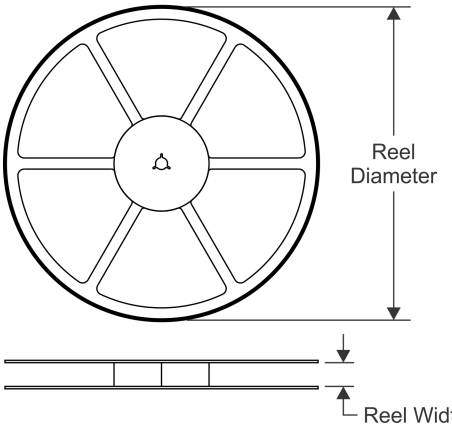
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

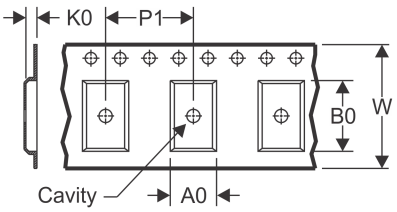
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

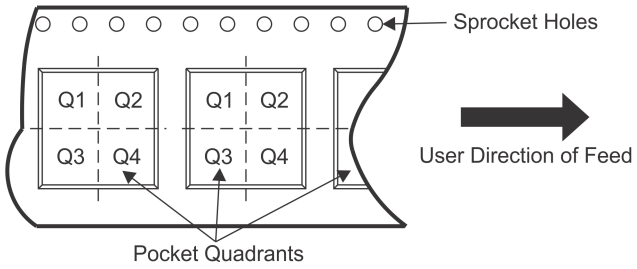


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

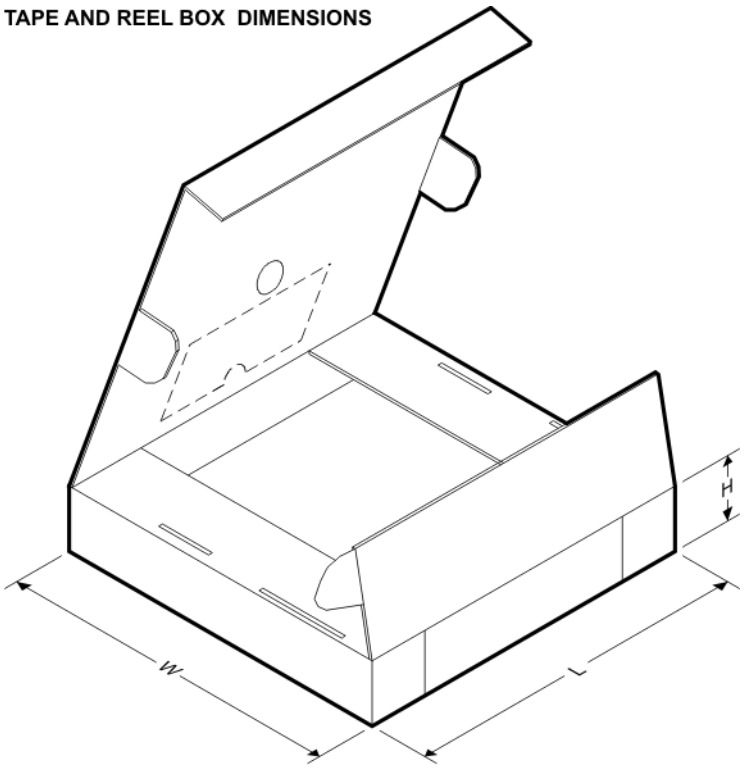
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS3701DDCR	SOT-23-THIN	DDC	6	3000	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS3701DDCT	SOT-23-THIN	DDC	6	250	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3

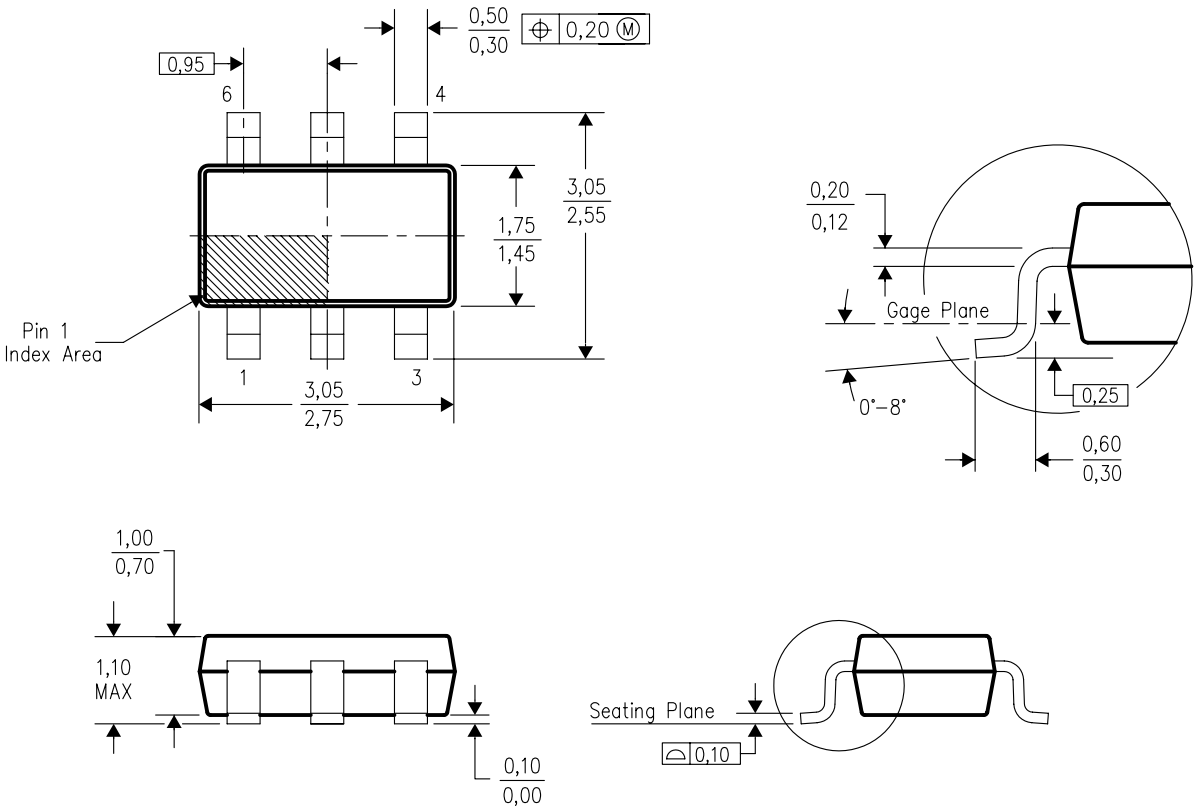
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS3701DDCR	SOT-23-THIN	DDC	6	3000	195.0	200.0	45.0
TPS3701DDCT	SOT-23-THIN	DDC	6	250	195.0	200.0	45.0

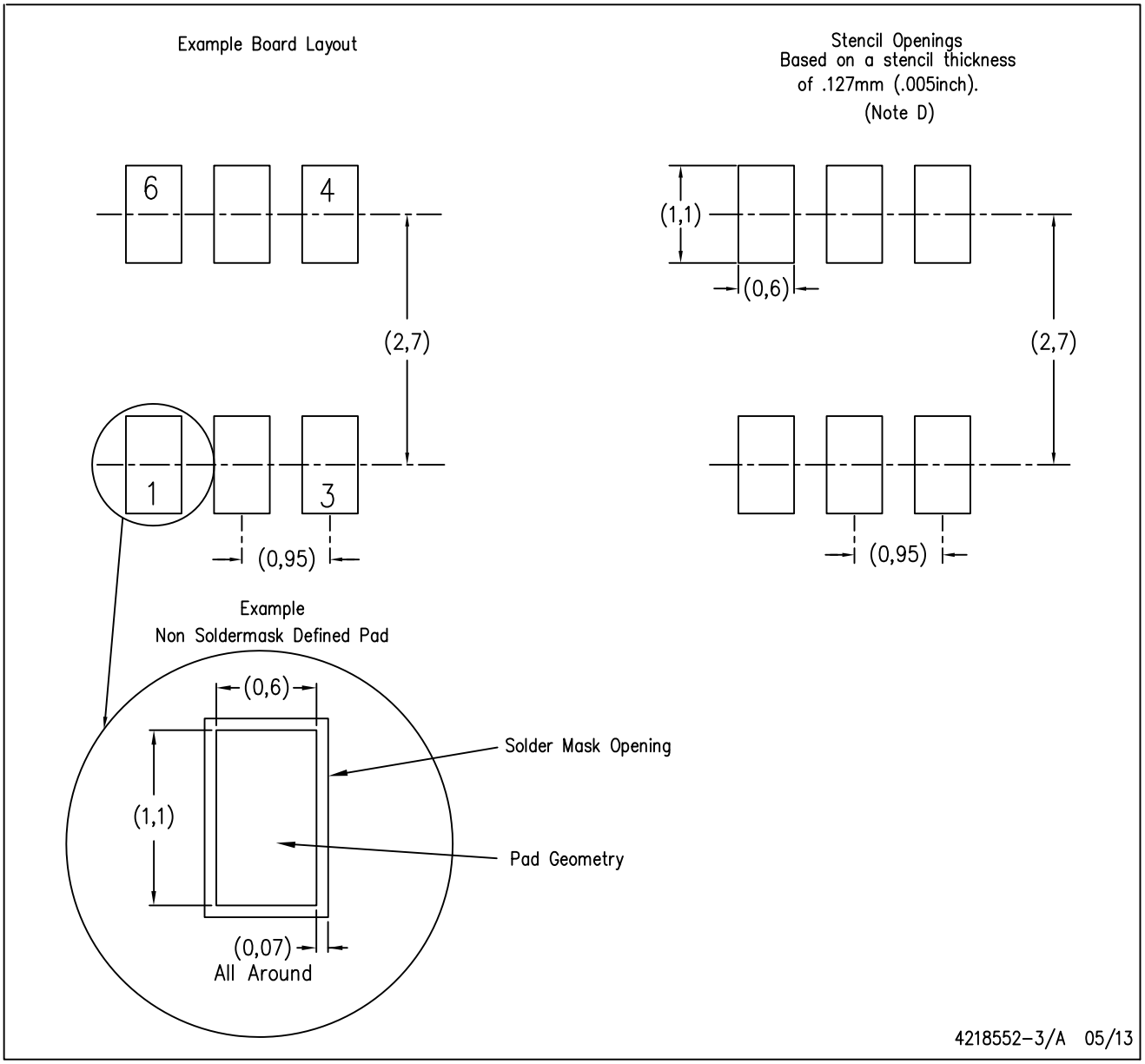
DDC (R–PDSO–G6) PLASTIC SMALL–OUTLINE



4204403–3/E 06/05

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion.
D. Falls within JEDEC MO–193 variation AA (6 pin).

DDC (R–PDSO–G6) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.

IMPORTANT NOTICE

Texas Instruments Incorporated (TI) reserves the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete.

TI's published terms of sale for semiconductor products (http://www.ti.com/sc/docs/stdterms.htm) apply to the sale of packaged integrated circuit products that TI has qualified and released to market. Additional terms may apply to the use or sale of other types of TI products and services.

Reproduction of significant portions of TI information in TI data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such reproduced documentation. Information of third parties may be subject to additional restrictions. Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyers and others who are developing systems that incorporate TI products (collectively, "Designers") understand and agree that Designers remain responsible for using their independent analysis, evaluation and judgment in designing their applications and that Designers have full and exclusive responsibility to assure the safety of Designers' applications and compliance of their applications (and of all TI products used in or for Designers' applications) with all applicable regulations, laws and other applicable requirements. Designer represents that, with respect to their applications, Designer has all the necessary expertise to create and implement safeguards that (1) anticipate dangerous consequences of failures, (2) monitor failures and their consequences, and (3) lessen the likelihood of failures that might cause harm and take appropriate actions. Designer agrees that prior to using or distributing any applications that include TI products, Designer will thoroughly test such applications and the functionality of such TI products as used in such applications.

TI's provision of technical, application or other design advice, quality characterization, reliability data or other services or information, including, but not limited to, reference designs and materials relating to evaluation modules, (collectively, "TI Resources") are intended to assist designers who are developing applications that incorporate TI products; by downloading, accessing or using TI Resources in any way, Designer (individually or, if Designer is acting on behalf of a company, Designer's company) agrees to use any particular TI Resource solely for this purpose and subject to the terms of this Notice.

TI's provision of TI Resources does not expand or otherwise alter TI's applicable published warranties or warranty disclaimers for TI products, and no additional obligations or liabilities arise from TI providing such TI Resources. TI reserves the right to make corrections, enhancements, improvements and other changes to its TI Resources. TI has not conducted any testing other than that specifically described in the published documentation for a particular TI Resource.

Designer is authorized to use, copy and modify any individual TI Resource only in connection with the development of applications that include the TI product(s) identified in such TI Resource. NO OTHER LICENSE, EXPRESS OR IMPLIED, BY ESTOPPEL OR OTHERWISE TO ANY OTHER TI INTELLECTUAL PROPERTY RIGHT, AND NO LICENSE TO ANY TECHNOLOGY OR INTELLECTUAL PROPERTY RIGHT OF TI OR ANY THIRD PARTY IS GRANTED HEREIN, including but not limited to any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information regarding or referencing third-party products or services does not constitute a license to use such products or services, or a warranty or endorsement thereof. Use of TI Resources may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

TI RESOURCES ARE PROVIDED "AS IS" AND WITH ALL FAULTS. TI DISCLAIMS ALL OTHER WARRANTIES OR REPRESENTATIONS, EXPRESS OR IMPLIED, REGARDING RESOURCES OR USE THEREOF, INCLUDING BUT NOT LIMITED TO ACCURACY OR COMPLETENESS, TITLE, ANY EPIDEMIC FAILURE WARRANTY AND ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, AND NON-INFRINGEMENT OF ANY THIRD PARTY INTELLECTUAL PROPERTY RIGHTS. TI SHALL NOT BE LIABLE FOR AND SHALL NOT DEFEND OR INDEMNIFY DESIGNER AGAINST ANY CLAIM, INCLUDING BUT NOT LIMITED TO ANY INFRINGEMENT CLAIM THAT RELATES TO OR IS BASED ON ANY COMBINATION OF PRODUCTS EVEN IF DESCRIBED IN TI RESOURCES OR OTHERWISE. IN NO EVENT SHALL TI BE LIABLE FOR ANY ACTUAL, DIRECT, SPECIAL, COLLATERAL, INDIRECT, PUNITIVE, INCIDENTAL, CONSEQUENTIAL OR EXEMPLARY DAMAGES IN CONNECTION WITH OR ARISING OUT OF TI RESOURCES OR USE THEREOF, AND REGARDLESS OF WHETHER TI HAS BEEN ADVISED OF THE POSSIBILITY OF SUCH DAMAGES.

Unless TI has explicitly designated an individual product as meeting the requirements of a particular industry standard (e.g., ISO/TS 16949 and ISO 26262), TI is not responsible for any failure to meet such industry standard requirements.

Where TI specifically promotes products as facilitating functional safety or as compliant with industry functional safety standards, such products are intended to help enable customers to design and create their own applications that meet applicable functional safety standards and requirements. Using products in an application does not by itself establish any safety features in the application. Designers must ensure compliance with safety-related requirements and standards applicable to their applications. Designer may not use any TI products in life-critical medical equipment unless authorized officers of the parties have executed a special contract specifically governing such use. Life-critical medical equipment is medical equipment where failure of such equipment would cause serious bodily injury or death (e.g., life support, pacemakers, defibrillators, heart pumps, neurostimulators, and implantables). Such equipment includes, without limitation, all medical devices identified by the U.S. Food and Drug Administration as Class III devices and equivalent classifications outside the U.S.

TI may expressly designate certain products as completing a particular qualification (e.g., Q100, Military Grade, or Enhanced Product). Designers agree that it has the necessary expertise to select the product with the appropriate qualification designation for their applications and that proper product selection is at Designers' own risk. Designers are solely responsible for compliance with all legal and regulatory requirements in connection with such selection.

Designer will fully indemnify TI and its representatives against any damages, costs, losses, and/or liabilities arising out of Designer's non-compliance with the terms and provisions of this Notice.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265