

## DS26C31x CMOS Quad Tri-State Differential Line Driver

### 1 Features

- TTL Input Compatible
- Typical Propagation Delays: 6 ns
- Typical Output Skew: 0.5 ns
- Outputs Will Not Load Line When  $V_{CC} = 0\text{ V}$
- DS26C31T Meets the Requirements of EIA Standard RS-422
- Operation From Single 5-V Supply
- Tri-State Outputs for Connection to System Buses
- Low Quiescent Current
- Available in Surface Mount
- Mil-Std-883C Compliant

### 2 Applications

Differential Line Driver for RS-422 Applications

### 3 Description

The DS26C31 device is a quad differential line driver designed for digital data transmission over balanced lines. The DS26C31T meets all the requirements of EIA standard RS-422 while retaining the low power characteristics of CMOS. The DS26C31M is compatible with EIA standard RS-422; however, one exception in test methodology is taken<sup>(2)</sup>. This enables the construction of serial and terminal interfaces while maintaining minimal power consumption.

The DS26C31 accepts TTL or CMOS input levels and translates these to RS-422 output levels. This part uses special output circuitry that enables the drivers to power down without loading down the bus. This device has enable and disable circuitry common to all four drivers. The DS26C31 is pin compatible to the AM26LS31 and the DS26LS31.

All inputs are protected against damage due to electrostatic discharge by diodes to  $V_{CC}$  and ground.

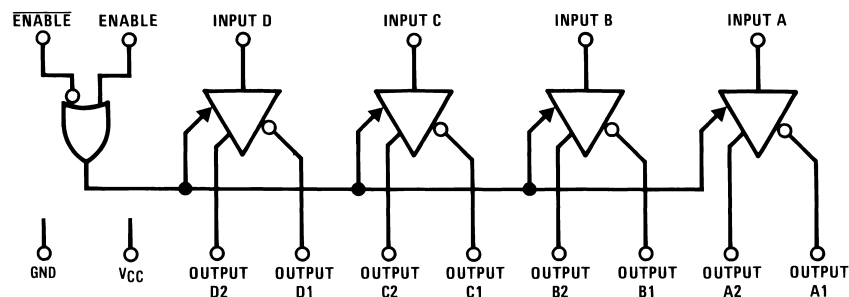
#### Device Information<sup>(1)</sup>

PART NUMBER	PACKAGE	BODY SIZE (NOM)
DS26C31M	SNLS3759577	9.90 mm × 3.91 mm
	PDIP (16)	19.304 mm × 6.35 mm
DS26C31T	SNLS3759577	9.90 mm × 3.91 mm
	PDIP (16)	19.304 mm × 6.35 mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.

(2) The DS26C31M (–55°C to 125°C) is tested with  $V_{OUT}$  between 6 V and 0 V while RS-422A condition is 6 V and –0.25 V.

### 4 Device Logic Diagram



## Table of Contents

<b>1 Features</b> .....	<b>1</b>	9.2 Functional Block Diagram .....	<b>13</b>
<b>2 Applications</b> .....	<b>1</b>	9.3 Feature Description .....	<b>13</b>
<b>3 Description</b> .....	<b>1</b>	9.4 Device Functional Modes .....	<b>13</b>
<b>4 Device Logic Diagram</b> .....	<b>1</b>	<b>10 Application and Implementation</b> .....	<b>14</b>
<b>5 Revision History</b> .....	<b>2</b>	10.1 Application Information .....	<b>14</b>
<b>6 Pin Configuration and Functions</b> .....	<b>3</b>	10.2 Typical Application .....	<b>14</b>
<b>7 Specifications</b> .....	<b>4</b>	<b>11 Power Supply Recommendations</b> .....	<b>16</b>
7.1 Absolute Maximum Ratings .....	<b>4</b>	<b>12 Layout</b> .....	<b>16</b>
7.2 Recommended Operating Conditions .....	<b>4</b>	12.1 Layout Guidelines .....	<b>16</b>
7.3 DC Electrical Characteristics .....	<b>5</b>	12.2 Layout Example .....	<b>16</b>
7.4 Switching Characteristics .....	<b>6</b>	<b>13 Device and Documentation Support</b> .....	<b>17</b>
7.5 Comparison Table of Switching Characteristics into "LS-Type" Load .....	<b>6</b>	13.1 Related Links .....	<b>17</b>
7.6 Typical Characteristics .....	<b>7</b>	13.2 Trademarks .....	<b>17</b>
<b>8 Parameter Measurement Information</b> .....	<b>11</b>	13.3 Electrostatic Discharge Caution .....	<b>17</b>
<b>9 Detailed Description</b> .....	<b>13</b>	13.4 Glossary .....	<b>17</b>
9.1 Overview .....	<b>13</b>	<b>14 Mechanical, Packaging, and Orderable Information</b> .....	<b>17</b>

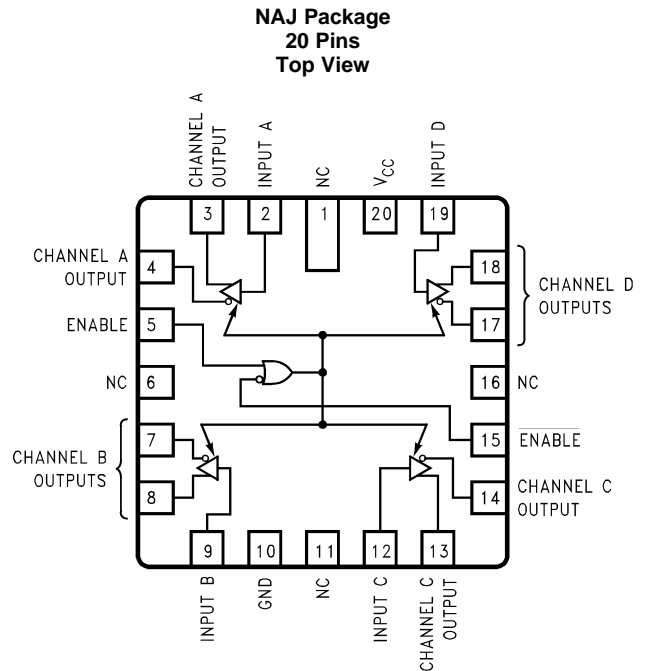
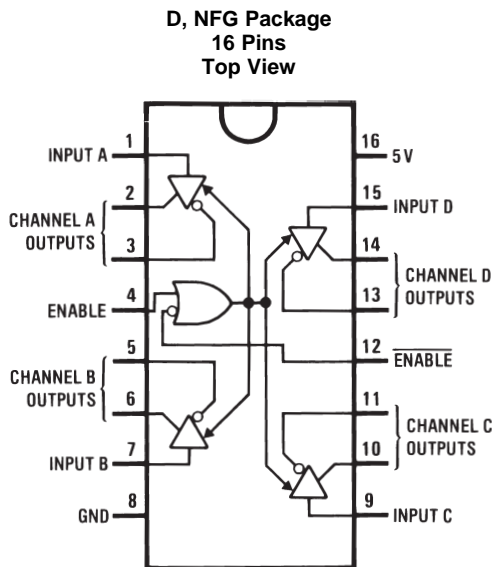
## 5 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

<b>Changes from Revision B (April 2013) to Revision C</b>	<b>Page</b>
<ul style="list-style-type: none"> <li>Added <i>Feature Description</i> section, <i>Device Functional Modes</i>, <i>Application and Implementation</i> section, <i>Power Supply Recommendations</i> section, <i>Layout</i> section, <i>Device and Documentation Support</i> section, and <i>Mechanical, Packaging, and Orderable Information</i> section .....</li> </ul>	<b>1</b>

<b>Changes from Revision A (April 2013) to Revision B</b>	<b>Page</b>
<ul style="list-style-type: none"> <li>Changed layout of National Data Sheet to TI format .....</li> </ul>	<b>9</b>

## 6 Pin Configuration and Functions



### Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO. <sup>(1)</sup>		
<b>DIFFERENTIAL SIGNALING I/O</b>			
CHANNEL A OUTPUTS (-, +)	3, 2	O	Channel A inverting and non-inverting differential driver outputs
CHANNEL B OUTPUTS (-, +)	5, 6	O	Channel B inverting and non-inverting differential driver outputs
CHANNEL C OUTPUTS (-, +)	11, 10	O	Channel C inverting and non-inverting differential driver outputs
CHANNEL D OUTPUTS (-, +)	13, 14	O	Channel D inverting and non-inverting differential driver outputs
INPUT A	1	I	TTL/CMOS compatible input for channel A
INPUT B	7	I	TTL/CMOS compatible input for channel B
INPUT C	9	I	TTL/CMOS compatible input for channel C
INPUT D	15	I	TTL/CMOS compatible input for channel D
<b>CONTROL PINS</b>			
ENABLE	4	I	Logic-high ENABLE Control
ENABLE	12	I	Logic-low ENABLE Control
<b>POWER</b>			
GND	8	—	GND Pin
VCC	16	—	Supply pin, provide 5 V supply

(1) Pin numbers correspond to PDIP and SOIC packages.

## 7 Specifications

### 7.1 Absolute Maximum Ratings<sup>(1)(2)(3)</sup>

		MIN	MAX	UNIT
Supply Voltage ( $V_{CC}$ )		-0.5	7	V
DC Input Voltage ( $V_{IN}$ )		-1.5	$V_{CC} + 1.5$	V
DC Output Voltage ( $V_{OUT}$ )		-0.5	7	V
Clamp Diode Current ( $I_{IK}, I_{OK}$ )		-20	20	mA
DC Output Current, per pin ( $I_{OUT}$ )		-150	150	mA
DC $V_{CC}$ or GND Current, per pin ( $I_{CC}$ )				
Max Power Dissipation ( $P_D$ ) at 25°C <sup>(4)</sup>	Ceramic "NFE" package		2419	mW
	Plastic "NFG" package		1736	mW
	SOIC "D" package		1226	mW
	Ceramic "NAD" package		1182	mW
	Ceramic "NAJ" package		2134	mW
Lead Temperature ( $T_L$ )	(Soldering, 4 s)		260	°C
Storage Temperature, $T_{stg}$		-65	150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) Unless otherwise specified, all voltages are referenced to ground. All currents into device pins are positive, all currents out of device pins are negative.
- (3) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/ Distributors for availability and specifications.
- (4) Ratings apply to ambient temperature at 25°C. Above this temperature derate NFG package at 13.89 mW/°C, NFE package 16.13 mW/°C, D package 9.80 mW/°C, NAJ package 12.20 mW/°C, and NAD package 6.75 mW/°C.

### 7.2 Recommended Operating Conditions

		MIN	MAX	UNIT
Supply Voltage ( $V_{CC}$ )		4.50	5.50	V
DC Input or Output Voltage	( $V_{IN}, V_{OUT}$ )	0	$V_{CC}$	V
Operating Temperature Range ( $T_A$ )	DS26C31T	-40	85	°C
	DS26C31M	-55	125	°C
Input Rise or Fall Times ( $t_r, t_f$ )			500	ns

### 7.3 DC Electrical Characteristics

 $V_{CC} = 5\text{ V} \pm 10\%$  (unless otherwise specified)<sup>(1)</sup>

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT	
$V_{IH}$	High Level Input Voltage	2.0			V	
$V_{IL}$	Low Level Input Voltage			0.8	V	
$V_{OH}$	High Level Output Voltage	$V_{IN} = V_{IH}$ or $V_{IL}$ , $I_{OUT} = -20\text{ mA}$	2.5	3.4	V	
$V_{OL}$	Low Level Output Voltage	$V_{IN} = V_{IH}$ or $V_{IL}$ , $I_{OUT} = 20\text{ mA}$		0.3	0.5	V
$V_T$	Differential Output Voltage	$R_L = 100\ \Omega$ See <sup>(2)</sup>	2.0	3.1	V	
$ V_T  -  \overline{V_T} $	Difference In Differential Output	$R_L = 100\ \Omega$ See <sup>(2)</sup>		0.4	V	
$V_{OS}$	Common Mode Output Voltage	$R_L = 100\ \Omega$ See <sup>(2)</sup>	1.8	3.0	V	
$ V_{OS} - \overline{V_{OS}} $	Difference In Common Mode Output	$R_L = 100\ \Omega$ See <sup>(2)</sup>		0.4	V	
$I_{IN}$	Input Current	$V_{IN} = V_{CC}, \text{GND}, V_{IH}, \text{ or } V_{IL}$		$\pm 1.0$	$\mu\text{A}$	
$I_{CC}$	Quiescent Supply Current <sup>(3)</sup>	DS26C31T	$V_{IN} = V_{CC}$ or GND	200	500	$\mu\text{A}$
			$V_{IN} = 2.4\text{ V}$ or $0.5\text{ V}$ <sup>(3)</sup>	0.8	2.0	mA
		DS26C31M	$V_{IN} = V_{CC}$ or GND	200	500	$\mu\text{A}$
			$V_{IN} = 2.4\text{ V}$ or $0.5\text{ V}$ <sup>(3)</sup>	0.8	2.1	mA
$I_{OZ}$	TRI-STATE Output Leakage Current	$V_{OUT} = V_{CC}$ or GND				$\mu\text{A}$
		ENABLE = $V_{IL}$		$\pm 0.5$	$\pm 5.0$	
		ENABLE = $V_{IH}$				
$I_{SC}$	Output Short Circuit Current	$V_{IN} = V_{CC}$ or GND <sup>(2)(4)</sup>	-30	-150	mA	
$I_{OFF}$	Output Leakage Current Power Off <sup>(2)</sup>	DS26C31T	$V_{OUT} = 6\text{ V}$		100	$\mu\text{A}$
			$V_{CC} = 0\text{ V}$	$V_{OUT} = -0.25\text{ V}$		-100
		DS26C31M	$V_{OUT} = 6\text{ V}$		100	$\mu\text{A}$
			$V_{CC} = 0\text{ V}$	$V_{OUT} = 0\text{ V}$ <sup>(5)</sup>		-100

(1) Unless otherwise specified, min/max limits apply across the recommended operating temperature range. All typicals are given for  $V_{CC} = 5\text{ V}$  and  $T_A = 25^\circ\text{C}$ .

(2) See EIA Specification RS-422 for exact test conditions.

(3) Measured per input. All other inputs at  $V_{CC}$  or GND.

(4) This is the current sourced when a high output is shorted to ground. Only one output at a time should be shorted.

(5) The DS26C31M ( $-55^\circ\text{C}$  to  $+125^\circ\text{C}$ ) is tested with  $V_{OUT}$  between  $+6\text{ V}$  and  $0\text{ V}$  while RS-422A condition is  $+6\text{ V}$  and  $-0.25\text{ V}$ .

## 7.4 Switching Characteristics

 $V_{CC} = 5\text{ V} \pm 10\%$ ,  $t_r \leq 6\text{ ns}$ ,  $t_f \leq 6\text{ ns}$  (Figure 22, Figure 23, Figure 24, Figure 25)<sup>(1)</sup>

PARAMETER	TEST CONDITIONS	MIN	TYP	DS26C31T	DS26C31M	UNIT
				MAX	MAX	
$t_{PLH}$ , $t_{PHL}$	Propagation Delays Input to Output	2	6	11	14	ns
Skew	<sup>(2)</sup>		0.5	2.0	3.0	ns
$t_{TLH}$ , $t_{THL}$	Differential Output Rise And Fall Times		6	10	14	ns
$t_{PZH}$	Output Enable Time		11	19	22	ns
$t_{PZL}$	Output Enable Time		13	21	28	ns
$t_{PHZ}$	Output Disable Time <sup>(3)</sup>		5	9	12	ns
$t_{PLZ}$	Output Disable Time <sup>(3)</sup>		7	11	14	ns
$C_{PD}$	Power Dissipation Capacitance <sup>(4)</sup>		50			pF
$C_{IN}$	Input Capacitance		6			pF

- Unless otherwise specified, min/max limits apply across the recommended operating temperature range. All typicals are given for  $V_{CC} = 5\text{ V}$  and  $T_A = 25^\circ\text{C}$ .
- Skew is defined as the difference in propagation delays between complementary outputs at the 50% point.
- Output disable time is the delay from  $\overline{\text{ENABLE}}$  or  $\overline{\text{ENABLE}}$  being switched to the output transistors turning off. The actual disable times are less than indicated due to the delay added by the RC time constant of the load.
- $C_{PD}$  determines the no load dynamic power consumption,  $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$ , and the no load dynamic current consumption,  $I_S = C_{PD} V_{CC} f + I_{CC}$ .

## 7.5 Comparison Table of Switching Characteristics into “LS-Type” Load

 $V_{CC} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$ ,  $t_r \leq 6\text{ ns}$ ,  $t_f \leq 6\text{ ns}$  (Figure 23, Figure 25, Figure 26, Figure 27)<sup>(1)</sup>

PARAMETER	TEST CONDITIONS	DS26C31T		DS26LS31C		UNIT
		TYP	MAX	TYP	MAX	
$t_{PLH}$ , $t_{PHL}$	Propagation Delays Input to Output $C_L = 30\text{ pF}$ S1 Closed S2 Closed	6	8	10	15	ns
Skew	See <sup>(2)</sup> $C_L = 30\text{ pF}$ S1 Closed S2 Closed	0.5	1.0	2.0	6.0	ns
$t_{THL}$ , $t_{TLH}$	Differential Output Rise and Fall Times $C_L = 30\text{ pF}$ S1 Closed S2 Closed	4	6			ns
$t_{PLZ}$	Output Disable Time <sup>(3)</sup> $C_L = 10\text{ pF}$ S1 Closed S2 Open	6	9	15	35	ns
$t_{PHZ}$	Output Disable Time <sup>(3)</sup> $C_L = 10\text{ pF}$ S1 Open S2 Closed	4	7	15	25	ns
$t_{PZL}$	Output Enable Time $C_L = 30\text{ pF}$ S1 Closed S2 Open	14	20	20	30	ns
$t_{PZH}$	Output Enable Time $C_L = 30\text{ pF}$ S1 Open S2 Closed	11	17	20	30	ns

- This table is provided for comparison purposes only. The values in this table for the DS26C31 reflect the performance of the device but are not tested or verified.
- Skew is defined as the difference in propagation delays between complementary outputs at the 50% point.
- Output disable time is the delay from  $\overline{\text{ENABLE}}$  or  $\overline{\text{ENABLE}}$  being switched to the output transistors turning off. The actual disable times are less than indicated due to the delay added by the RC time constant of the load.

## 7.6 Typical Characteristics

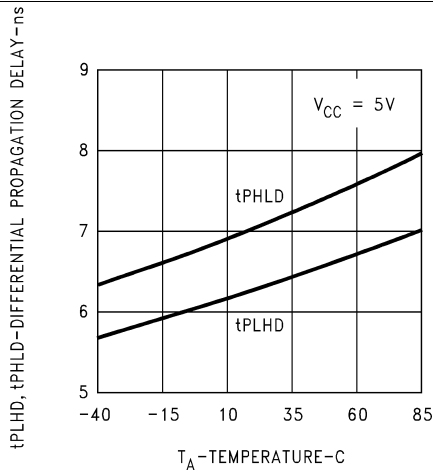


Figure 1. Differential Propagation Delay vs Temperature

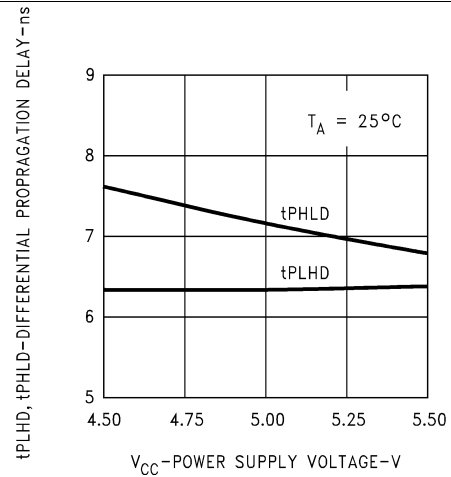


Figure 2. Differential Propagation Delay vs Power Supply Voltage

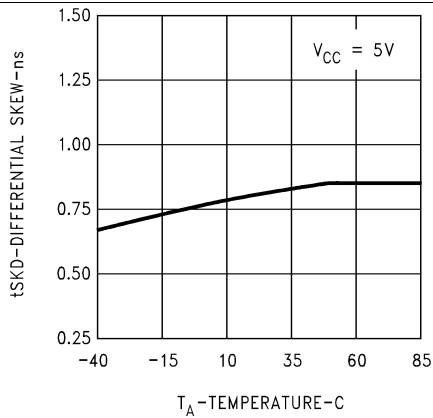


Figure 3. Differential Skew vs Temperature

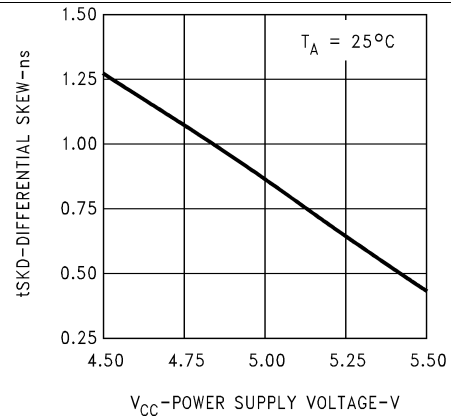


Figure 4. Differential Skew vs Power Supply Voltage

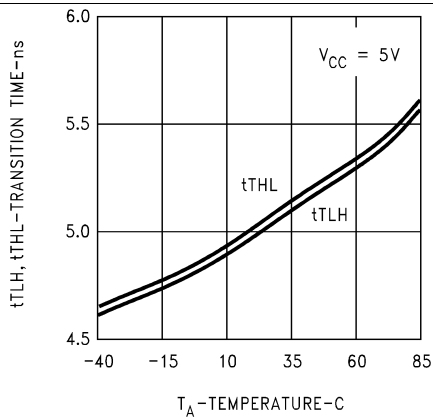


Figure 5. Differential Transition Time vs Temperature

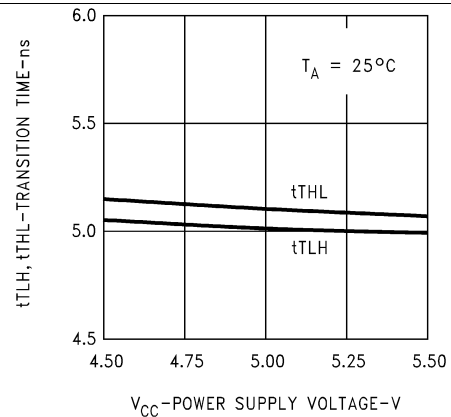


Figure 6. Differential Transition Time vs Power Supply Voltage

Typical Characteristics (continued)

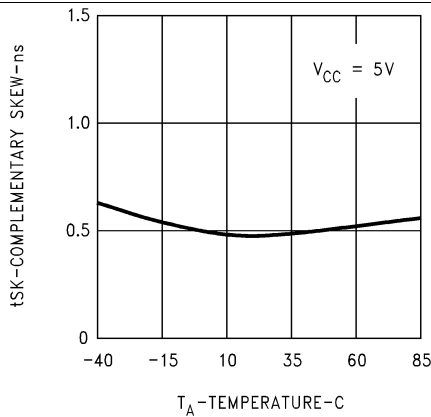


Figure 7. Complementary Skew vs Temperature

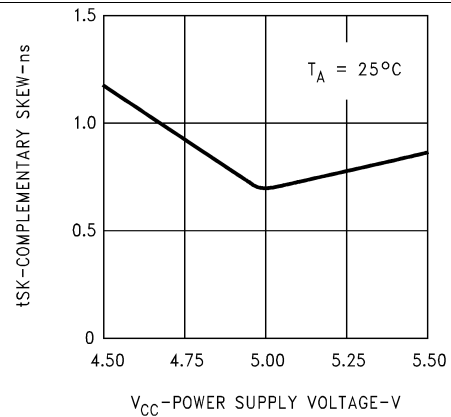


Figure 8. Complementary Skew vs Power Supply Voltage

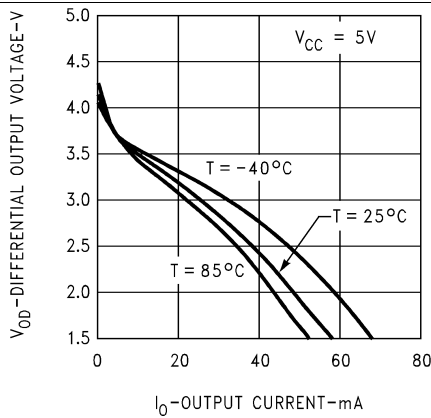


Figure 9. Differential Output Voltage vs Output Current

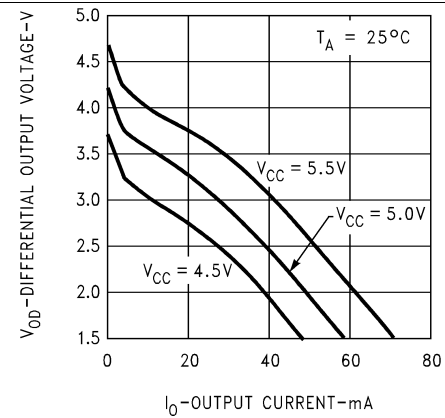


Figure 10. Differential Output Voltage vs Output Current

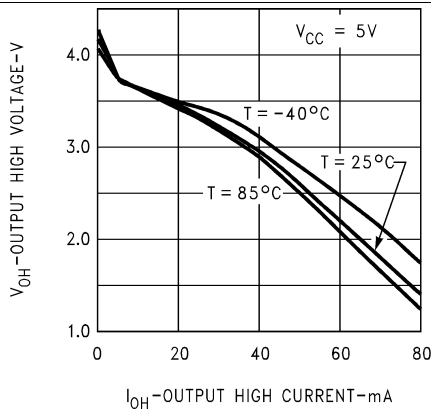


Figure 11. Output High Voltage vs Output High Current

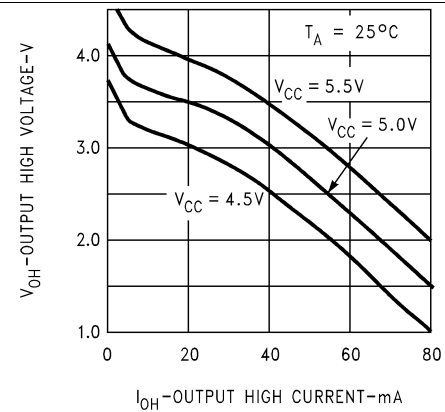


Figure 12. Output High Voltage vs Output High Current



Typical Characteristics (continued)

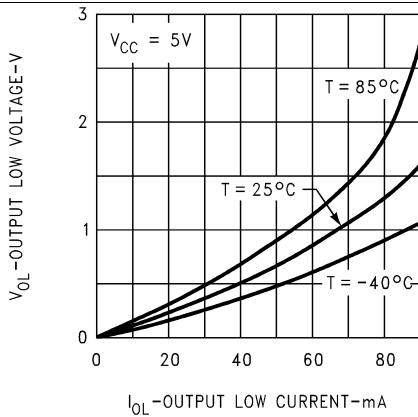


Figure 13. Output Low Voltage vs Output Low Current

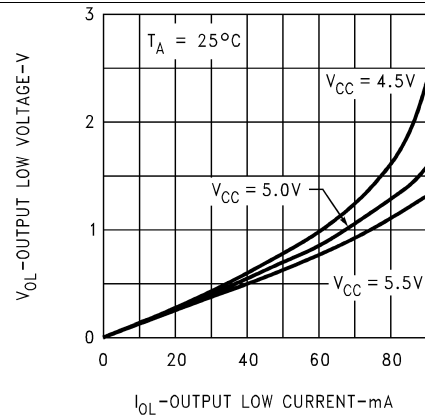


Figure 14. Output Low Voltage vs Output Low Current

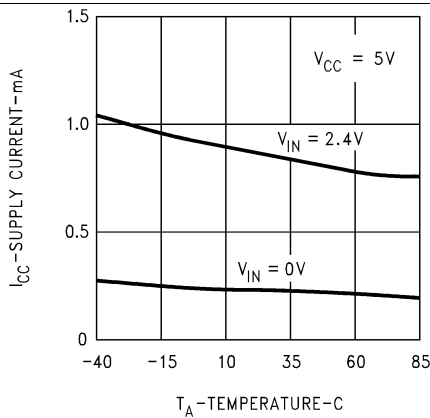


Figure 15. Supply Current vs Temperature

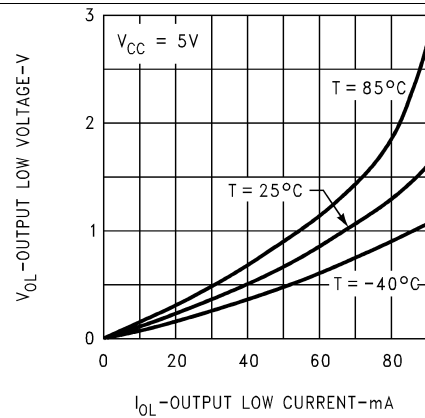


Figure 16. Output Low Voltage vs Output Low Current

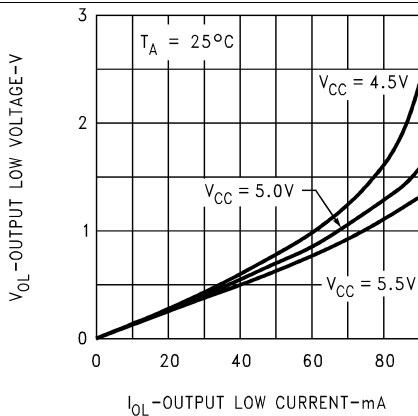


Figure 17. Output Low Voltage vs Output Low Current

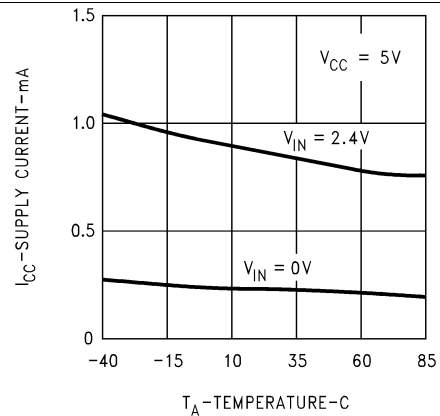
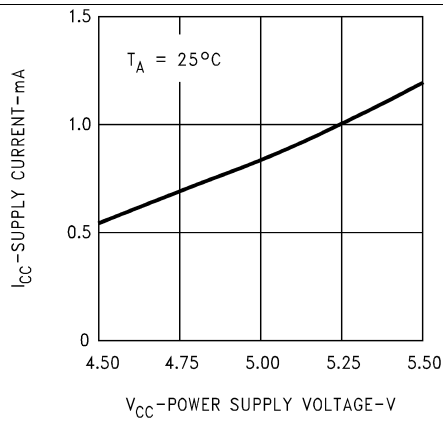
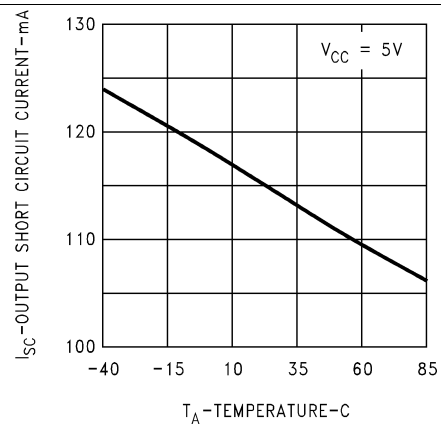


Figure 18. Supply Current vs Temperature

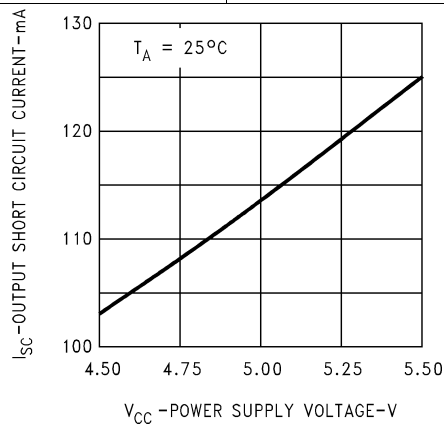
**Typical Characteristics (continued)**



**Figure 19. Supply Current vs Power Supply Voltage**

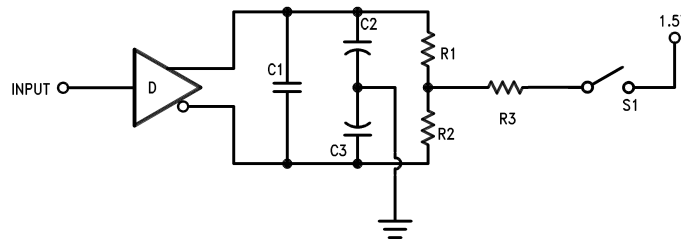


**Figure 20. Output Short Circuit Current vs Temperature**



**Figure 21. Output Short Circuit Current vs Power Supply Voltage**

## 8 Parameter Measurement Information



Note: C1 = C2 = C3 = 40 pF (Including Probe and Jig Capacitance), R1 = R2 = 50Ω, R3 = 500Ω.

Figure 22. AC Test Circuit

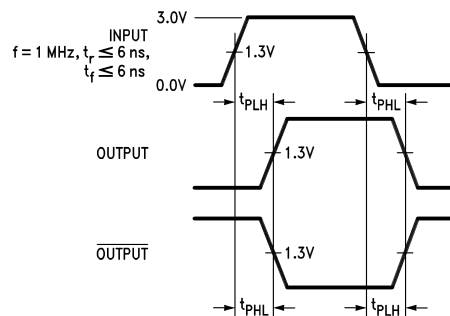


Figure 23. Propagation Delays

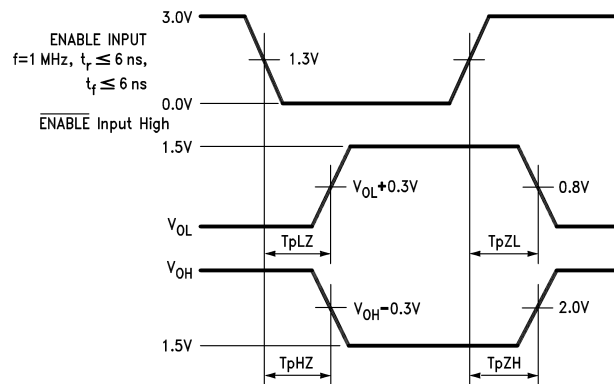
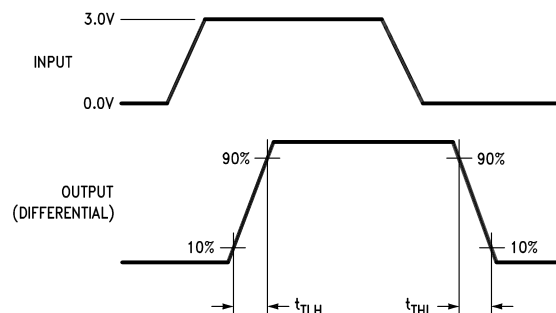
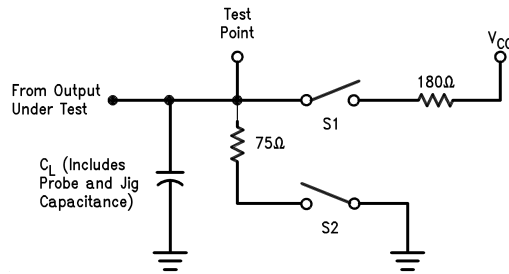
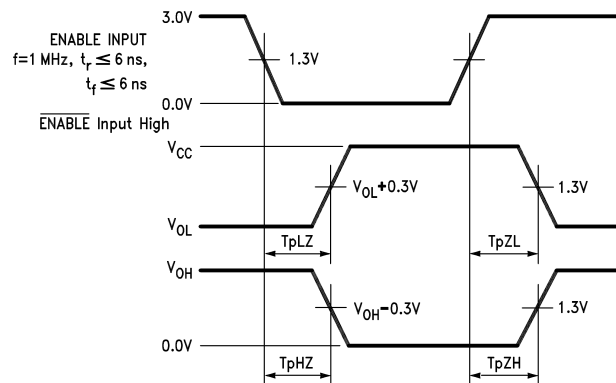


Figure 24. Enable and Disable Times



Input pulse; f = 1 MHz, 50%;  $t_r \leq 6$  ns,  $t_f \leq 6$  ns

Figure 25. Differential Rise and Fall Times

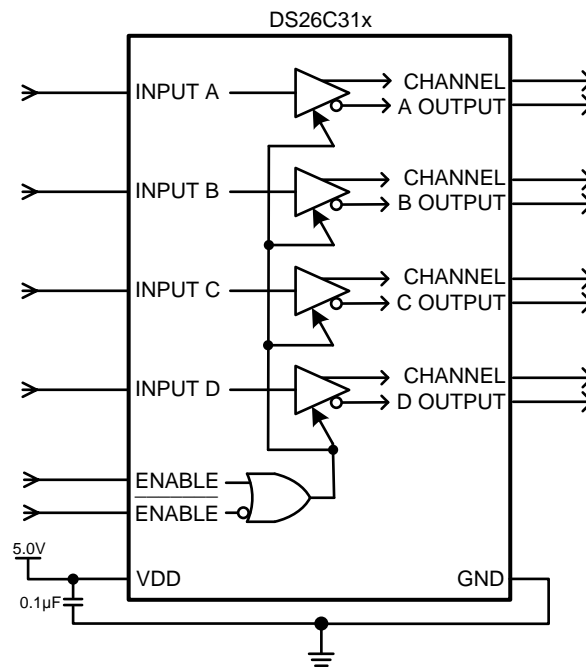
**Parameter Measurement Information (continued)**

**Figure 26. Load AC Test Circuit for “LS-Type” Load**

**Figure 27. Enable and Disable Times for “LS-Type” Load**

## 9 Detailed Description

### 9.1 Overview

The DS26C31 is a quad differential line driver designed for data transmission over balanced cable or printed circuit board traces. The DS26C31M supports a temperature range of -55°C to 125°C, while the DS26C31T supports a temperature range of -40°C to 85°C.

### 9.2 Functional Block Diagram



### 9.3 Feature Description

Each driver converts the TTL or CMOS signal at its input to a pair of complementary differential outputs. The drivers are enabled when the ENABLE control pin is a logic HIGH or when the  $\overline{\text{ENABLE}}$  control pin is a logic LOW.

### 9.4 Device Functional Modes

Table 1. Function Table<sup>(1)</sup>

ENABLE	$\overline{\text{ENABLE}}$	INPUT	NON-INVERTING OUTPUT	INVERTING OUTPUT
L	H	X	Z	Z
All other combinations of enable inputs		L	L	H
		H	H	L

- (1) L = Low logic state  
X = Irrelevant  
H = High logic state  
Z = Tri-state (high impedance)

## 10 Application and Implementation

### NOTE

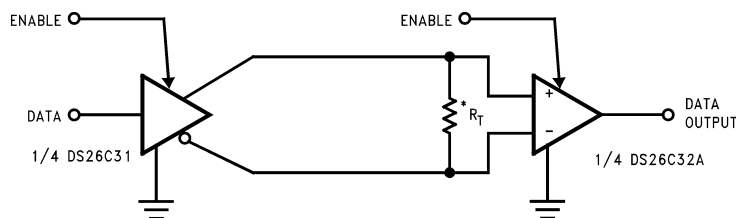
Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

### 10.1 Application Information

The DS26C31 is a quad differential line driver designed for applications that require long distance digital data transmission over balanced cables. The DS26C31 can be used in applications that require conversion from TTL or CMOS input levels to differential signal levels, compatible to RS-422. The use of complimentary signaling in a balanced transmission media provides good immunity in the midst of noisy environments or shifts in ground reference potential.

### 10.2 Typical Application

Figure 28 depicts a typical implementation of the DS26C31x device in a RS-422 application.



\*R<sub>T</sub> is optional although highly recommended to reduce reflection.

**Figure 28. Two-Wire Balanced System, RS-422**

#### 10.2.1 Design Requirements

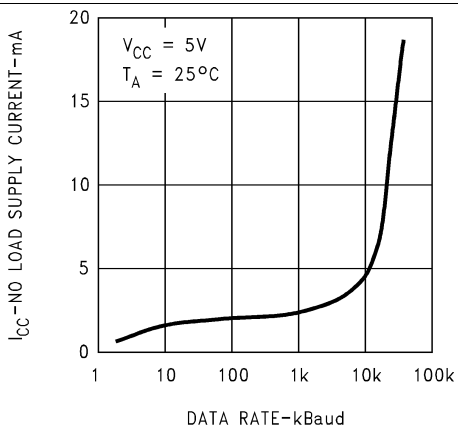
- Apply TTL or LVCMOS signal to driver input lines INPUT A-D.
- Transmit complementary outputs at OUTPUT A-D.
- Use controlled-impedance transmission lines such as printed circuit board traces, twisted-pair wires or parallel wire cable.
- Place a terminating resistor at the far end of the differential pair.

#### 10.2.2 Detailed Design Procedure

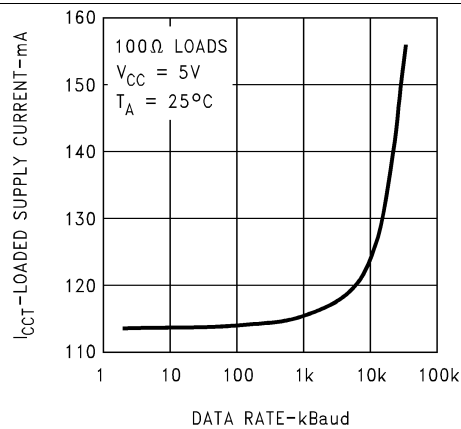
- Connect VCC and GND pins to the power and ground planes of the PCB with a 0.1- $\mu$ F bypass capacitor.
- Use TTL/LVCMOS logic levels at INPUT A-D.
- Use controlled-impedance transmission media for the differential output signals.
- Place an optional terminating resistor at the far-end of the differential pair to avoid reflection.

**Typical Application (continued)**

**10.2.3 Application Curves**



**Figure 29. No Load Supply Current vs Data Rate**



**Figure 30. Loaded Supply Current vs Data Rate**

## 11 Power Supply Recommendations

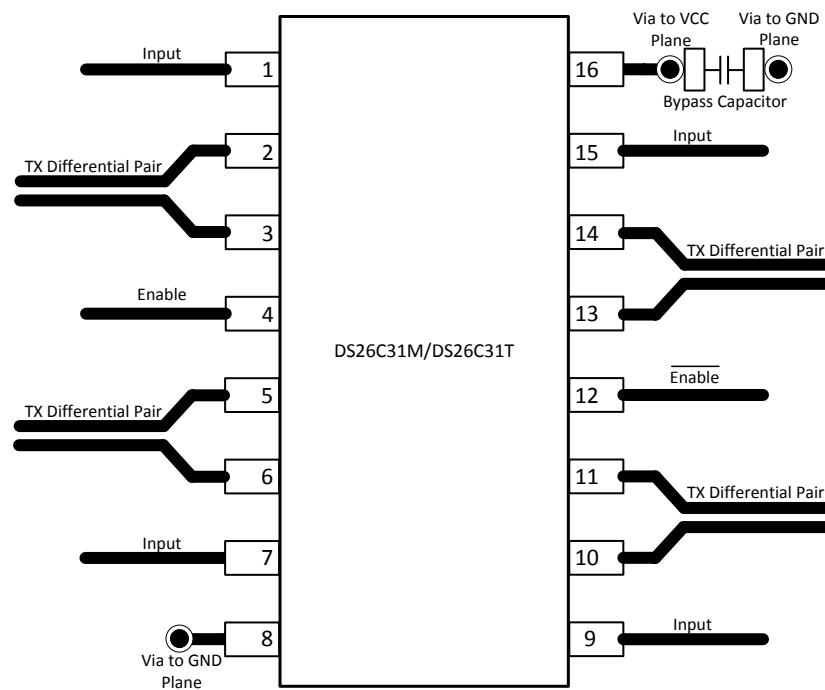
It is recommended that the supply (VCC) and ground (GND) pins be connected to power planes that are placed in the inner layers of the printed circuit board. A 0.1- $\mu$ F bypass capacitor should be connect to the VCC pin such that the capacitor is as close as possible to the device.

## 12 Layout

### 12.1 Layout Guidelines

The output differential signals of the device should be routed on one layer of the board, and clearance should be provided in order to minimize crosstalk between differential pairs that may be running in parallel over a long distance. Additionally, the differential pairs should have a controlled impedance with minimum impedance discontinuities and be terminated at the far-end, near the receiver, with a resistor that is closely matched to the differential pair impedance in order to minimize transmission line reflections. The differential pairs should be routed with uniform trace width and spacing to minimize impedance mismatching.

### 12.2 Layout Example



**Figure 31. DS26C31 Example Layout**



## 13 Device and Documentation Support

### 13.1 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

**Table 2. Related Links**

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
DS26C31M	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>
DS26C31T	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>

### 13.2 Trademarks

All trademarks are the property of their respective owners.

### 13.3 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

### 13.4 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

## 14 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
DS26C31TM	LIFEBUY	SOIC	D	16	48	TBD	Call TI	Call TI	-40 to 85	DS26C31TM	
DS26C31TM/NOPB	ACTIVE	SOIC	D	16	48	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	DS26C31TM	Samples
DS26C31TMX	LIFEBUY	SOIC	D	16	2500	TBD	Call TI	Call TI	-40 to 85	DS26C31TM	
DS26C31TMX/NOPB	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	DS26C31TM	Samples
DS26C31TN	LIFEBUY	PDIP	NFG	16	25	TBD	Call TI	Call TI	-40 to 85	DS26C31TN	
DS26C31TN/NOPB	LIFEBUY	PDIP	NFG	16	25	Green (RoHS & no Sb/Br)	CU SN	Level-1-NA-UNLIM	-40 to 85	DS26C31TN	

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

**Important Information and Disclaimer:** The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

## TAPE AND REEL INFORMATION



### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DS26C31TMX	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.3	8.0	16.0	Q1
DS26C31TMX/NOPB	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.3	8.0	16.0	Q1

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DS26C31TMX	SOIC	D	16	2500	367.0	367.0	35.0
DS26C31TMX/NOPB	SOIC	D	16	2500	367.0	367.0	35.0

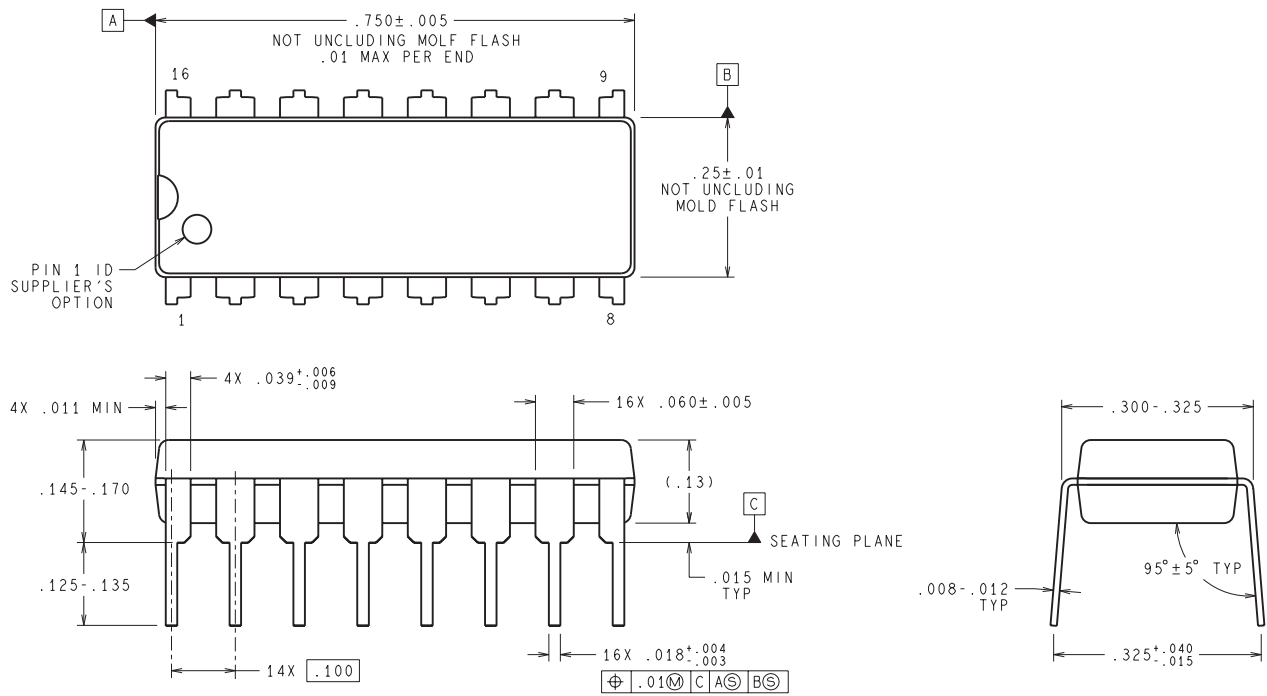
D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
  - D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
  - E. Reference JEDEC MS-012 variation AC.

NFG0016E



**DIMENSIONS ARE IN INCHES**  
 DIMENSIONS IN ( ) FOR REFERENCE ONLY

N16E (Rev G)

## IMPORTANT NOTICE

Texas Instruments Incorporated (TI) reserves the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete.

TI's published terms of sale for semiconductor products (<http://www.ti.com/sc/docs/stdterms.htm>) apply to the sale of packaged integrated circuit products that TI has qualified and released to market. Additional terms may apply to the use or sale of other types of TI products and services.

Reproduction of significant portions of TI information in TI data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such reproduced documentation. Information of third parties may be subject to additional restrictions. Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyers and others who are developing systems that incorporate TI products (collectively, "Designers") understand and agree that Designers remain responsible for using their independent analysis, evaluation and judgment in designing their applications and that Designers have full and exclusive responsibility to assure the safety of Designers' applications and compliance of their applications (and of all TI products used in or for Designers' applications) with all applicable regulations, laws and other applicable requirements. Designer represents that, with respect to their applications, Designer has all the necessary expertise to create and implement safeguards that (1) anticipate dangerous consequences of failures, (2) monitor failures and their consequences, and (3) lessen the likelihood of failures that might cause harm and take appropriate actions. Designer agrees that prior to using or distributing any applications that include TI products, Designer will thoroughly test such applications and the functionality of such TI products as used in such applications.

TI's provision of technical, application or other design advice, quality characterization, reliability data or other services or information, including, but not limited to, reference designs and materials relating to evaluation modules, (collectively, "TI Resources") are intended to assist designers who are developing applications that incorporate TI products; by downloading, accessing or using TI Resources in any way, Designer (individually or, if Designer is acting on behalf of a company, Designer's company) agrees to use any particular TI Resource solely for this purpose and subject to the terms of this Notice.

TI's provision of TI Resources does not expand or otherwise alter TI's applicable published warranties or warranty disclaimers for TI products, and no additional obligations or liabilities arise from TI providing such TI Resources. TI reserves the right to make corrections, enhancements, improvements and other changes to its TI Resources. TI has not conducted any testing other than that specifically described in the published documentation for a particular TI Resource.

Designer is authorized to use, copy and modify any individual TI Resource only in connection with the development of applications that include the TI product(s) identified in such TI Resource. NO OTHER LICENSE, EXPRESS OR IMPLIED, BY ESTOPPEL OR OTHERWISE TO ANY OTHER TI INTELLECTUAL PROPERTY RIGHT, AND NO LICENSE TO ANY TECHNOLOGY OR INTELLECTUAL PROPERTY RIGHT OF TI OR ANY THIRD PARTY IS GRANTED HEREIN, including but not limited to any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information regarding or referencing third-party products or services does not constitute a license to use such products or services, or a warranty or endorsement thereof. Use of TI Resources may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

TI RESOURCES ARE PROVIDED "AS IS" AND WITH ALL FAULTS. TI DISCLAIMS ALL OTHER WARRANTIES OR REPRESENTATIONS, EXPRESS OR IMPLIED, REGARDING RESOURCES OR USE THEREOF, INCLUDING BUT NOT LIMITED TO ACCURACY OR COMPLETENESS, TITLE, ANY EPIDEMIC FAILURE WARRANTY AND ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, AND NON-INFRINGEMENT OF ANY THIRD PARTY INTELLECTUAL PROPERTY RIGHTS. TI SHALL NOT BE LIABLE FOR AND SHALL NOT DEFEND OR INDEMNIFY DESIGNER AGAINST ANY CLAIM, INCLUDING BUT NOT LIMITED TO ANY INFRINGEMENT CLAIM THAT RELATES TO OR IS BASED ON ANY COMBINATION OF PRODUCTS EVEN IF DESCRIBED IN TI RESOURCES OR OTHERWISE. IN NO EVENT SHALL TI BE LIABLE FOR ANY ACTUAL, DIRECT, SPECIAL, COLLATERAL, INDIRECT, PUNITIVE, INCIDENTAL, CONSEQUENTIAL OR EXEMPLARY DAMAGES IN CONNECTION WITH OR ARISING OUT OF TI RESOURCES OR USE THEREOF, AND REGARDLESS OF WHETHER TI HAS BEEN ADVISED OF THE POSSIBILITY OF SUCH DAMAGES.

Unless TI has explicitly designated an individual product as meeting the requirements of a particular industry standard (e.g., ISO/TS 16949 and ISO 26262), TI is not responsible for any failure to meet such industry standard requirements.

Where TI specifically promotes products as facilitating functional safety or as compliant with industry functional safety standards, such products are intended to help enable customers to design and create their own applications that meet applicable functional safety standards and requirements. Using products in an application does not by itself establish any safety features in the application. Designers must ensure compliance with safety-related requirements and standards applicable to their applications. Designer may not use any TI products in life-critical medical equipment unless authorized officers of the parties have executed a special contract specifically governing such use. Life-critical medical equipment is medical equipment where failure of such equipment would cause serious bodily injury or death (e.g., life support, pacemakers, defibrillators, heart pumps, neurostimulators, and implantables). Such equipment includes, without limitation, all medical devices identified by the U.S. Food and Drug Administration as Class III devices and equivalent classifications outside the U.S.

TI may expressly designate certain products as completing a particular qualification (e.g., Q100, Military Grade, or Enhanced Product). Designers agree that it has the necessary expertise to select the product with the appropriate qualification designation for their applications and that proper product selection is at Designers' own risk. Designers are solely responsible for compliance with all legal and regulatory requirements in connection with such selection.

Designer will fully indemnify TI and its representatives against any damages, costs, losses, and/or liabilities arising out of Designer's non-compliance with the terms and provisions of this Notice.