

## 1.5 A Low-Dropout Linear Regulator with Programmable Soft-Start

Check for Samples: [TPS74801-Q1](#)

### FEATURES

- Qualified for Automotive Applications
- AEC-Q100 Qualified with the Following Results:
  - Device Temperature Grade 1:  $-40^{\circ}\text{C}$  to  $125^{\circ}\text{C}$  Ambient Operating Temperature Range
  - Device HBM ESD Classification Level H2
  - Device HBM ESD Classification Level C4B
- $V_{\text{OUT}}$  Range: 0.8 V to 3.6 V
- Ultralow  $V_{\text{IN}}$  Range: 0.8 V to 5.5 V
- $V_{\text{BIAS}}$  Range 2.7 V to 5.5 V
- Low Dropout: 60 mV typ at 1.5 A,  $V_{\text{BIAS}} = 5$  V
- Power Good (PG) Output Allows Supply Monitoring or Provides a Sequencing Signal for Other Supplies
- 2% Accuracy Over Line/Load/Temperature
- Programmable Soft-Start Provides Linear Voltage Startup
- $V_{\text{BIAS}}$  Permits Low  $V_{\text{IN}}$  Operation with Good Transient Response
- Stable with Any Output Capacitor  $\geq 2.2 \mu\text{F}$
- Available in a Small 3-mm x 3-mm x 1-mm SON-10 and 5 x 5 QFN-20 Packages

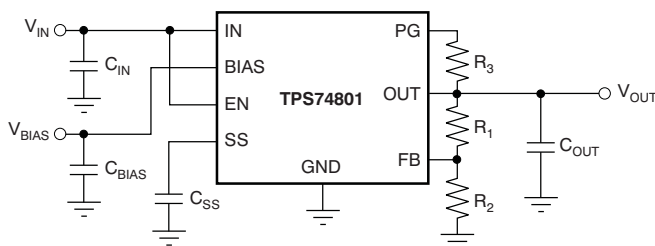
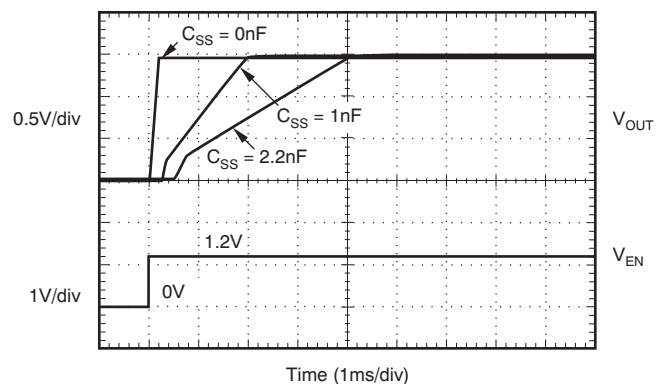
### APPLICATIONS

- FPGA Applications
- DSP Core and I/O Voltages
- Post-Regulation Applications
- Applications with Special Start-Up Time or Sequencing Requirements
- Hot-Swap and Inrush Controls

### DESCRIPTION

The TPS74801-Q1 low-dropout (LDO) linear regulator provides an easy-to-use robust power management solution for a wide variety of applications. User-programmable soft-start minimizes stress on the input power source by reducing capacitive inrush current on start-up. The soft-start is monotonic and well-suited for powering many different types of processors and ASICs. The enable input and power good output allow easy sequencing with external regulators. This complete flexibility permits the user to configure a solution that meets the sequencing requirements of FPGAs, DSPs, and other applications with special start-up requirements.

A precision reference and error amplifier deliver 2% accuracy over load, line, temperature, and process. The device is stable with any type of capacitor greater than or equal to  $2.2 \mu\text{F}$ , and is fully specified from  $-40^{\circ}\text{C}$  to  $105^{\circ}\text{C}$  for the DRC package, and from  $-40^{\circ}\text{C}$  to  $125^{\circ}\text{C}$  for the RGW package. The TPS74801-Q1 is offered in a small 3-mm x 3-mm SON-10 package, yielding a highly compact, total solution size. It is also available in a 5 x 5 QFN-20 for compatibility with the TPS74401.


**Figure 1. Typical Application Circuit (Adjustable)**

**Figure 2. Turn-On Response**


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This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## ABSOLUTE MAXIMUM RATINGS<sup>(1)</sup>

At  $T_A = -40^\circ\text{C}$  to  $105^\circ\text{C}$  (for TPS74801TDRCRQ1),  $T_A = -40^\circ\text{C}$  to  $125^\circ\text{C}$  (for TPS74801QRGWRQ1), unless otherwise noted. All voltages are with respect to GND.

		TPS74801-Q1	UNIT
$V_{IN}, V_{BIAS}$	Input voltage range	-0.3 to 6	V
$V_{EN}$	Enable voltage range	-0.3 to 6	V
$V_{PG}$	Power good voltage range	-0.3 to 6	V
$I_{PG}$	PG sink current	0 to 1.5	mA
$V_{SS}$	Soft-start voltage range	-0.3 to 6	V
$V_{FB}$	Feedback voltage range	-0.3 to 6	V
$V_{OUT}$	Output voltage range	-0.3 to $V_{IN} + 0.3$	V
$I_{OUT}$	Maximum output current	Internally limited	
	Output short-circuit duration	Indefinite	
$P_{DISS}$	Continuous total power dissipation	See <a href="#">Thermal Information</a> Table	
$T_J$	Operating junction temperature range	-40 to 150	$^\circ\text{C}$
$T_{STG}$	Storage junction temperature range	-55 to 150	$^\circ\text{C}$
Electrostatic Discharge (ESD) Ratings	Human body model (HBM) classification level H2	2000	V
	Charged device model (CDM) classification level C4B	750	V

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

## THERMAL INFORMATION

THERMAL METRIC <sup>(1)</sup>		TPS74801-Q1 <sup>(2)</sup>		UNIT
		RGW	DRC	
		20 PINS	10 PINS	
$\theta_{JA}$	Junction-to-ambient thermal resistance <sup>(3)</sup>	35.6	41.5	°C/W
$\theta_{JcTop}$	Junction-to-case (top) thermal resistance <sup>(4)</sup>	33.3	78	
$\theta_{JB}$	Junction-to-board thermal resistance <sup>(5)</sup>	15	N/A	
$\psi_{JT}$	Junction-to-top characterization parameter <sup>(6)</sup>	0.4	0.7	
$\psi_{JB}$	Junction-to-board characterization parameter <sup>(7)</sup>	15.2	11.3	
$\theta_{JcBot}$	Junction-to-case (bottom) thermal resistance <sup>(8)</sup>	3.8	6.6	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, [SPRA953A](#).

(2) Thermal data for the RGW and DRC packages are derived by thermal simulations based on JEDEC-standard methodology as specified in the JESD51 series. The following assumptions are used in the simulations:

(a) i. RGW: The exposed pad is connected to the PCB ground layer through a 4x4 thermal via array.

ii. DRC: The exposed pad is connected to the PCB ground layer through a 3x2 thermal via array.

(b) i. RGW: Each of top and bottom copper layers has a dedicated pattern for 20% copper coverage.

ii. DRC: The top and bottom copper layers are assumed to have a 20% thermal conductivity of copper representing a 20% copper coverage.

(c) This data was generated with only a single device at the center of a JEDEC high-K (2s2p) board with 3-in × 3-in copper area. To understand the effects of the copper area on thermal performance, see the [Power Dissipation](#) and [Estimating Junction Temperature](#) sections of this data sheet.

(3) The junction-to-ambient thermal resistance under natural convection is obtained in a simulation on a JEDEC-standard, high-K board, as specified in JESD51-7, in an environment described in JESD51-2a.

(4) The junction-to-case (top) thermal resistance is obtained by simulating a cold plate test on the top of the package. No specific JEDEC standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.

(5) The junction-to-board thermal resistance is obtained by simulating in an environment with a ring cold plate fixture to control the PCB temperature, as described in JESD51-8.

(6) The junction-to-top characterization parameter,  $\psi_{JT}$ , estimates the junction temperature of a device in a real system and is extracted from the simulation data to obtain  $\theta_{JA}$  using a procedure described in JESD51-2a (sections 6 and 7).

(7) The junction-to-board characterization parameter,  $\psi_{JB}$ , estimates the junction temperature of a device in a real system and is extracted from the simulation data to obtain  $\theta_{JA}$  using a procedure described in JESD51-2a (sections 6 and 7).

(8) The junction-to-case (bottom) thermal resistance is obtained by simulating a cold plate test on the exposed (power) pad. No specific JEDEC standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.

## ELECTRICAL CHARACTERISTICS

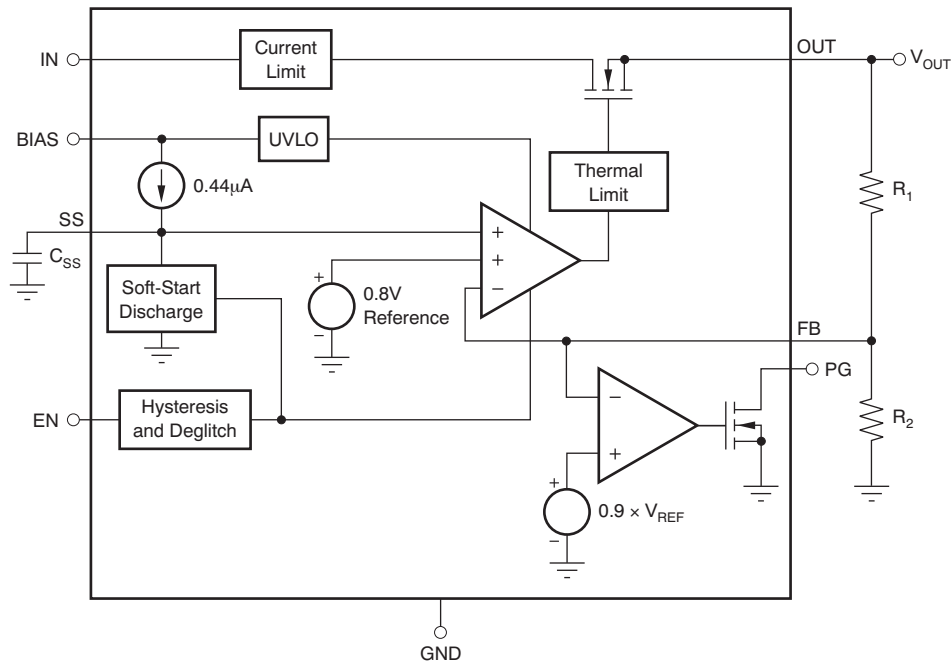
At  $V_{EN} = 1.1\text{ V}$ ,  $V_{IN} = V_{OUT} + 0.3\text{ V}$ ,  $C_{BIAS} = 0.1\text{ }\mu\text{F}$ ,  $C_{IN} = C_{OUT} = 10\text{ }\mu\text{F}$ ,  $C_{NR} = 1\text{ nF}$ ,  $I_{OUT} = 50\text{ mA}$ ,  $V_{BIAS} = 5\text{ V}$ ,  $T_A = -40^\circ\text{C}$  to  $105^\circ\text{C}$  (DRC) and  $T_A = -40^\circ\text{C}$  to  $125^\circ\text{C}$  (RGW), unless otherwise noted. Typical values are at  $T_A = 25^\circ\text{C}$ .

PARAMETER	TEST CONDITIONS	TPS74801-Q1			UNIT
		MIN	TYP	MAX	
$V_{IN}$	Input voltage range	$V_{OUT} + V_{DO}$			V
$V_{BIAS}$	Bias pin voltage range	2.7		5.5	V
$V_{REF}$	Internal reference (Adj.)	$T_A = 25^\circ\text{C}$			V
$V_{OUT}$	Output voltage range	$V_{IN} = 5\text{ V}$ , $I_{OUT} = 1.5\text{ A}$			V
	Accuracy <sup>(1)</sup>	$2.97\text{ V} \leq V_{BIAS} \leq 5.5\text{ V}$ , $50\text{ mA} \leq I_{OUT} \leq 1.5\text{ A}$			%
$V_{OUT}/V_{IN}$	Line regulation	$V_{OUT(NOM)} + 0.3 \leq V_{IN} \leq 5.5\text{ V}$			%/V
$V_{OUT}/I_{OUT}$	Load regulation	$50\text{ mA} \leq I_{OUT} \leq 1.5\text{ A}$			%/A
$V_{DO}$	$V_{IN}$ dropout voltage <sup>(2)</sup>	$I_{OUT} = 1.5\text{ A}$ , $V_{BIAS} - V_{OUT(NOM)} \geq 3.25\text{ V}^{(3)}$			mV
	$V_{BIAS}$ dropout voltage <sup>(2)</sup>	$I_{OUT} = 1.5\text{ A}$ , $V_{IN} = V_{BIAS}$			V
$I_{CL}$	Current limit	$V_{OUT} = 80\% \times V_{OUT(NOM)}$			A
$I_{BIAS}$	Bias pin current		1	2	mA
$I_{SHDN}$	Shutdown supply current ( $I_{GND}$ )	$V_{EN} \leq 0.4\text{ V}$			$\mu\text{A}$
$I_{FB}$	Feedback pin current	-1	0.150	1	$\mu\text{A}$
PSRR	Power-supply rejection ( $V_{IN}$ to $V_{OUT}$ )	1 kHz, $I_{OUT} = 1.5\text{ A}$ , $V_{IN} = 1.8\text{ V}$ , $V_{OUT} = 1.5\text{ V}$			dB
		300 kHz, $I_{OUT} = 1.5\text{ A}$ , $V_{IN} = 1.8\text{ V}$ , $V_{OUT} = 1.5\text{ V}$			
	Power-supply rejection ( $V_{BIAS}$ to $V_{OUT}$ )	1 kHz, $I_{OUT} = 1.5\text{ A}$ , $V_{IN} = 1.8\text{ V}$ , $V_{OUT} = 1.5\text{ V}$			dB
		300 kHz, $I_{OUT} = 1.5\text{ A}$ , $V_{IN} = 1.8\text{ V}$ , $V_{OUT} = 1.5\text{ V}$			
Noise	Output noise voltage	100 Hz to 100 kHz, $I_{OUT} = 1.5\text{ A}$ , $C_{SS} = 0.001\text{ }\mu\text{F}$			$\mu\text{V}_{RMS}$
$t_{STR}$	Minimum startup time	$R_{LOAD}$ for $I_{OUT} = 1\text{ A}$ , $C_{SS} = \text{open}$			$\mu\text{s}$
$I_{SS}$	Soft-start charging current	$V_{SS} = 0.4\text{ V}$			nA
$V_{EN, HI}$	Enable input high level	1.1		5.5	V
$V_{EN, LO}$	Enable input low level	0		0.4	V
$V_{EN, HYS}$	Enable pin hysteresis		50		mV
$V_{EN, DG}$	Enable pin deglitch time		20		$\mu\text{s}$
$I_{EN}$	Enable pin current	$V_{EN} = 5\text{ V}$			$\mu\text{A}$
$V_{IT}$	PG trip threshold	$V_{OUT}$ decreasing			% $V_{OUT}$
$V_{HYS}$	PG trip hysteresis		3		% $V_{OUT}$
$V_{PG, LO}$	PG output low voltage	$I_{PG} = 1\text{ mA}$ (sinking), $V_{OUT} < V_{IT}$			V
$I_{PG, LKG}$	PG leakage current	$V_{PG} = 5.25\text{ V}$ , $V_{OUT} > V_{IT}$			$\mu\text{A}$
$T_{SD}$	Thermal shutdown temperature	Shutdown, temperature increasing			$^\circ\text{C}$
		Reset, temperature decreasing			

(1) Adjustable devices tested at 0.8 V; resistor tolerance is not taken into account.

(2) Dropout is defined as the voltage from  $V_{IN}$  to  $V_{OUT}$  when  $V_{OUT}$  is 3% below nominal.

(3) 3.25 V is a test condition of this device and can be adjusted by referring to [Figure 8](#).

**BLOCK DIAGRAM**

**Table 1. Standard 1% Resistor Values for Programming the Output Voltage<sup>(1)</sup>**

R <sub>1</sub> (kΩ)	R <sub>2</sub> (kΩ)	V <sub>OUT</sub> (V)
Short	Open	0.8
0.619	4.99	0.9
1.13	4.53	1
1.37	4.42	1.05
1.87	4.99	1.1
2.49	4.99	1.2
4.12	4.75	1.5
3.57	2.87	1.8
3.57	1.69	2.5
3.57	1.15	3.3

$$(1) V_{OUT} = 0.8 \times (1 + R_1 / R_2).$$

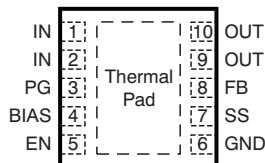
**Table 2. Standard Capacitor Values for Programming the Soft-Start Time<sup>(1)</sup>**

C <sub>SS</sub>	SOFT-START TIME
Open	0.1 ms
270 pF	0.5 ms
560 pF	1 ms
2.7 nF	5 ms
5.6 nF	10 ms
0.01 µF	18 ms

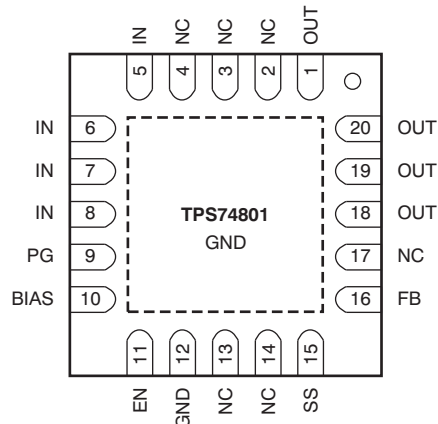
$$(1) t_{SS}(s) = 0.8 \times C_{SS}(F) / 4.4 \times 10^{-7}.$$

**DEVICE INFORMATION**

**DRC PACKAGE**  
3-mm x 3-mm SON  
(TOP VIEW)



**RGW PACKAGE**  
5 x 5 QFN  
(TOP VIEW)

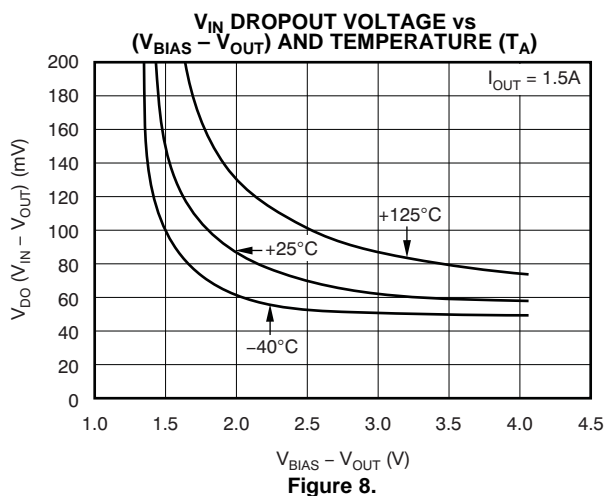
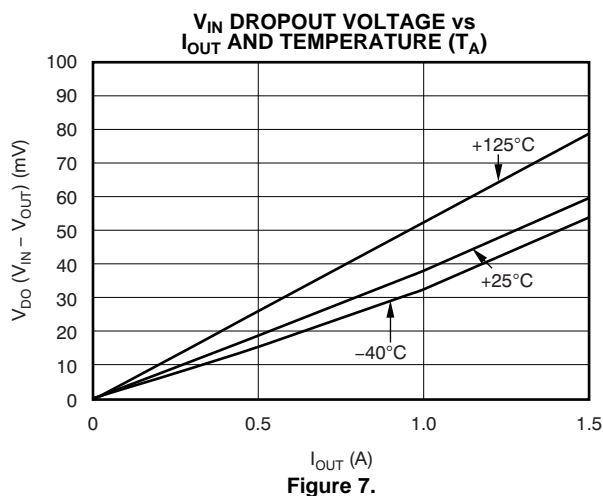
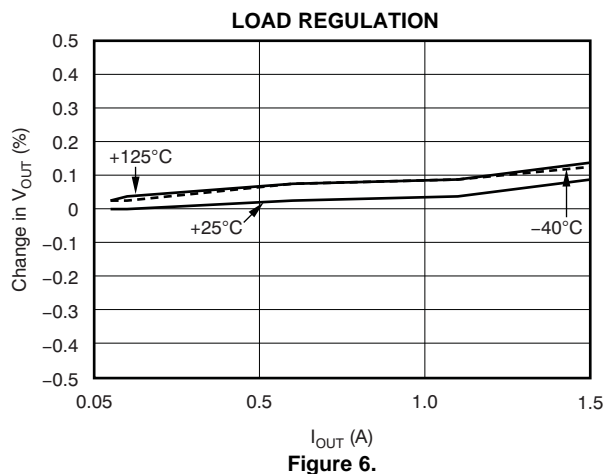
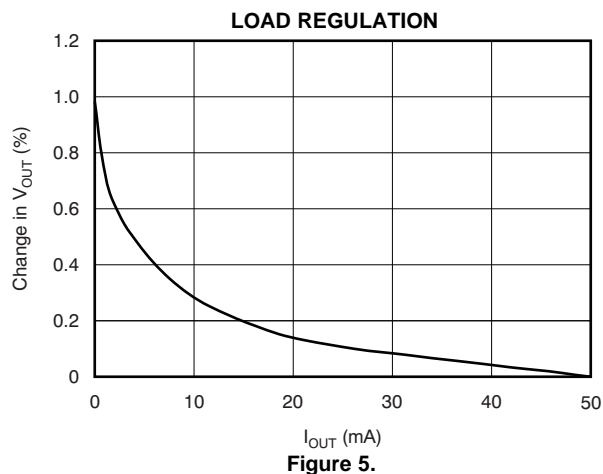
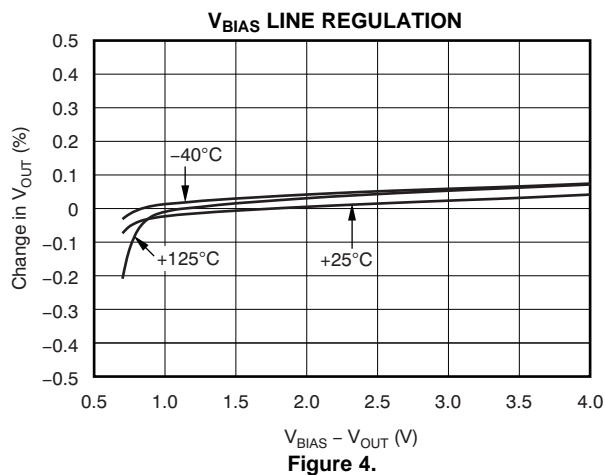
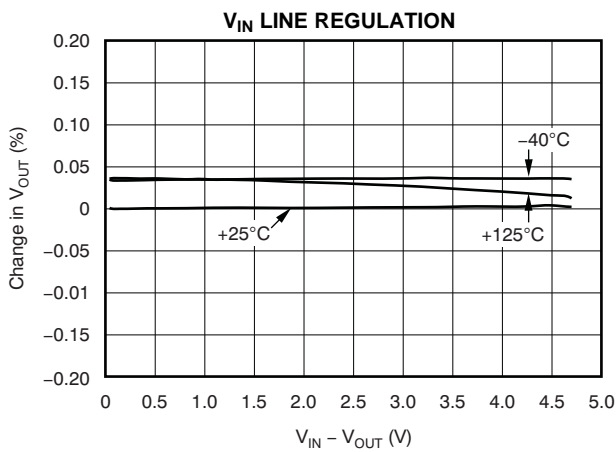


**PIN DESCRIPTIONS**

NAME	DRC (SON)	RGW (QFN)	DESCRIPTION
IN	1, 2	5-8	Input to the device.
EN	5	11	Enable pin. Driving this pin high enables the regulator. Driving this pin low puts the regulator into shutdown mode. This pin must not be left unconnected.
SS	7	15	Soft-Start pin. A capacitor connected on this pin to ground sets the start-up time. If this pin is left unconnected, the regulator output soft-start ramp time is typically 200 $\mu$ s.
BIAS	4	10	Bias input voltage for error amplifier, reference, and internal control circuits.
PG	3	9	Power Good pin. An open-drain, active-high output that indicates the status of $V_{OUT}$ . When $V_{OUT}$ exceeds the PG trip threshold, the PG pin goes into a high-impedance state. When $V_{OUT}$ is below this threshold the pin is driven to a low-impedance state. A pull-up resistor from 10 k $\Omega$ to 1 M $\Omega$ should be connected from this pin to a supply of up to 5.5 V. The supply can be higher than the input voltage. Alternatively, the PG pin can be left unconnected if output monitoring is not necessary.
FB	8	16	Feedback pin. The feedback connection to the center tap of an external resistor divider network that sets the output voltage. This pin must not be left floating.
OUT	9, 10	1, 18-20	Regulated output voltage. A small capacitor (total typical capacitance $\geq$ 2.2 $\mu$ F, ceramic) is needed from this pin to ground to assure stability.
NC	N/A	2-4, 13, 14, 17	No connection. This pin can be left floating or connected to GND to allow better thermal contact to the top-side plane.
GND	6	12	Ground
Thermal Pad	—		Should be soldered to the ground plane for increased thermal performance.

### TYPICAL CHARACTERISTICS

At  $T_A = 25^\circ\text{C}$ ,  $V_{IN} = V_{OUT(TYP)} + 0.3\text{ V}$ ,  $V_{BIAS} = 5\text{ V}$ ,  $I_{OUT} = 50\text{ mA}$ ,  $V_{EN} = V_{IN}$ ,  $C_{IN} = 1\text{ }\mu\text{F}$ ,  $C_{BIAS} = 4.7\text{ }\mu\text{F}$ , and  $C_{OUT} = 10\text{ }\mu\text{F}$ , unless otherwise noted.



**TYPICAL CHARACTERISTICS (continued)**

At  $T_A = 25^\circ\text{C}$ ,  $V_{IN} = V_{OUT(TYP)} + 0.3\text{ V}$ ,  $V_{BIAS} = 5\text{ V}$ ,  $I_{OUT} = 50\text{ mA}$ ,  $V_{EN} = V_{IN}$ ,  $C_{IN} = 1\ \mu\text{F}$ ,  $C_{BIAS} = 4.7\ \mu\text{F}$ , and  $C_{OUT} = 10\ \mu\text{F}$ , unless otherwise noted.

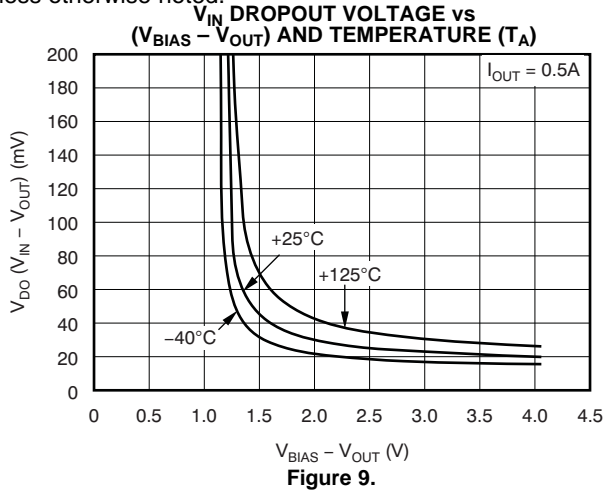


Figure 9.

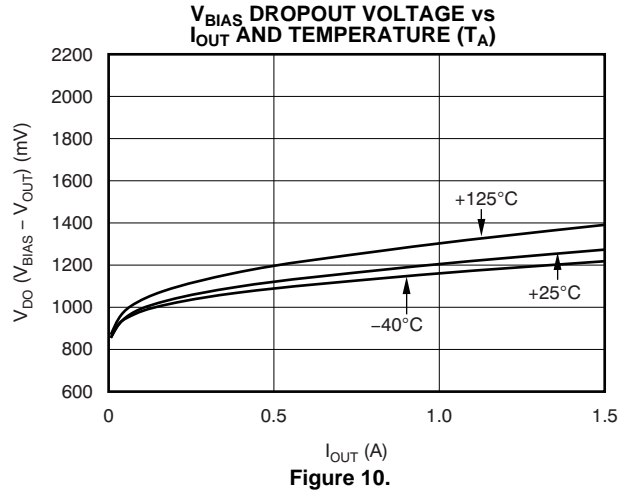


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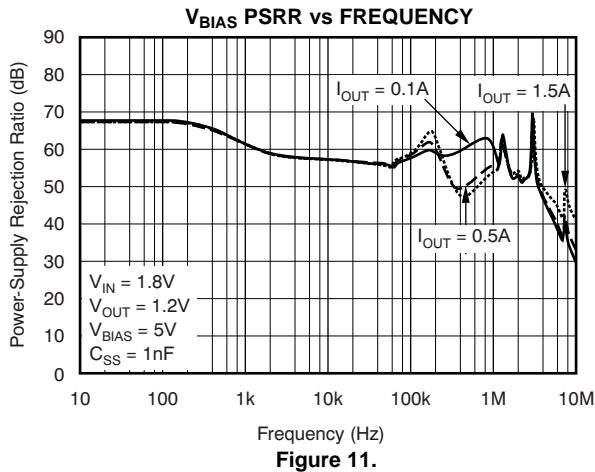


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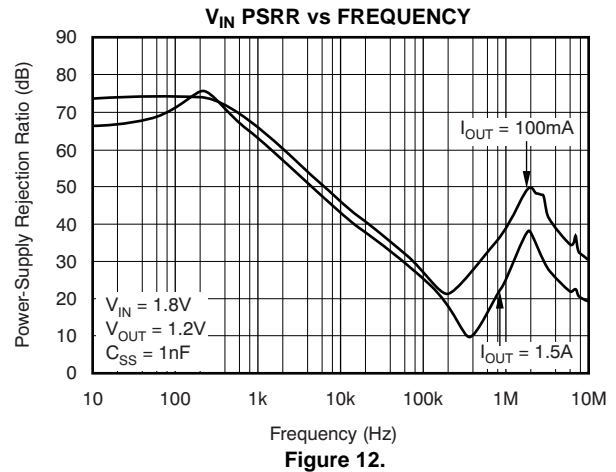


Figure 12.

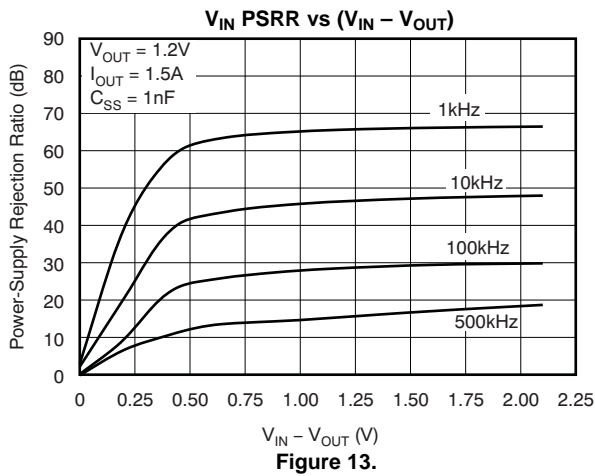


Figure 13.

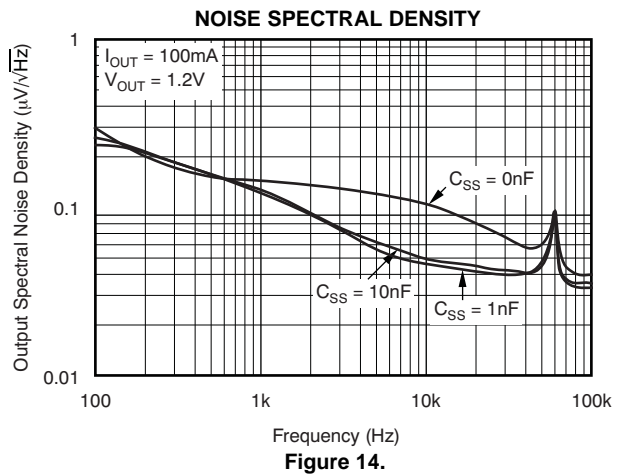


Figure 14.



**TYPICAL CHARACTERISTICS (continued)**

At  $T_A = 25^\circ\text{C}$ ,  $V_{IN} = V_{OUT(TYP)} + 0.3\text{ V}$ ,  $V_{BIAS} = 5\text{ V}$ ,  $I_{OUT} = 50\text{ mA}$ ,  $V_{EN} = V_{IN}$ ,  $C_{IN} = 1\text{ }\mu\text{F}$ ,  $C_{BIAS} = 4.7\text{ }\mu\text{F}$ , and  $C_{OUT} = 10\text{ }\mu\text{F}$ , unless otherwise noted.

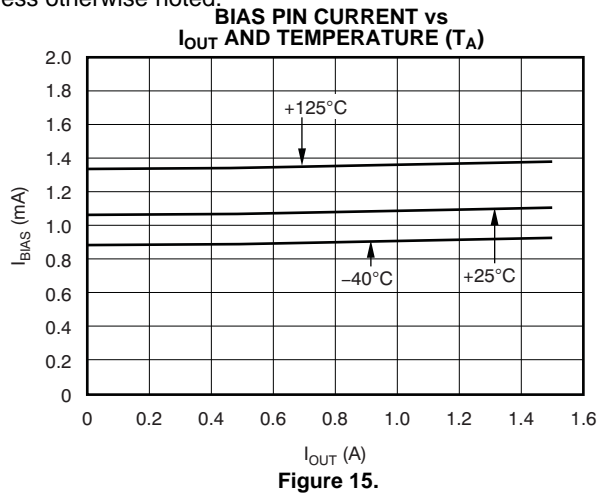


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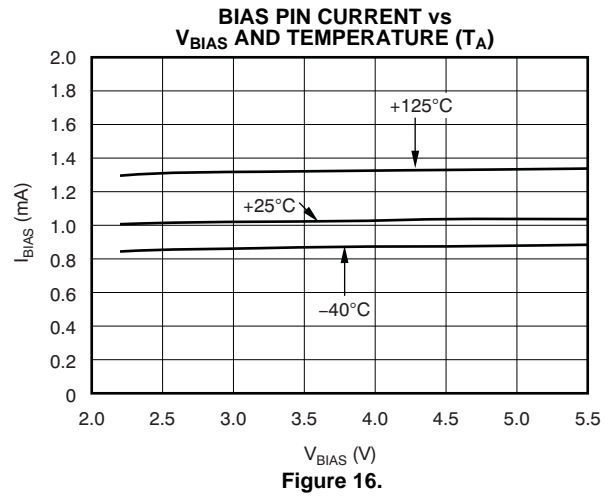


Figure 16.

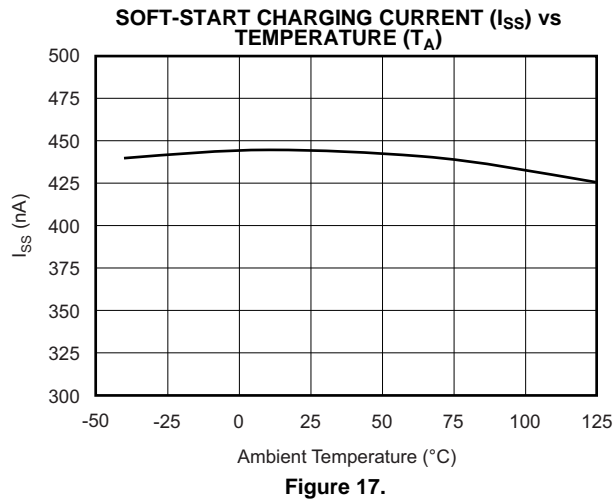


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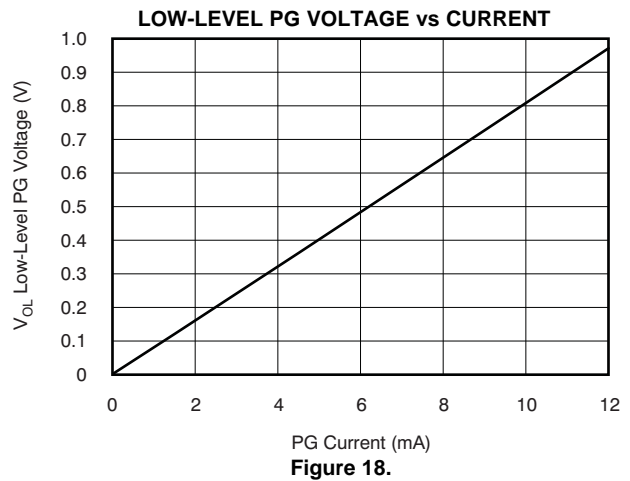


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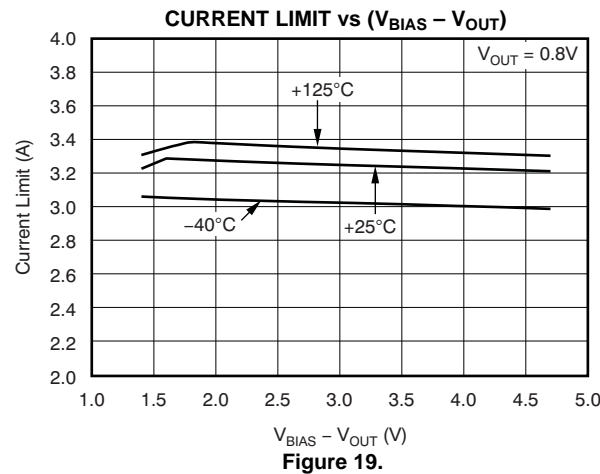


Figure 19.

**TYPICAL CHARACTERISTICS**

At  $T_A = 25^\circ\text{C}$ ,  $V_{IN} = V_{OUT(TYP)} + 0.3\text{ V}$ ,  $V_{BIAS} = 5\text{ V}$ ,  $I_{OUT} = 1\text{ A}$ ,  $V_{EN} = V_{IN} = 1.8\text{ V}$ ,  $V_{OUT} = 1.5\text{ V}$ ,  $C_{IN} = 1\text{ }\mu\text{F}$ ,  $C_{BIAS} = 4.7\text{ }\mu\text{F}$ , and  $C_{OUT} = 10\text{ }\mu\text{F}$ , unless otherwise noted.

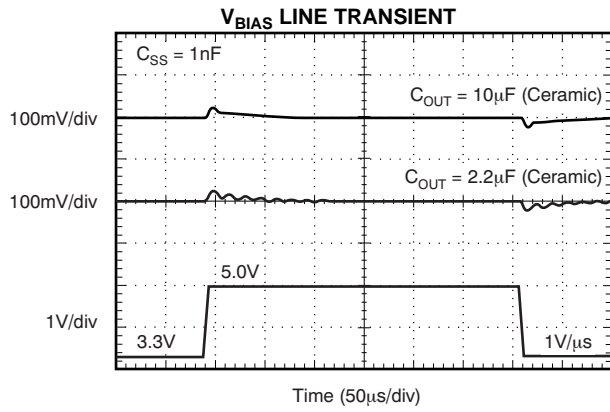


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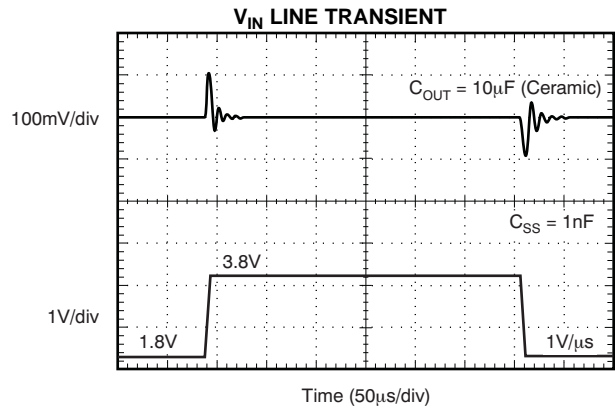


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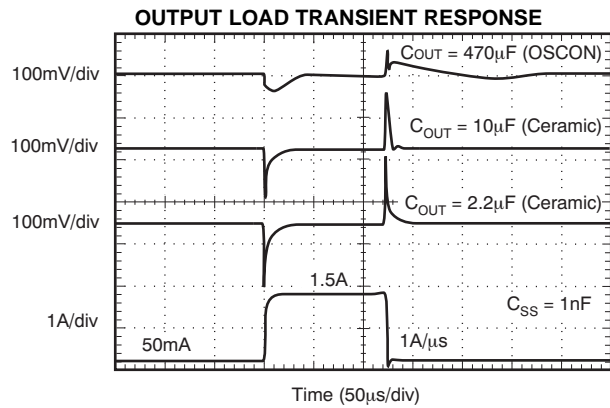


Figure 22.

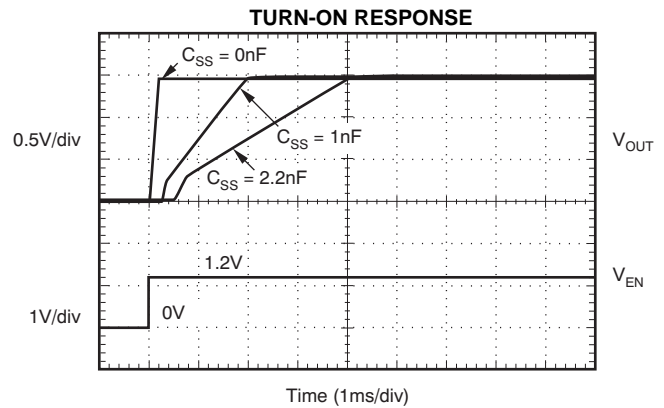


Figure 23.

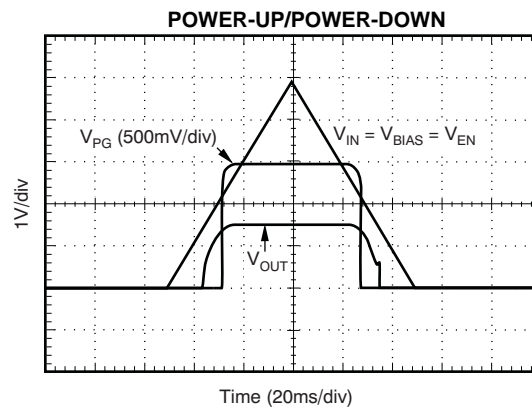


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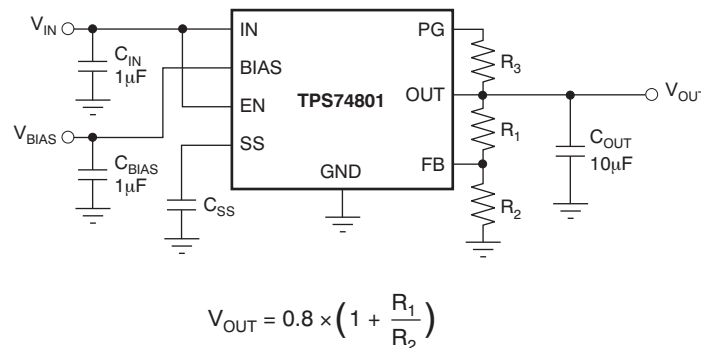
## APPLICATION INFORMATION

The TPS74801-Q1 belongs to a family of low dropout regulators that feature soft-start capability. These regulators use a low current bias input to power all internal control circuitry, allowing the NMOS pass transistor to regulate very low input and output voltages.

The use of an NMOS-pass FET offers several critical advantages for many applications. Unlike a PMOS topology device, the output capacitor has little effect on loop stability. This architecture allows the TPS74801-Q1 to be stable with any capacitor type of value 2.2  $\mu\text{F}$  or greater. Transient response is also superior to PMOS topologies, particularly for low  $V_{\text{IN}}$  applications.

The TPS74801-Q1 features a programmable voltage-controlled soft-start circuit that provides a smooth, monotonic start-up and limits startup inrush currents that may be caused by large capacitive loads. A power good (PG) output is available to allow supply monitoring and sequencing of other supplies. An enable (EN) pin with hysteresis and deglitch allows slow-ramping signals to be used for sequencing the device. The low  $V_{\text{IN}}$  and  $V_{\text{OUT}}$  capability allows for inexpensive, easy-to-design, and efficient linear regulation between the multiple supply voltages often present in processor-intensive systems.

Figure 25 illustrates the typical application circuit for the TPS74801-Q1 adjustable output device.



**Figure 25. Typical Application Circuit for the TPS74801-Q1 (Adjustable)**

$R_1$  and  $R_2$  can be calculated for any output voltage using the formula shown in Figure 25. Refer to Table 1 for sample resistor values of common output voltages. In order to achieve the maximum accuracy specifications,  $R_2$  should be  $\leq 4.99 \text{ k}\Omega$ .

### INPUT, OUTPUT, AND BIAS CAPACITOR REQUIREMENTS

The device is designed to be stable for all available types and values of output capacitors  $\geq 2.2 \mu\text{F}$ . The device is also stable with multiple capacitors in parallel, which can be of any type or value.

The capacitance required on the IN and BIAS pins strongly depends on the input supply source impedance. To counteract any inductance in the input, the minimum recommended capacitor for  $V_{\text{IN}}$  and  $V_{\text{BIAS}}$  is 1  $\mu\text{F}$ . If  $V_{\text{IN}}$  and  $V_{\text{BIAS}}$  are connected to the same supply, the recommended minimum capacitor for  $V_{\text{BIAS}}$  is 4.7  $\mu\text{F}$ . Good quality, low ESR capacitors should be used on the input; ceramic X5R and X7R capacitors are preferred. These capacitors should be placed as close the pins as possible for optimum performance.

### TRANSIENT RESPONSE

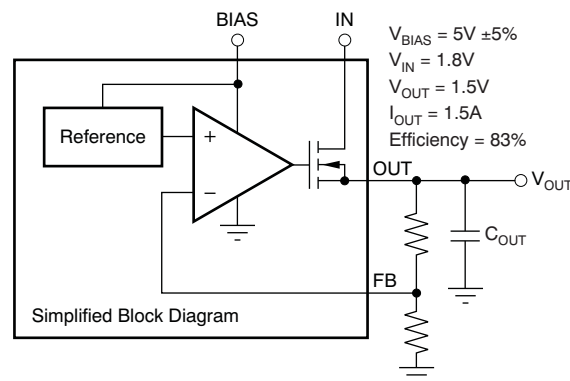
The TPS74801-Q1 was designed to have excellent transient response for most applications with a small amount of output capacitance. In some cases, the transient response may be limited by the transient response of the input supply. This limitation is especially true in applications where the difference between the input and output is less than 300 mV. In this case, adding additional input capacitance improves the transient response much more than just adding additional output capacitance would do. With a solid input supply, adding additional output capacitance reduces undershoot and overshoot during a transient event; refer to Figure 22 in the Typical

**Characteristics** section. Because the TPS74801-Q1 is stable with output capacitors as low as 2.2  $\mu\text{F}$ , many applications may then need very little capacitance at the LDO output. For these applications, local bypass capacitance for the powered device may be sufficient to meet the transient requirements of the application. This design reduces the total solution cost by avoiding the need to use expensive, high-value capacitors at the LDO output.

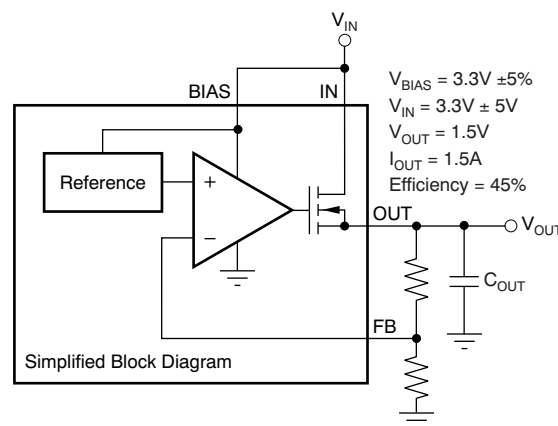
## DROPOUT VOLTAGE

The TPS74801-Q1 offers very low dropout performance, making it well-suited for high-current, low  $V_{\text{IN}}$  / low  $V_{\text{OUT}}$  applications. The low dropout of the TPS74801-Q1 allows the device to be used in place of a DC-DC converter and still achieve good efficiency. This provides designers with the power architecture for their application to achieve the smallest, simplest, and lowest cost solution.

There are two different specifications for dropout voltage with the TPS74801-Q1. The first specification (shown in [Figure 26](#)) is referred to as  $V_{\text{IN}}$  Dropout and is used when an external bias voltage is applied to achieve low dropout. This specification assumes that  $V_{\text{BIAS}}$  is at least 3.25 V<sup>(1)</sup> above  $V_{\text{OUT}}$ , which is the case for  $V_{\text{BIAS}}$  when powered by a 5-V rail with 5% tolerance and with  $V_{\text{OUT}} = 1.5\text{ V}$ . If  $V_{\text{BIAS}}$  is higher than  $V_{\text{OUT}} 3.25\text{ V}^{(1)}$ ,  $V_{\text{IN}}$  dropout is less than specified.



**Figure 26. Typical Application of the TPS74801-Q1 Using an Auxiliary Bias Rail**



**Figure 27. Typical Application of the TPS74801-Q1 Without an Auxiliary Bias Rail**

The second specification (shown in [Figure 27](#)) is referred to as  $V_{\text{BIAS}}$  Dropout and applies to applications where IN and BIAS are tied together. This option allows the device to be used in applications where an auxiliary bias voltage is not available or low dropout is not required. Dropout is limited by BIAS in these applications because  $V_{\text{BIAS}}$  provides the gate drive to the pass FET; therefore,  $V_{\text{BIAS}}$  must be 1.6 V above  $V_{\text{OUT}}$ . Because of this usage, IN and BIAS tied together easily consume huge power. Pay attention not to exceed the power rating of the IC package.

(1) 3.25 V is a test condition of this device and can be adjusted by referring to [Figure 8](#).

## PROGRAMMABLE SOFT-START

The TPS74801-Q1 features a programmable, monotonic, voltage-controlled soft-start that is set with an external capacitor ( $C_{SS}$ ). This feature is important for many applications because it eliminates power-up initialization problems when powering FPGAs, DSPs, or other processors. The controlled voltage ramp of the output also reduces peak inrush current during start-up, minimizing start-up transient events to the input power bus.

To achieve a linear and monotonic soft-start, the TPS74801-Q1 error amplifier tracks the voltage ramp of the external soft-start capacitor until the voltage exceeds the internal reference. The soft-start ramp time depends on the soft-start charging current ( $I_{SS}$ ), soft-start capacitance ( $C_{SS}$ ), and the internal reference voltage ( $V_{REF}$ ), and can be calculated using [Equation 1](#):

$$t_{SS} = \frac{V_{REF} \times C_{SS}}{I_{SS}} \quad (1)$$

If large output capacitors are used, the device current limit ( $I_{CL}$ ) and the output capacitor may set the start-up time. In this case, the start-up time is given by [Equation 2](#):

$$t_{SSCL} = \frac{V_{OUT(NOM)} \times C_{OUT}}{I_{CL(MIN)}} \quad (2)$$

where:

$V_{OUT(NOM)}$  is the nominal output voltage,

$C_{OUT}$  is the output capacitance, and

$I_{CL(MIN)}$  is the minimum current limit for the device.

In applications where monotonic startup is required, the soft-start time given by [Equation 1](#) should be set greater than [Equation 2](#).

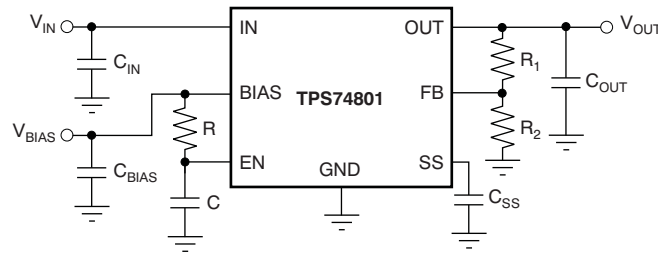
The maximum recommended soft-start capacitor is 0.015  $\mu$ F. Larger soft-start capacitors can be used and do not damage the device; however, the soft-start capacitor discharge circuit may not be able to fully discharge the soft-start capacitor when enabled. Soft-start capacitors larger than 0.015  $\mu$ F could be a problem in applications where it is necessary to rapidly pulse the enable pin and still require the device to soft-start from ground.  $C_{SS}$  must be low-leakage; X7R, X5R, or C0G dielectric materials are preferred. Refer to [Table 2](#) for suggested soft-start capacitor values.

## SEQUENCING REQUIREMENTS

$V_{IN}$ ,  $V_{BIAS}$ , and  $V_{EN}$  can be sequenced in any order without causing damage to the device. However, for the soft-start function to work as intended, certain sequencing rules must be applied. Connecting EN to IN is acceptable for most applications, as long as  $V_{IN}$  is greater than 1.1 V and the ramp rate of  $V_{IN}$  and  $V_{BIAS}$  is faster than the set soft-start ramp rate. If the ramp rate of the input sources is slower than the set soft-start time, the output tracks the slower supply minus the dropout voltage until it reaches the set output voltage. If EN is connected to BIAS, the device soft-starts as programmed, provided that  $V_{IN}$  is present before  $V_{BIAS}$ . If  $V_{BIAS}$  and  $V_{EN}$  are present before  $V_{IN}$  is applied and the set soft-start time has expired, then  $V_{OUT}$  tracks  $V_{IN}$ . If the soft-start time has not expired, the output tracks  $V_{IN}$  until  $V_{OUT}$  reaches the value set by the charging soft-start capacitor. [Figure 28](#) shows the use of an RC-delay circuit to hold off  $V_{EN}$  until  $V_{BIAS}$  has ramped. This technique can also be used to drive EN from  $V_{IN}$ . An external control signal can also be used to enable the device after  $V_{IN}$  and  $V_{BIAS}$  are present.

### NOTE

When  $V_{BIAS}$  and  $V_{EN}$  are present and  $V_{IN}$  is not supplied, this device outputs approximately 50  $\mu$ A of current from OUT. Although this condition does not cause any damage to the device, the output current may charge up the OUT node if total resistance between OUT and GND (including external feedback resistors) is greater than 10 k $\Omega$ .



**Figure 28. Soft-Start Delay Using an RC Circuit to Enable the Device**

## OUTPUT NOISE

The TPS74801-Q1 provides low output noise when a soft-start capacitor is used. When the device reaches the end of the soft-start cycle, the soft-start capacitor serves as a filter for the internal reference. By using a 0.001- $\mu\text{F}$  soft-start capacitor, the output noise is reduced by half and is typically 30- $\mu\text{V}_{\text{RMS}}$  for a 1.2-V output (10 Hz to 100 kHz). Further increasing  $C_{\text{SS}}$  has little effect on noise. Because most of the output noise is generated by the internal reference, the noise is a function of the set output voltage. The RMS noise with a 0.001- $\mu\text{F}$  soft-start capacitor is given in [Equation 3](#):

$$V_{\text{N}}(\mu\text{V}_{\text{RMS}}) = 25 \left( \frac{\mu\text{V}_{\text{RMS}}}{\text{V}} \right) \times V_{\text{OUT}}(\text{V}) \quad (3)$$

The low output noise of the TPS74801-Q1 makes it a good choice for powering transceivers, PLLs, or other noise-sensitive circuitry.

## ENABLE AND SHUTDOWN

The enable (EN) pin is active high and is compatible with standard digital signaling levels.  $V_{\text{EN}}$  below 0.4 V turns the regulator off, while  $V_{\text{EN}}$  above 1.1 V turns the regulator on. Unlike many regulators, the enable circuitry has hysteresis and deglitching for use with relatively slowly ramping analog signals. This configuration allows the TPS74801-Q1 to be enabled by connecting the output of another supply to the EN pin. The enable circuitry typically has 50 mV of hysteresis and a deglitch circuit to help avoid on-off cycling as a result of small glitches in the  $V_{\text{EN}}$  signal.

The enable threshold is typically 0.8 V and varies with temperature and process variations. Temperature variation is approximately  $-1 \text{ mV}/^\circ\text{C}$ ; process variation accounts for most of the rest of the variation to the 0.4-V and 1.1-V limits. If precise turn-on timing is required, a fast rise-time signal must be used to enable the TPS74801-Q1.

If not used, EN can be connected to either IN or BIAS. If EN is connected to IN, it should be connected as close as possible to the largest capacitance on the input to prevent voltage droops on that line from triggering the enable circuit.

## POWER GOOD

The power good (PG) pin is an open-drain output and can be connected to any 5.5-V or lower rail through an external pull-up resistor. This pin requires at least 1.1 V on  $V_{\text{BIAS}}$  in order to have a valid output. The PG output is high-impedance when  $V_{\text{OUT}}$  is greater than  $V_{\text{IT}} + V_{\text{HYS}}$ . If  $V_{\text{OUT}}$  drops below  $V_{\text{IT}}$  or if  $V_{\text{BIAS}}$  drops below 1.9 V, the open-drain output turns on and pulls the PG output low. The PG pin also asserts when the device is disabled. The recommended operating condition of PG pin sink current is up to 1 mA, so the pull-up resistor for PG should be in the range of 10 k $\Omega$  to 1 M $\Omega$ . If output voltage monitoring is not needed, the PG pin can be left floating.

## INTERNAL CURRENT LIMIT

The TPS74801-Q1 features a factory-trimmed, accurate current limit that is flat over temperature and supply voltage. The current limit allows the device to supply surges of up to 2 A and maintain regulation. The current limit responds in approximately 10  $\mu\text{s}$  to reduce the current during a short-circuit fault.

The internal current limit protection circuitry of the TPS74801-Q1 is designed to protect against overload conditions. It is not intended to allow operation above the rated current of the device. Continuously running the TPS74801-Q1 above the rated current degrades device reliability.

## THERMAL PROTECTION

Thermal protection disables the output when the junction temperature rises to approximately 160°C, allowing the device to cool. When the junction temperature cools to approximately 140°C, the output circuitry is enabled. Depending on power dissipation, thermal resistance, and ambient temperature the thermal protection circuit may cycle on and off. This cycling limits the dissipation of the regulator, protecting it from damage as a result of overheating.

Activation of the thermal protection circuit indicates excessive power dissipation or inadequate heatsinking. For reliable operation, junction temperature should be limited to 150°C maximum. To estimate the margin of safety in a complete design (including heatsink), increase the ambient temperature until thermal protection is triggered; use worst-case loads and signal conditions. For good reliability, thermal protection should trigger at least 40°C above the maximum expected ambient condition of the application. This condition produces a worst-case junction temperature of 150°C at the highest expected ambient temperature and worst-case load.

The internal protection circuitry of the TPS74801-Q1 is designed to protect against overload conditions. It is not intended to replace proper heatsinking. Continuously running the TPS74801-Q1 into thermal shutdown degrades device reliability.

## LAYOUT RECOMMENDATIONS AND POWER DISSIPATION

An optimal layout can greatly improve transient performance, PSRR, and noise. To minimize the voltage drop on the input of the device during load transients, the capacitance on IN and BIAS should be connected as close as possible to the device. This capacitance also minimizes the effects of parasitic inductance and resistance of the input source and can, therefore, improve stability. To achieve optimal transient performance and accuracy, the top side of R<sub>1</sub> in [Figure 25](#) should be connected as close as possible to the load. If BIAS is connected to IN, it is recommended to connect BIAS as close to the sense point of the input supply as possible. This connection minimizes the voltage drop on BIAS during transient conditions and can improve the turn-on response.

Knowing the device power dissipation and proper sizing of the thermal plane that is connected to the thermal pad is critical to avoiding thermal shutdown and ensuring reliable operation. Power dissipation of the device depends on input voltage and load conditions and can be calculated using [Equation 4](#):

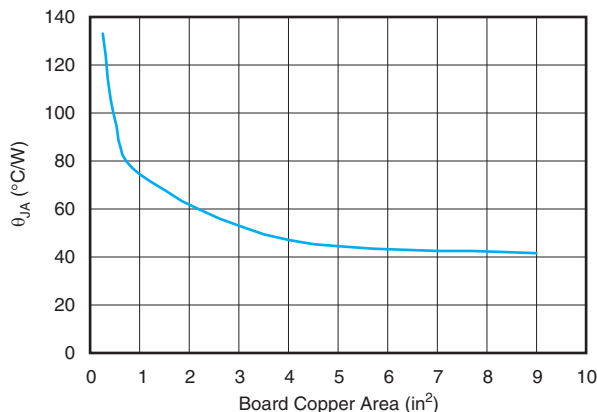
$$P_D = (V_{IN} - V_{OUT}) \times I_{OUT} \quad (4)$$

Power dissipation can be minimized and greater efficiency can be achieved by using the lowest possible input voltage necessary to achieve the required output voltage regulation.

The primary conduction path for heat is through the exposed pad to the printed circuit board (PCB). The pad can be connected to ground or be left floating; however, it should be attached to an appropriate amount of copper PCB area to ensure the device does not overheat. The maximum junction-to-ambient thermal resistance depends on the maximum ambient temperature, maximum device junction temperature, and power dissipation of the device and can be calculated using [Equation 5](#):

$$R_{\theta JA} = \frac{(150^{\circ}\text{C} - T_A)}{P_D} \quad (5)$$

Knowing the maximum R<sub>θJA</sub>, the minimum amount of PCB copper area needed for appropriate heatsinking can be estimated using [Figure 29](#).



Note:  $\theta_{JA}$  value at board size of 9 in<sup>2</sup> (that is, 3-in × 3-in) is a JEDEC standard.

**Figure 29.  $\theta_{JA}$  vs Board Size**

Figure 29 shows the variation of  $\theta_{JA}$  as a function of ground plane copper area in the board. It is intended only as a guideline to demonstrate the effects of heat spreading in the ground plane and should not be used to estimate actual thermal performance in real application environments.

#### NOTE

When the device is mounted on an application PCB, it is strongly recommended to use  $\Psi_{JT}$  and  $\Psi_{JB}$ , as explained in the [Estimating Junction Temperature](#) section.

## ESTIMATING JUNCTION TEMPERATURE

Using the thermal metrics  $\Psi_{JT}$  and  $\Psi_{JB}$ , as shown in the [Thermal Information](#) table, the junction temperature can be estimated with corresponding formulas (given in [Equation 6](#)). For backwards compatibility, an older  $\theta_{JC, Top}$  parameter is listed as well.

$$\Psi_{JT}: T_J = T_T + \Psi_{JT} \cdot P_D$$

$$\Psi_{JB}: T_J = T_B + \Psi_{JB} \cdot P_D \quad (6)$$

Where  $P_D$  is the power dissipation shown by [Equation 4](#),  $T_T$  is the temperature at the center-top of the IC package, and  $T_B$  is the PCB temperature measured 1mm away from the IC package *on the PCB surface* (see [Figure 31](#)).

#### NOTE

Both  $T_T$  and  $T_B$  can be measured on actual application boards using a thermo-gun (an infrared thermometer).

For more information about measuring  $T_T$  and  $T_B$ , see the application note [SBVA025, Using New Thermal Metrics](#), available for download at [www.ti.com](http://www.ti.com).

By looking at [Figure 30](#), the new thermal metrics ( $\Psi_{JT}$  and  $\Psi_{JB}$ ) have very little dependency on board size. That is, using  $\Psi_{JT}$  or  $\Psi_{JB}$  with [Equation 6](#) is a good way to estimate  $T_J$  by simply measuring  $T_T$  or  $T_B$ , regardless of the application board size.



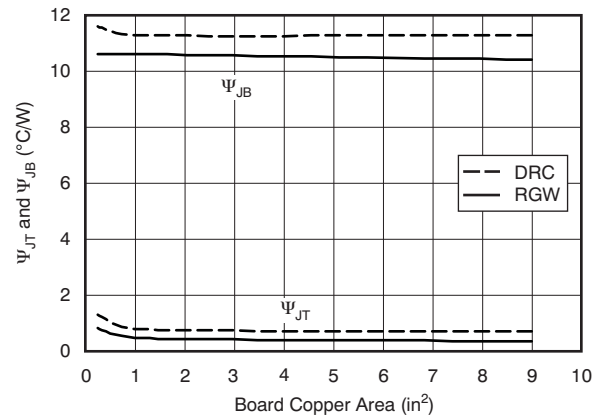
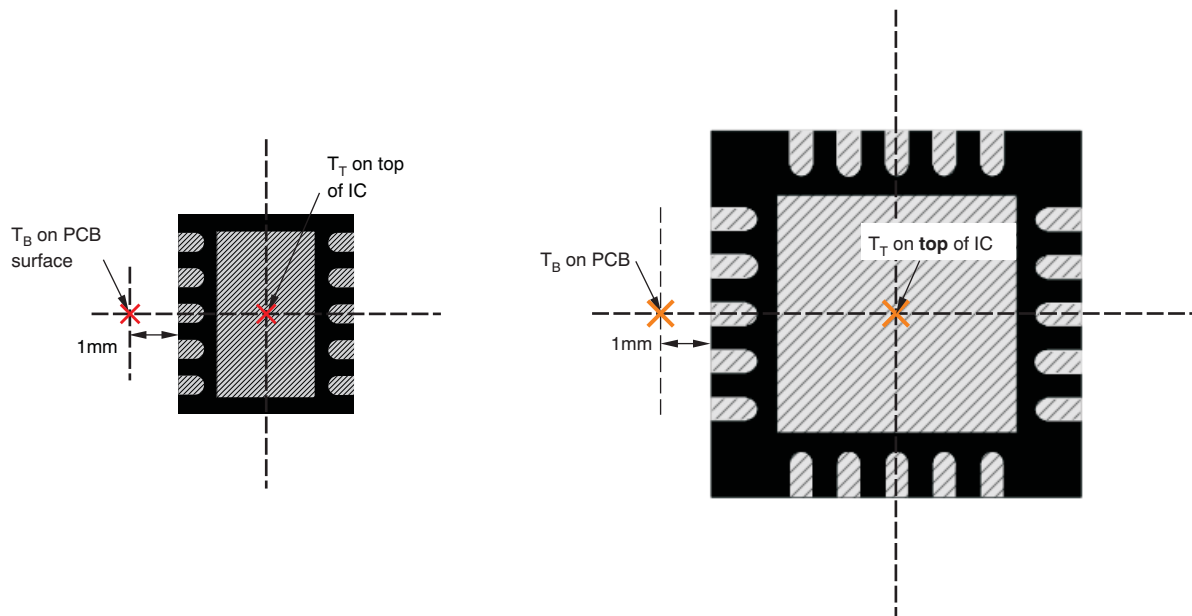


Figure 30.  $\Psi_{JT}$  and  $\Psi_{JB}$  vs Board Size

For a more detailed discussion of why TI does not recommend using  $\theta_{JC(top)}$  to determine thermal characteristics, refer to application report [SBVA025](#), *Using New Thermal Metrics*, available for download at [www.ti.com](http://www.ti.com). For further information, refer to application report [SPRA953](#), *IC Package Thermal Metrics*, also available on the TI website.



(a) Example DRC (SON) Package Measurement

(b) Example RGW (QFN) Package Measurement

- (1)  $T_T$  is measured at the center of both the X- and Y-dimensional axes.
- (2)  $T_B$  is measured **below** the package lead on the PCB surface.

Figure 31. Measuring Points for  $T_T$  and  $T_B$

## REVISION HISTORY

Changes from Revision A (February 2011) to Revision B	Page
• Added AEC-Q100 info to Features. ....	1
• Added an extra sentence to the Description. ....	1
• Removed Ordering Information table. ....	2
• Changed Abs Max condition statement. ....	2
• Changed T <sub>J</sub> max temp limit from 125 to 150. ....	2
• Added ESD ratings to Abs Max table. ....	2
• Added RGW package to Thermal Information table. ....	3
• Added T <sub>A</sub> –40°C to 125°C in Electrical Characteristics condition; changed T <sub>J</sub> to T <sub>A</sub> . ....	4
• Changed T <sub>J</sub> to T <sub>A</sub> in VREF test condition. ....	4
• Removed T <sub>A</sub> and T <sub>J</sub> from Electrical Characteristics table. ....	4
• Added second package to Device Information section (Pinout drawing and Pin Descriptions table). ....	6
• Changed T <sub>J</sub> to T <sub>A</sub> throughout entire Typical Characteristics section. ....	7
• Image update - changed Junction Temperature to Ambient Temperature. ....	9
• Changed 125°C to 150°C in Thermal Protection section. ....	15
• Image update - changed temperature from 125°C to 150°C in equation. ....	15
• Replaced $\Psi_{JT}$ and $\Psi_{JB}$ vs Board Size with 2-package image. ....	17
• Replaced Measuring Points for T <sub>T</sub> and T <sub>B</sub> with 2-package image. ....	17

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS74801QRGWRQ1	ACTIVE	VQFN	RGW	20	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 125	TPS 74801Q	<a href="#">Samples</a>
TPS74801TDRCRQ1	ACTIVE	VSON	DRC	10	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 105	QVK	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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**OTHER QUALIFIED VERSIONS OF TPS74801-Q1 :**

- Catalog: [TPS74801](#)

**NOTE: Qualified Version Definitions:**

- Catalog - TI's standard catalog product

**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS74801QRGWRQ1	VQFN	RGW	20	3000	330.0	12.4	5.3	5.3	1.5	8.0	12.0	Q2
TPS74801TDRCRQ1	VSON	DRC	10	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2

## TAPE AND REEL BOX DIMENSIONS

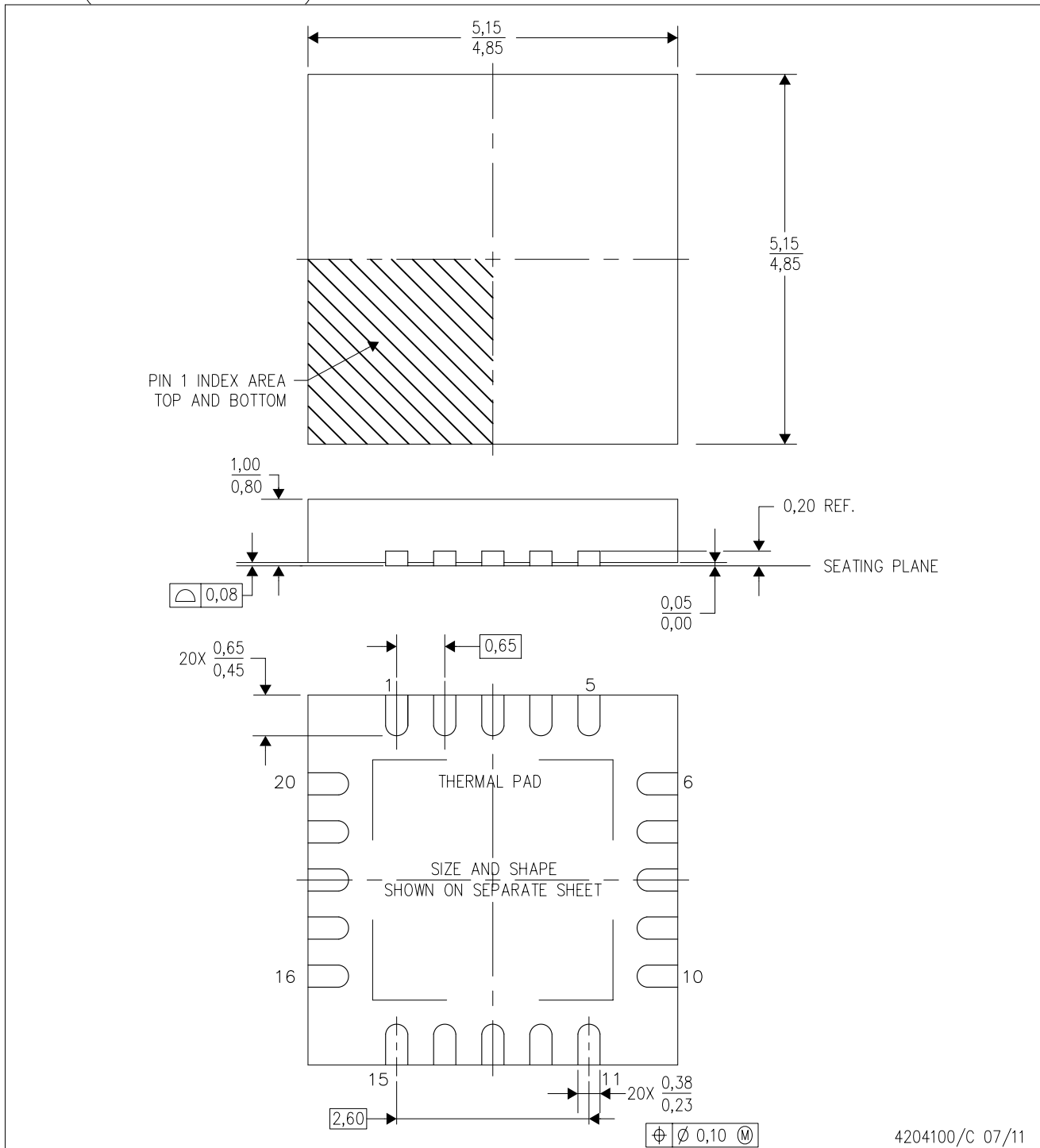


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS74801QRGWRQ1	VQFN	RGW	20	3000	367.0	367.0	35.0
TPS74801TDRCRQ1	VSON	DRC	10	3000	367.0	367.0	35.0

RGW (S-PVQFN-N20)

PLASTIC QUAD FLATPACK NO-LEAD



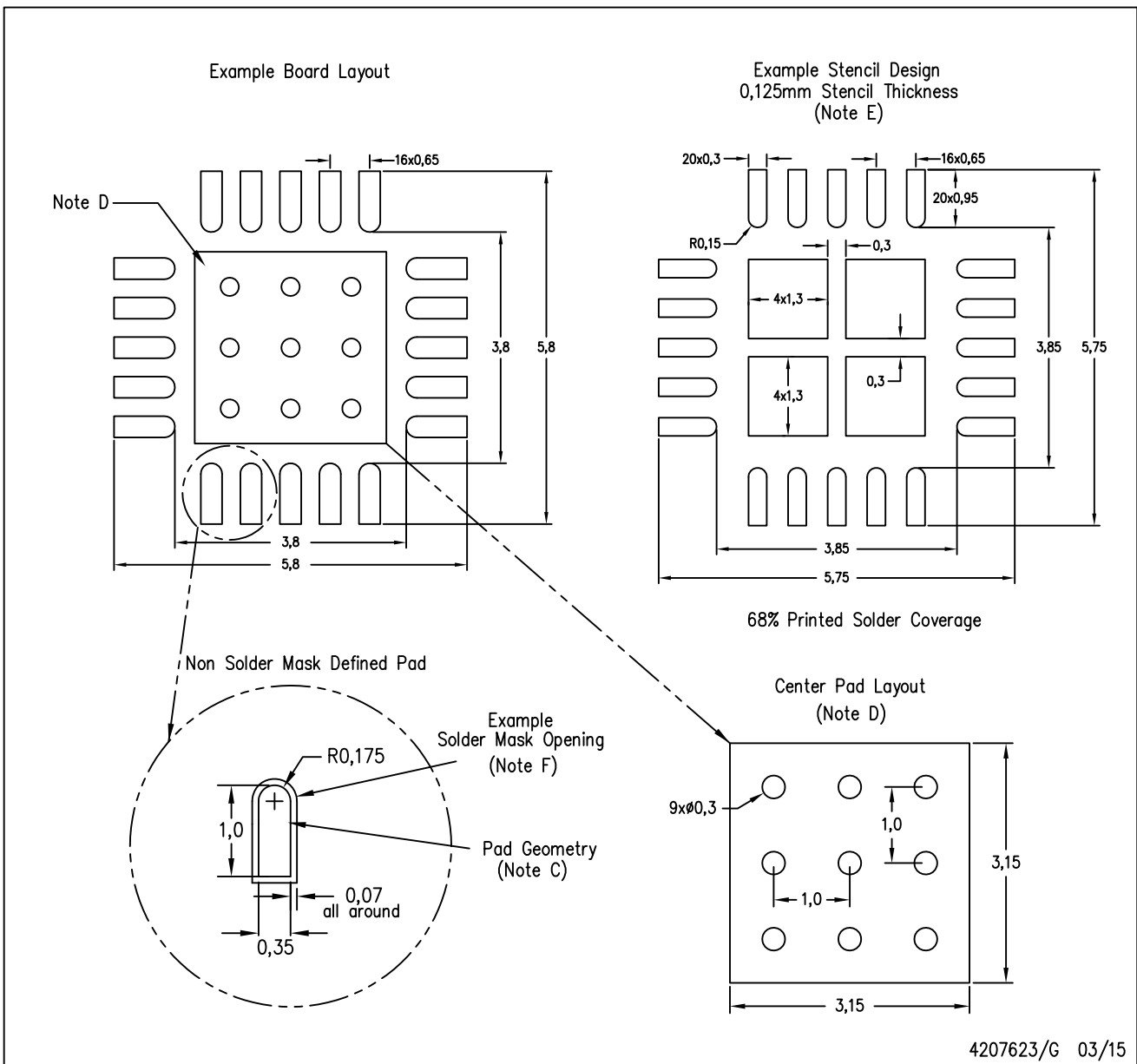
- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5-1994.
  - B. This drawing is subject to change without notice.
  - C. Quad Flat pack, No-leads (QFN) package configuration
  - D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
  - E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
  - F. Falls within JEDEC MO-220.





RGW (S-PVQFN-N20)

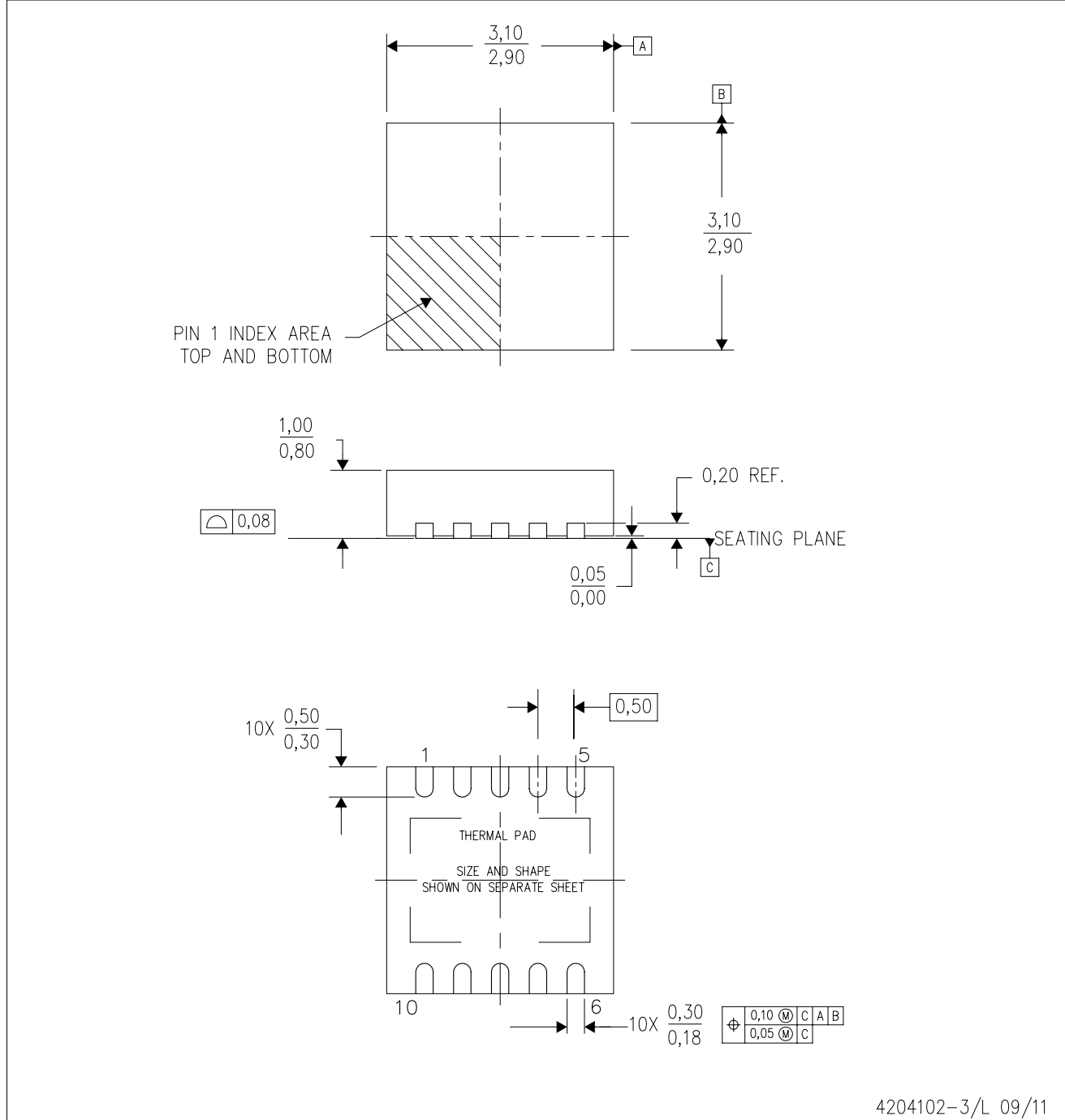
PLASTIC QUAD FLATPACK NO-LEAD



- NOTES:
- All linear dimensions are in millimeters.
  - This drawing is subject to change without notice.
  - Publication IPC-7351 is recommended for alternate designs.
  - This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, QFN Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at [www.ti.com](http://www.ti.com) <<http://www.ti.com>>.
  - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
  - Customers should contact their board fabrication site for solder mask tolerances.

DRC (S-PVSON-N10)

PLASTIC SMALL OUTLINE NO-LEAD



- NOTES:
- All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
  - This drawing is subject to change without notice.
  - Small Outline No-Lead (SON) package configuration.
  - The package thermal pad must be soldered to the board for thermal and mechanical performance, if present.
  - See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions, if present.

# THERMAL PAD MECHANICAL DATA

DRC (S-PVSON-N10)

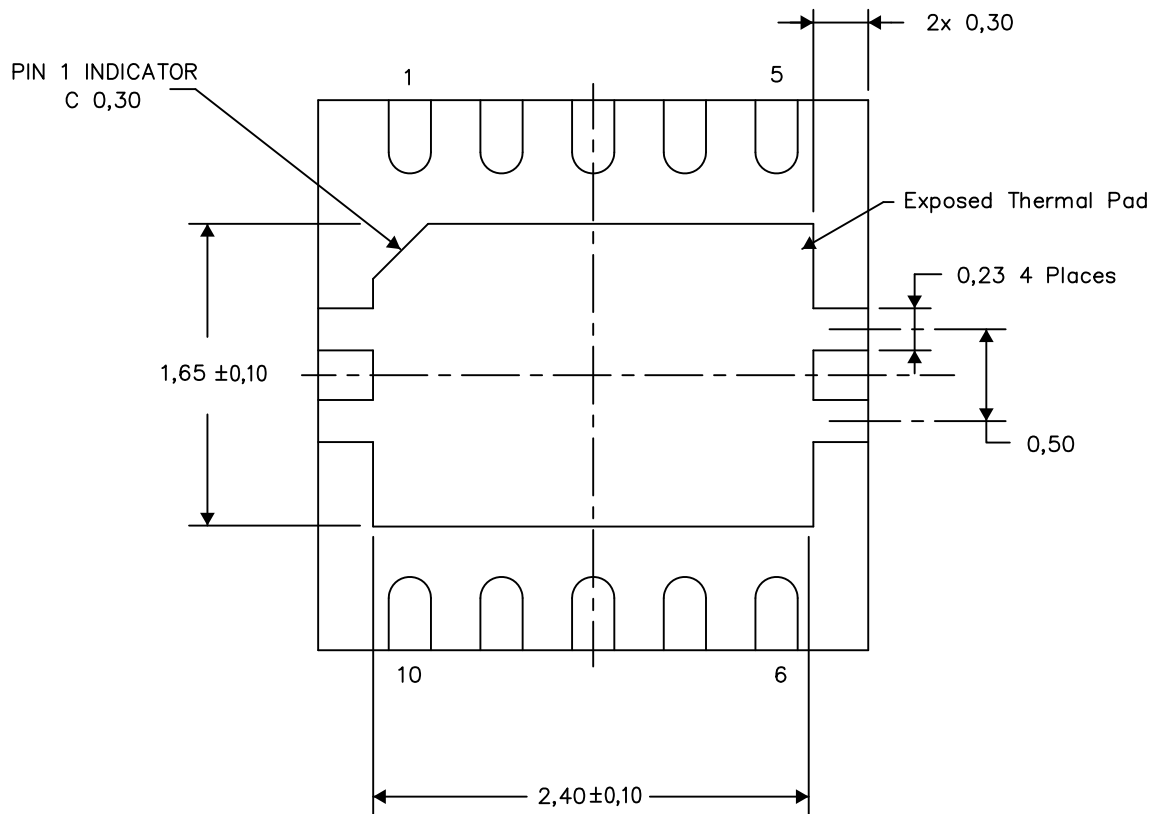
PLASTIC SMALL OUTLINE NO-LEAD

## THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at [www.ti.com](http://www.ti.com).

The exposed thermal pad dimensions for this package are shown in the following illustration.



Bottom View

Exposed Thermal Pad Dimensions

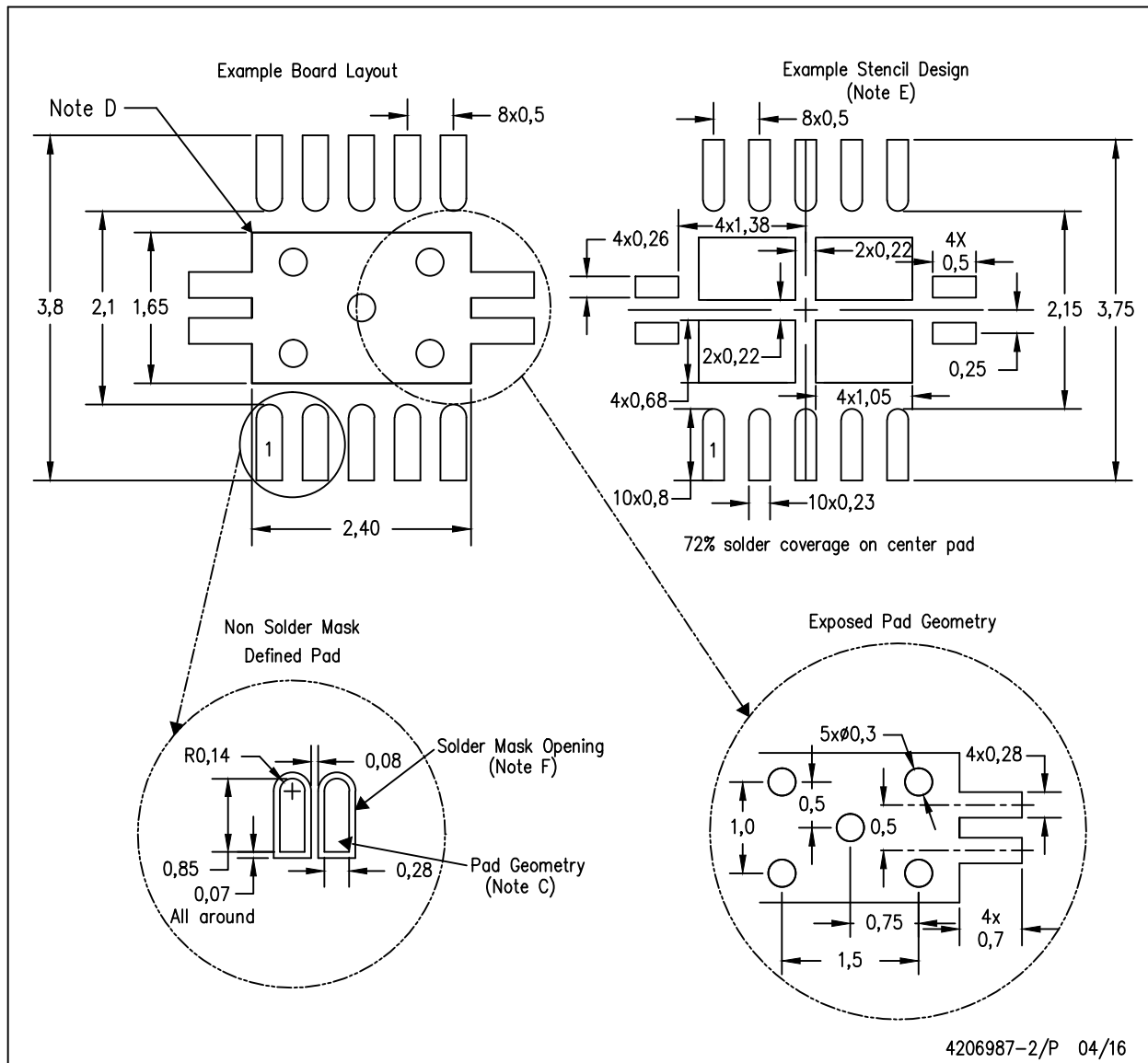
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NOTE: A. All linear dimensions are in millimeters

# LAND PATTERN DATA

DRC (S-PVSON-N10)

PLASTIC SMALL OUTLINE NO-LEAD



- NOTES:
- All linear dimensions are in millimeters.
  - This drawing is subject to change without notice.
  - Publication IPC-7351 is recommended for alternate designs.
  - This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat-Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at [www.ti.com](http://www.ti.com) <<http://www.ti.com>>.
  - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
  - Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.

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