具有电源路径管理功能和 I²C 接口的 bq2416xx 2.5A、双输入、单节电池开关模式锂离子电池充电器

1 特性

- 具有独立电源路径控制的高效开关模式充电器
  - 从深度放电电池或者在无电池的情况下快速启动系统
- 兼容 MaxLife™ 技术，与 bq27530 搭配使用时可实现快速充电
- 双输入、集成式 FET 充电器，充电电流高达 2.5A
  - 20V 输入额定值，具有过压保护 (OVP)
    - 6.5V，适用于高达 1.5A 的 USB 输入
    - 10.5V，适用于高达 2.5A 的 IN 输入（bq24160、bq24160A、bq24161、bq24163）
    - 6.5V，适用于高达 2.5A 的 IN 输入 (bq24168)
- 安全精准的电池管理功能
  - 电池稳压精度为 1%
  - 充电电流精度为 10%
- 可使用 I²C 接口对充电参数编程
- 基于电压的 NTC 监控输入
  - 符合 JEITA 标准（bq24160、bq24160A、bq24161B、bq24163、bq24168）
- 采用小型 2.8mm × 2.8mm 49 焊球 WCSP 封装或 4mm × 4mm VQFN-24 封装

2 应用

- 手持产品
- 便携式媒体播放器
- 便携式设备
- 上网本和便携式互联网器件

3 说明

bq24160、bq24160A、bq24161、bq24161B、bq24163 和 bq24168 是高度集成的单节锂离子电池充电器和系统电源路径管理器件，适用于采用高容量电池的空间受限型便携式 应用 。此单节电池充电器具有双输入，可由 USB 端口或更高功率的输入电源（即交流适配器或无线充电输入）供电，适用于多用途解决方案。这两个输入彼此完全隔离，并可以使用 I²C 接口方便地进行选择。

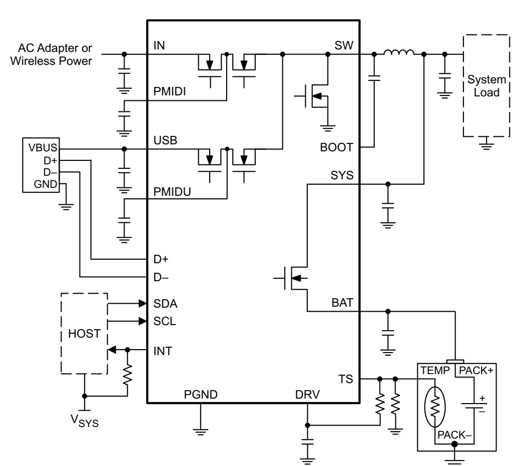
电源路径管理功能使得 bq2416xx 能够在对电池进行独立充电的同时通过一个高效的直流/直流转换器为系统供电。电源路径管理架构使系统能够采用有缺陷的电池组或在电池组缺失的情况下运行，并且即使在电池完全放电或者无电池的情况下也可实现即时系统启动。

器件信息

器件编号	封装	封装尺寸（标称值）
bq2416xx	VQFN (24)	4.00mm x 4.00mm
	DSBGA (49)	2.80mm × 2.80mm

(1) 如需了解所有可用封装，请见数据表末尾的可订购产品附录。

4 应用电路原理图



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5 修订历史记录

注：之前版本的页码可能与当前版本有所不同。

Changes from Revision F (July 2014) to Revision G	Page
• Deleted hyperlink to unpublished application note SLUA727	26

Changes from Revision E (November 2013) to Revision F	Page
• 已添加 *处理额定值* 表、*特性* *说明部分*，*器件功能模式*，*应用和实施部分*，*电源相关建议部分*，*布局部分*，*器件和文档支持部分以及机械、封装和可订购信息部分*	1
• Changed the Ordering Information table to the Device Comparison Table	4
• Changed to V_{BAD_SOURCE} include values for "During Bad Source Detection"	8
• Changed the Functional Block Diagram. Changed the device numbers above D+/D- and PSEL	13
• Changed the PWM Controller in Charge Mode section to include the soft-start function	15
• Changed the Battery Charging Process section. New text added starting with "The bq2416xx monitors the charging current.."	15
• Changed the Input Source Connected section	16
• Changed the Input Source Connected section	18
• Added the Reverse Boost (Boost Back) Prevention Circuit section	24

Changes from Revision D (November 2012) to Revision E	Page
• 添加了特性：兼容 MaxLife 技术，与 bq27530 搭配使用时可实现快速充电	1
• 将整个数据表中的 QFN-24 封装更改为 VQFN-24 封装	1

Changes from Revision C (October 2012) to Revision D	Page
• Changed the Ordering Information table to include the WSCP package for bq24161BRGR and bq24161BYFF	4

Changes from Revision B (September 2012) to Revision C **Page**

- Changed the Ordering Information table to include bq24160A 4

Changes from Revision A (March 2012) to Revision B **Page**

- Changed the Ordering Information table to include bq24161B 4
- Changed text From: "battery FET (Q6)" To: "battery FET (Q4)" in the Battery Only Connected section 18
- Changed From: $V_{WARM} < V_{TS} < V_{HOT}$ To: $V_{WARM} > V_{TS} > V_{HOT}$, and Changed From: $V_{COLD} < V_{TS} < V_{COOL}$ To: $V_{COLD} > V_{TS} > V_{COOL}$ in the External NTC Monitoring (TS) section 21
- Changed Figure 33 40

Changes from Original (November 2011) to Revision A **Page**

- Changed the USB Pin numbers in the YFF pachkage for bq24160/3 From: A5-A6 To: A5-A7 5
- Changed V_{BATREG} - Voltage regulation accuracy 7
- Changed Figure 21 34
- Changed Figure 22 35

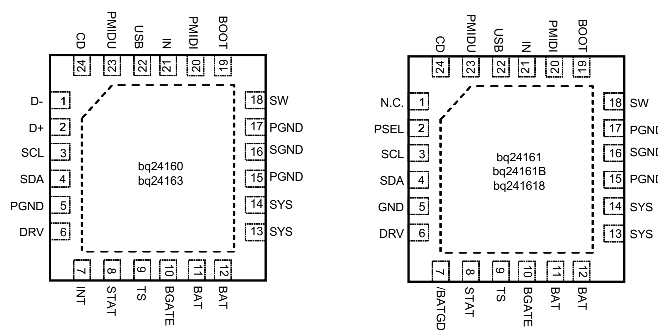
6 Device Comparison Table

PART NUMBER(1) (2)	USB OVP	IN OVP	USB DETECTION	TIMERS (Safety and Watchdog)	NTC MONITORING	$V_{BATSHRT}$/ $I_{BATSHRT}$	V_{MINSYS}
bq24160	6.5V	10.5V	D+/D–	Yes	JEITA	3.0V 50mA	3.5V
bq24160A	6.5V	10.5V	D+/D–	No	JEITA	3.0V 50mA	3.5V
bq24161	6.5V	10.5V	PSEL (0=1.5A, 1=100mA)	Yes	Standard	2.0V 50mA	3.5V
bq24161B	6.5V	10.5V	PSEL (0=1.5A, 1=500mA)	Yes	JEITA	3.0V 50mA	3.5V
bq24163	6.5V	10.5V	D+/D–	Yes	JEITA	2.0V 50mA	3.2V
bq24168	6.5V	6.5V	PSEL (0=1.5A, 1=100mA)	No	JEITA	2.0V 50mA	3.5V

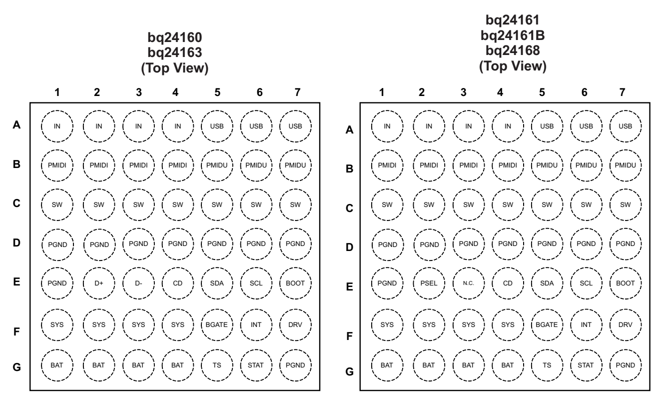
(1) Each of the above are available in as YFF and RGE packages with the following options:
R - tabed and reeled in quantities of 3,000 devices per reel.
T - taped and reeled in quantities of 250 devices per reel.
(2) This product is RoHS compatible, including a lead concentration that does not exceed 0.1% of total product weight, and is suitable for use in specified lead-free soldering processes. In addition, this product uses package materials that do not contain halogens, including bromine (Br) or antimony (Sb) above 0.1% of total product weight.

7 Pin Configuration and Functions

RGE Package
VQFN 24 Pins
Top View



YFF Package
WCSP 49 Pins
Top View



Pin Functions

PIN					I/O	DESCRIPTION
NAME	NO. bq24160, 3		NO. bq24161, 1B, 8			
	YFF	RGE	YFF	RGE		
BAT	G1-G4	11, 12	G1-G4	11, 12	I/O	**Battery Connection –** Connect to the positive terminal of the battery. Additionally, bypass BAT to GND with at least a 1μF capacitor.
BGATE	F5	10	F5	10	O	**External Discharge MOSFET Gate Connection –** BGATE drives an external P-Channel MOSFET to provide a very low-resistance discharge path. Connect BGATE to the gate of the external MOSFET. BGATE is low during high impedance mode and when no input is connected.
BOOT	E7	19	E7	19	I	**High Side MOSFET Gate Driver Supply –** Connect a 0.01μF ceramic capacitor (voltage rating > 10V) from BOOT to SW to supply the gate drive for the high side MOSFETs.
$\overline{CD}$	E4	24	E4	24	I	**IC Hardware Chip Disable Input –** Drive $\overline{CD}$ high to place the bq2416xx in high-z mode. Drive $\overline{CD}$ low for normal operation. Do not leave CD unconnected.
D+	E2	2	—	—	I	**D+ and D– Connections for USB Input Adapter Detection –** When a charge cycle is initiated by the USB input, and a short is detected between D+ and D–, the USB input current limit is set to 1.5A. If a short is not detected, the USB100 mode is selected. The D+/D– detection has no effect on the IN input.
D–	E3	1	—	—	I	
DRV	F7	6	F7	6	O	**Gate Drive Supply –** DRV is the bias supply for the gate drive of the internal MOSFETs. Bypass DRV to PGND with a 1μF ceramic capacitor. DRV may be used to drive external loads up to 10mA. DRV is active whenever the input is connected and $V_{SUPPLY} > V_{UVLO}$ and $V_{SUPPLY} > (V_{BAT} + V_{SLP})$
IN	A1- A4	21	A1- A4	21	I	**Input power supply –** IN is connected to the external DC supply (AC adapter or alternate power source). Bypass IN to PGND with at least a 1μF ceramic capacitor.
INT	F6	7	F6	7	O	**Status Output –** INT is an open-drain output that signals charging status and fault interrupts. INT pulls low during charging. INT is high impedance when charging is complete or the charger is disabled. When a fault occurs, a 128μs pulse is sent out as an interrupt for the host. INT is enabled/disabled using the EN_STAT bit in the control register. Connect INT to a logic rail through a 100kΩ resistor to communicate with the host processor.
PGND	D1-D7, E1, G7	5, 15, 16, 17	D1-D7, E1, G7	5, 15, 16, 17	—	**Ground terminal –** Connect to the thermal pad (for VQFN only) and the ground plane of the circuit.
PMIDI	B1-B4	20	B1-B4	20	O	**Reverse Blocking MOSFET and High Side MOSFET Connection Point for High Power Input –** Bypass PMIDI to GND with at least a 4.7μF ceramic capacitor. Use caution when connecting an external load to PMIDI. The PMIDI output is not current limited. Any short on PMIDI will damage the IC.
PMIDU	B5-B7	23	B5-B7	23	O	**Reverse Blocking MOSFET and High Side MOSFET Connection Point for USB Input –** Bypass PMIDU to GND with at least a 4.7μF ceramic capacitor. Use caution when connecting an external load to PMIDU. The PMIDU output is not current limited. Any short on PMIDU will damage the IC.
PSEL	—	—	E2	2		**USB Source Detection Input –** Drive PSEL high to indicate that a USB source is connected to the USB input. When PSEL is high, the IC starts up with a 100mA (bq24161/8) or 500mA (bq24161B) input current limit for USB. Drive PSEL low to indicate that an AC Adapter is connected to the USB input. When PSEL is low, the IC starts up with a 1.5A input current limit for USB. PSEL has no effect on the IN input. Do not leave PSEL unconnected.
SCL	E6	3	E6	3	I	**I^2C Interface Clock –** Connect SCL to the logic rail through a 10kΩ resistor.
SDA	E5	4	E5	4	I/O	**I^2C Interface Data –** Connect SDA to the logic rail through a 10kΩ resistor.
STAT	G6	8	G6	8	O	**Status Output –** STAT is an open-drain output that signals charging status and fault interrupts. STAT pulls low during charging. STAT is high impedance when charging is complete or the charger is disabled. When a fault occurs, a 128μs pulse is sent out as an interrupt for the host. STAT is enabled /disabled using the EN_STAT bit in the control register. Pull STAT up to a logic rail thruogh an LED for visual indication or through a 10kΩ resistor to communicate with the host processor.
SW	C1-C7	18	C1-C7	18	O	**Inductor Connection –** Connect to the switched side of the external inductor.
SYS	F1-F4	13, 14	F1-F4	13,14	I	**System Voltage Sense and Charger FET Connection –** Connect SYS to the system output at the output bulk capacitors. Bypass SYS locally with at least 10μF. A 47μF bypass capacitor is recommended for optimal transient response.
TS	G5	9	G5	9	I	**Battery Pack NTC Monitor –** Connect TS to the center tap of a resistor divider from DRV to GND. The NTC is connected from TS to GND. The TS function provides 4 thresholds for JEITA compatibility (160, 161B, 163, 168 only). TS faults are reported by the I^2C interface. See the *NTC Monitor* section for more details on operation and selecting the resistor values. Connect TS to DRV to disable the TS function.
USB	A5-A7	22	A5-A7	22	I	**USB Input Power Supply –** USB is connected to the external DC supply (AC adapter or USB port). Bypass USB to PGND with at least a 1μF ceramic capacitor.
Thermal Pad	—	Pad	—	Pad	—	There is an internal electrical connection between the exposed thermal pad and the PGND pin of the device. The thermal pad must be connected to the same potential as the PGND pin on the printed circuit board. Do not use the thermal pad as the primary ground input for the device. PGND pin must be connected to ground at all times.

8 Specifications

8.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Pin voltage range (with respect to VSS)	IN, USB	–2	20	V
	PMIDI, PMIDU, BOOT	–0.3	20	V
	SW	–0.7	12	V
	SDA, SCL, SYS, BAT, STAT, BGATE, DRV, TS, D+, D–, INT, PSEL, CD	–0.3	7	V
BOOT to SW		–0.3	7	V
Output current (Continuous)	SW	4.5		A
	SYS, BAT	3.5		A
Input current (Continuous)	IN	2.75		A
	USB	1.75		A
Output sink current	$\overline{\text{STAT}}$	10		mA
	INT	1		mA
Operating free-air temperature range		–40	85	°C
Junction temperature, T_J		–40	125	°C
Lead temperature (soldering, 10 s)		300		° C

(1) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability. All voltage values are with respect to the network ground terminal unless otherwise noted.

8.2 Handling Ratings

			MIN	MAX	UNIT
T_{stg}	Storage temperature range		–65	150	°C
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)		2	kV
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2)		500	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

8.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_{IN}	IN voltage range	4.2	18	V
	IN operating voltage range (bq24160/1/3)	4.2	10	
	IN operating voltage range (bq24168)	4.2	6	
V_{USB}	USB voltage range	4.2	18	V
	USB operating range	4.2	6	
I_{IN}	Input current, IN input		2.5	A
I_{USB}	Input current USB input		1.5	A
I_{SYS}	Output Current from SW, DC		3	A
I_{BAT}	Charging		2.5	A
	Discharging, using internal battery FET		2.5	A
T_J	Operating junction temperature range	0	125	ºC

8.4 Thermal Information

THERMAL METRIC[1]		bq2416xx 49 PINS (YFF)	bq2416xx 24 PINS (RGE)	UNIT
θ_{JA}	Junction-to-ambient thermal resistance	49.8	32.6	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance	0.2	30.5	°C/W
θ_{JB}	Junction-to-board thermal resistance	1.1	3.3	°C/W
ψ_{JT}	Junction-to-top characterization parameter	1.1	0.4	°C/W
ψ_{JB}	Junction-to-board characterization parameter	6.6	9.3	°C/W
θ_{JCbot}	Junction-to-case (bottom) thermal resistance	n/a	2.6	°C/W

(1) For more information about traditional and new thermal metrics, see the IC Package Thermal Metrics application report, SPRA953.

8.5 Electrical Characteristics

Circuit of Figure 21, $V_{SUPPLY} = V_{USB}$ or V_{IN} (whichever is supplying the IC), $V_{UVLO} < V_{SUPPLY} < V_{OVP}$ and $V_{SUPPLY} > V_{BAT}+V_{SLP}$, T_J = -40°C – 125°C and T_J = 25ºC for typical values (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
INPUT CURRENTS							
I_{SUPPLY}	Supply current for control (V_{IN} or V_{USB})	$V_{UVLO} < V_{SUPPLY} < V_{OVP}$ and $V_{SUPPLY} > V_{BAT}+V_{SLP}$	PWM switching		15		mA
			PWM NOT switching			5	
		0°C < T_J < 85°C, High-Z Mode				175	μA
$I_{BATLEAK}$	Leakage current from BAT to the Supply	0°C < T_J < 85°C, V_{BAT} = 4.2V, $V_{USB} = V_{IN}$ = 0V				5	μA
I_{BAT_HIZ}	Battery discharge current in High Impedance mode, (BAT, SW, SYS)	0°C< T_J < 85°C, V_{BAT} = 4.2V, V_{SUPPLY} = 5V or 0V, SCL, SDA = 0 V or 1.8V, High-Z Mode				55	μA
POWER-PATH MANAGEMENT							
$V_{SYS(REG)}$	System regulation voltage	Charge Enabled, $V_{BAT} < V_{MINSYS}$	bq24160, 1, 1B, 8	3.60	3.7	3.82	V
			bq24163	3.3	3.4	3.5	
		Battery FET turned off (Charge Disabled, TS Fault or Charging Terminated)		V_{BATREG} + 1.5%	V_{BATREG} + 3.0%	V_{BATREG} + 4.17%	
V_{MINSYS}	Minimum system regulation voltage	Charge enabled, $V_{BAT} < V_{MINSYS}$, Input current limit or V_{INDPM} active	bq24160, 1, 1B, 8	3.4	3.5	3.62	V
			bq24163	3.1	3.2	3.3	V
V_{BSUP1}	Enter supplement mode threshold	V_{BAT} > 2.5V			V_{BAT} –30mV		V
V_{BSUP2}	Exit supplement mode threshold	V_{BAT} > 2.5V			V_{BAT} –10mV		V
$I_{LIM(discharge)}$	Current limit, discharge or supplement mode	Current monitored in internal FET only.			7		A
$t_{DGL(SC1)}$	Deglitch time, SYS short circuit during discharge or supplement mode	Measured from ($V_{BAT} – V_{SYS}$) = 300mV to BAT high-impedance			250		µs
$t_{REC(SC1)}$	Recovery time, SYS short circuit during discharge or supplement mode				60		ms
	Battery range for BGATE and supplement mode operation			2.5		4.5	V
BATTERY CHARGER							
$R_{ON(BAT-SYS)}$	Internal battery charger MOSFET on-resistance	Measured from BAT to SYS, V_{BAT} = 4.2V	YFF pkg		37	57	mΩ
			RGE pkg		50	70	
V_{BATREG}	Charge Voltage	Operating in voltage regulation, Programmable range		3.5		4.44	V
	Voltage regulation accuracy			–1%		1%	
I_{CHARGE}	Fast charge current range	$V_{BATSHRT} \le V_{BAT} < V_{BAT(REG)}$ programmable range		550		2500	mA
	Fast charge current accuracy	0°C to 125°C		–10%		+10%	
$V_{BATSHRT}$	Battery short circuit threshold	100mV Hysteresis	bq24161, 3, 8	1.9	2.0	2.1	V
			bq24160, 1B	2.9	3.0	3.1	
$I_{BATSHRT}$	Battery short circuit current	$V_{BAT} < V_{BATSHRT}$			50		mA
$t_{DGL(BATSHRT)}$	Deglitch time for battery short circuit to fastcharge transition				32		ms
I_{TERM}	Termination charge current accuracy	I_{TERM} = 50mA		–35%		+35%	
		$I_{TERM} \ge$ 100mA		–15%		+15%	
$t_{DGL(TERM)}$	Deglitch time for charge termination	Both rising and falling, 2mV overdrive, t_{RISE}, t_{FALL} = 100ns			32		ms
V_{RCH}	Recharge threshold voltage	Below V_{BATREG}			120		mV
$t_{DGL(RCH)}$	Deglitch time	VBAT falling below VRCH, tFALL=100ns			32		ms

Electrical Characteristics (continued)

Circuit of Figure 21, $V_{SUPPLY} = V_{USB}$ or V_{IN} (whichever is supplying the IC), $V_{UVLO} < V_{SUPPLY} < V_{OVP}$ and $V_{SUPPLY} > V_{BAT}+V_{SLP}$, T_J = -40°C – 125°C and T_J = 25ºC for typical values (unless otherwise noted)

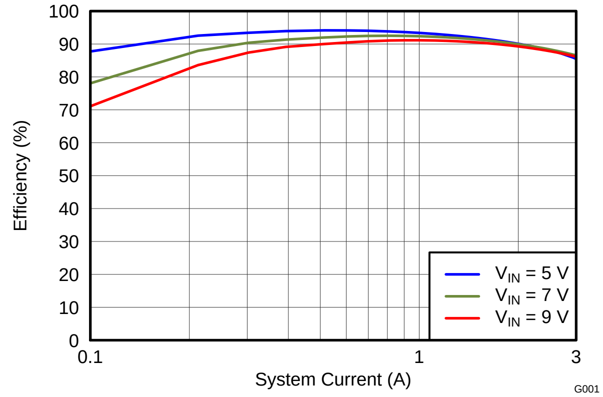
PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{DETECT}	Battery detection threshold	During battery detection source cycle			3.3		V
		During battery detection sink cycle			3.0		
I_{DETECT}	Battery detection current before charge done (sink current)	Termination enabled (EN_TERM = 1)			2.5		mA
t_{DETECT}	Battery detection time	Termination enabled (EN_TERM = 1)			250		ms
V_{IH}	PSEL, CD Input high logic level			1.3			V
V_{IL}	PSEL, CD Input low logic level					0.4	V
INPUT CURRENT LIMITING							
I_{IN_USB}	Input current limit threshold (USB input)	USB charge mode, V_{USB} = 5V, DC Current pulled from SW	I_{USBLIM} = USB100	90	95	100	mA
			I_{USBLIM} = USB500	450	475	500	
			I_{USBLIM} = USB150	135	142.5	150	
			I_{USBLIM} = USB900	800	850	900	
			I_{USBLIM} = USB800	700	750	800	
			I_{USBLIM} = 1.5A	1250	1400	1500	
I_{IN_IN}	Input current limit threshold (IN input)	IN charge mode, V_{IN} = 5V, DC Current pulled from SW	I_{INLIM} = 1.5A	1.35	1.5	1.65	A
			I_{INLIM} = 2.5A	2.3	2.5	2.8	
V_{IN_DPM}	Input based DPM threshold range	Charge mode, programmable via I^2C, both inputs		4.2		4.76	V
	V_{IN_DPM} threshold accuracy			–2		+2%	
VDRV BIAS REGULATOR							
V_{DRV}	Internal bias regulator voltage	V_{SUPPLY} > 5.45V		5	5.2	5.45	V
I_{DRV}	DRV output current			10			mA
V_{DO_DRV}	DRV Dropout voltage ($V_{SUPPLY} – V_{DRV}$)	I_{SUPPLY} = 1A, V_{SUPPLY} = 5V, I_{DRV} = 10mA				450	mV
STATUS OUTPUT (STAT, INT)							
V_{OL}	Low-level output saturation voltage	I_O = 10mA, sink current				0.4	V
I_{IH}	High-level leakage current	$V_{STAT} = V_{INT}$ = 5V				1	µA
PROTECTION							
V_{UVLO}	IC active threshold voltage	V_{IN} rising		3.6	3.8	4	V
V_{UVLO_HYS}	IC active hysteresis	V_{IN} falling from above V_{UVLO}		120	150		mV
V_{SLP}	Sleep-mode entry threshold, $V_{SUPPLY}-V_{BAT}$	2.0V ≤V_{BAT} ≤V_{BATREG}, V_{IN} falling		0	40	100	mV
V_{SLP_EXIT}	Sleep-mode exit hysteresis	2.0V ≤V_{BAT} ≤V_{BATREG}		40	100	175	mV
	Deglitch time for supply rising above $V_{SLP}+V_{SLP\_EXIT}$	Rising voltage, 2mV over drive, t_{RISE} = 100ns			30		ms
V_{BAD_SOURCE}	Bad source detection threshold	After Bad Source Detection completes			V_{IN_DPM} – 80 mV		V
		During Bad Source Detection			V_{IN_DPM} + 80 mV		V
$t_{DGL(BSD)}$	Deglitch on bad source detection				32		ms
V_{OVP}	Input supply OVP threshold voltage	USB, V_{USB} Rising		6.3	6.5	6.7	V
		IN, V_{IN} Rising (bq24160/1/1B/3)		10.3	10.5	10.7	
		IN, V_{IN} Rising (bq24168)		6.3	6.5	6.7	
$V_{OVP(HYS)}$	V_{OVP} hysteresis	Supply falling from V_{OVP}			100		mV
V_{BOVP}	Battery OVP threshold voltage	V_{BAT} threshold over V_{OREG} to turn off charger during charge		1.025 × V_{BATREG}	1.05 × V_{BATREG}	1.075 × V_{BATREG}	V
	V_{BOVP} hysteresis	Lower limit for V_{BAT} falling from above V_{BOVP}			1		% of V_{BATREG}
$t_{DGL(BOVP)}$	Battery OVP deglitch	BOVP fault shown in register once $t_{DGL(BOVP)}$ expires. Buck converter shut down immediately when $V_{BAT} > V_{BATOVP}$			1		ms
$V_{BATUVLO}$	Battery undervoltage lockout threshold	V_{BAT} rising, 100mV hysteresis			2.5		V
I_{LIMIT}	Cycle-by-cycle current limit	V_{SYS} shorted		4.1	4.9	5.6	A
T_{SHTDWN}	Thermal trip				165		°C
	Thermal hysteresis				10		
T_{REG}	Thermal regulation threshold	Charge current begins to cut off			120		°C
	Safety timer accuracy	(bq24160/1/1B/3 Only)		–20%		20%	
PWM							
	Internal top reverse blocking MOSFET on-resistance	I_{IN_LIMIT} = 500mA, Measured from USB to PMIDU			95	175	mΩ
		I_{IN_LIMIT} = 500mA, Measured from IN to PMIDI			45	80	

Electrical Characteristics (continued)

Circuit of Figure 21, V_{SUPPLY} = V_{USB} or V_{IN} (whichever is supplying the IC), V_{UVLO} < V_{SUPPLY} < V_{OVP} and V_{SUPPLY} > V_{BAT}+V_{SLP}, T_J = -40°C – 125°C and T_J = 25ºC for typical values (unless otherwise noted)

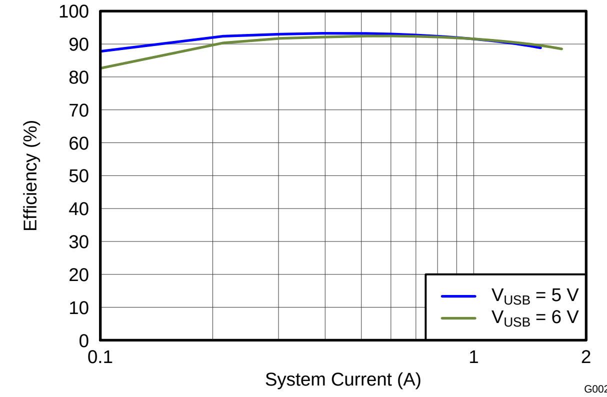
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Internal top N-channel Switching MOSFET on-resistance	Measured from PMIDU to SW		100	175	mΩ
		Measured from PMIDI to SW		65	110	
	Internal bottom N-channel MOSFET on-resistance	Measured from SW to PGND		65	115	mΩ
f_{OSC}	Oscillator frequency		1.35	1.50	1.65	MHz
D_{MAX}	Maximum duty cycle			95%		
D_{MIN}	Minimum duty cycle		0%			
BATTERY-PACK NTC MONITOR						
V_{HOT}	High temperature threshold	V_{TS} falling	29.7	30	30.5	$\%V_{DRV}$
$V_{HYS(HOT)}$	Hysteresis on high threshold	V_{TS} rising		1		
V_{WARM}	High temperature threshold	V_{TS} falling	37.9	38.3	39.6	$\%V_{DRV}$
$V_{HYS(WARM)}$	Hysteresis on high threshold	V_{TS} rising		1		
V_{COOL}	Low temperature threshold	V_{TS} falling	56	56.5	56.9	$\%V_{DRV}$
$V_{HYS(COOL)}$	Hysteresis on low threshold	V_{TS} rising		1		
V_{COLD}	Low temperature threshold	V_{TS} falling	59.5	60	60.4	$\%V_{DRV}$
$V_{HYS(COLD)}$	Hysteresis on low threshold	V_{TS} rising		1		
TSOFF	TS Disable threshold	V_{TS} rising, 2%V_{DRV} hysteresis	70		73	$\%V_{DRV}$
$t_{DGL(TS)}$	Deglitch time on TS change			50		ms
D+/D– DETECTION (bq24160)						
V_{D+_SRC}	D+ Voltage Source		0.5	0.6	0.7	V
I_{D+_SRC}	D+ Connection Check Current Source		7		14	µA
I_{D-_SINK}	D- Current Sink		50	100	150	µA
I_{D_LKG}	Leakage Current into D+/D-	D–, switch open	–1		1	µA
		D+, switch open	–1		1	µA
V_{D+_LOW}	D+ Low Comparator Threshold		0.8			V
$V_{D-\_LOWdatref}$	D- Low Comparator Threshold		250		400	mV
R_{D-_DWN}	D- Pulldown for Connection Check		14.25		24.8	kΩ
BATGD OPERATION						
V_{BATGD}	Good Battery threshold		3.6	3.8	3.9	V
	Deglitch for good battery threshold	V_{BAT} rising to HIGH-Z mode, DEFAULT Mode Only		32		ms
I²C COMPATIBLE INTERFACE						
V_{IH}	Input low threshold level	$V_{PULL-UP}$ = 1.8V, SDA and SCL	1.3			V
V_{IL}	Input low threshold level	$V_{PULL-UP}$ = 1.8V, SDA and SCL			0.4	V
V_{OL}	Output low threshold level	I_L = 10mA, sink current			0.4	V
I_{BIAS}	High-Level leakage current	$V_{PULL-UP}$ = 1.8V, SDA and SCL		1		µA
$t_{WATCHDOG}$	Watchdog timer timeout	(bq24160/1/3 Only)	30			s

8.6 Typical Characteristics



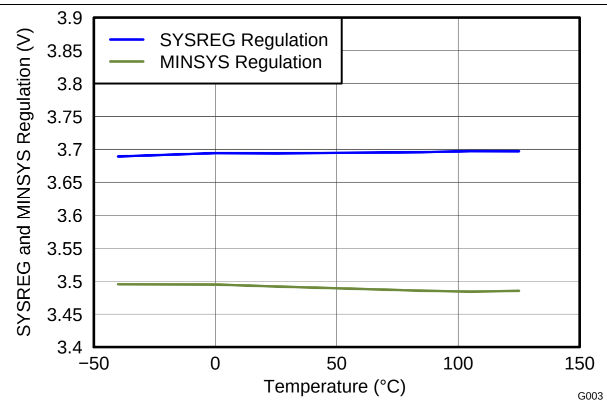
Charge Disabled
SYS loaded
V_{BATREG} = 3.6V
IN2500 ILIM

Figure 1. IN Efficiency



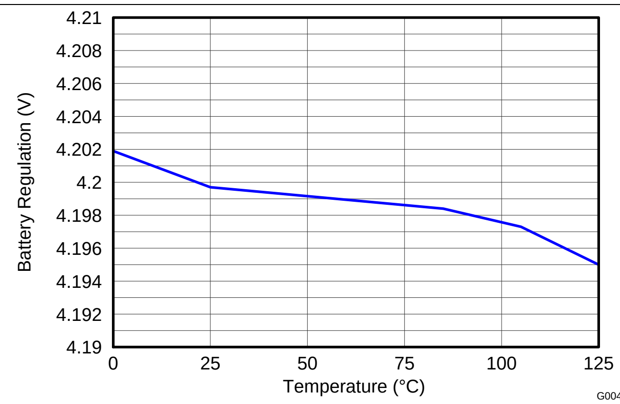
Charge Disabled
SYS loaded
V_{BATREG} = 3.6V
USB1500 ILIM

Figure 2. USB Efficiency



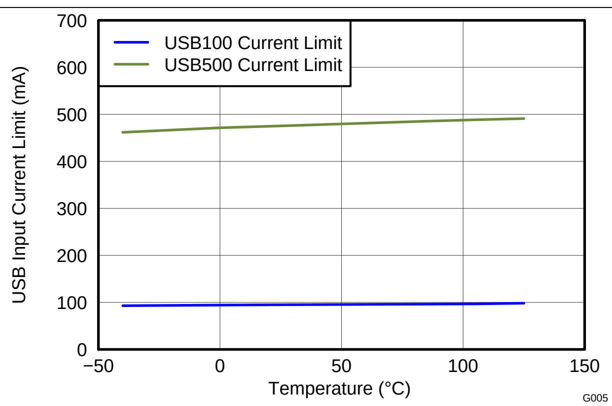
V_{BAT} = 3V

Figure 3. SYSREG and MINSYS Regulation vs Temperature



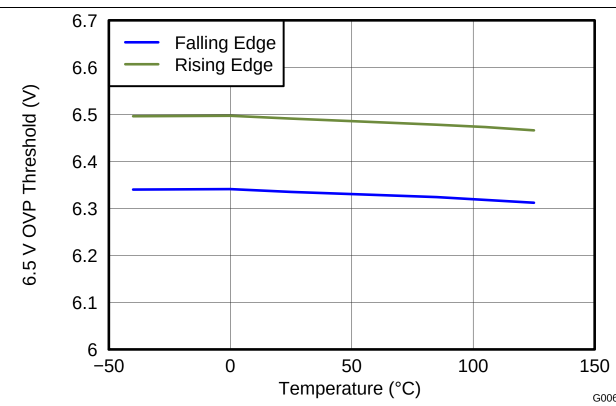
V_{BATREG} = 4.2V
No load
Termination Disabled

Figure 4. Battery Regulation vs Temperature



USB100 and USB500 current limit
V_{USB} = 5V
V_{BAT} = 3.6V

Figure 5. USB Input Current Limit vs. Temperature



USB input and IN input (bq24168)

Figure 6. 6.5V OVP Threshold vs. Temperature

Typical Characteristics (continued)

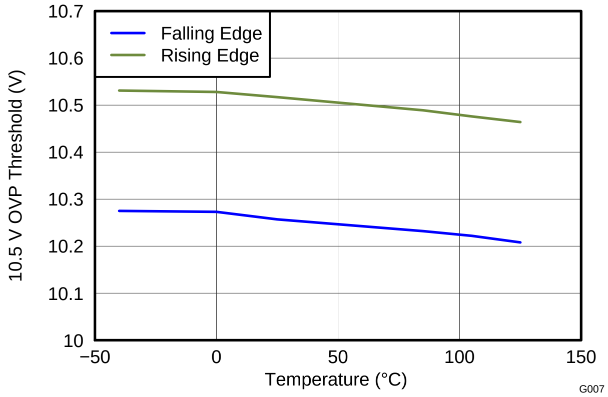
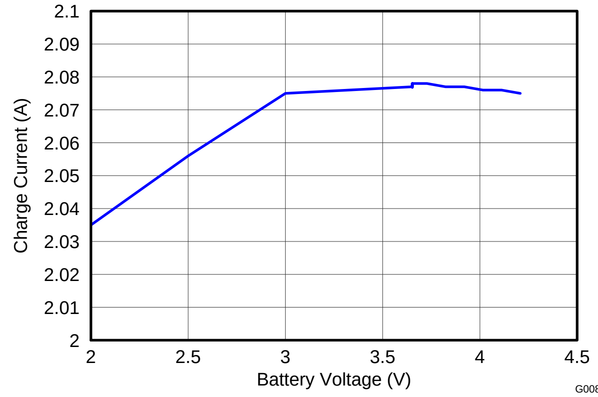


Figure 7. 10.5V OVP Threshold vs. Temperature



I_{CHARGE} = 2A
V_{IN} = 5V
V_{BATREG} = 4.44V

Figure 8. Charge Current vs. Battery Voltage

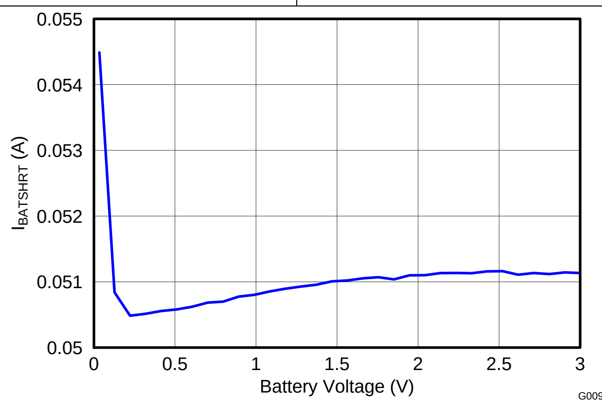


Figure 9. $I_{BATSHRT}$ vs. Battery Voltage

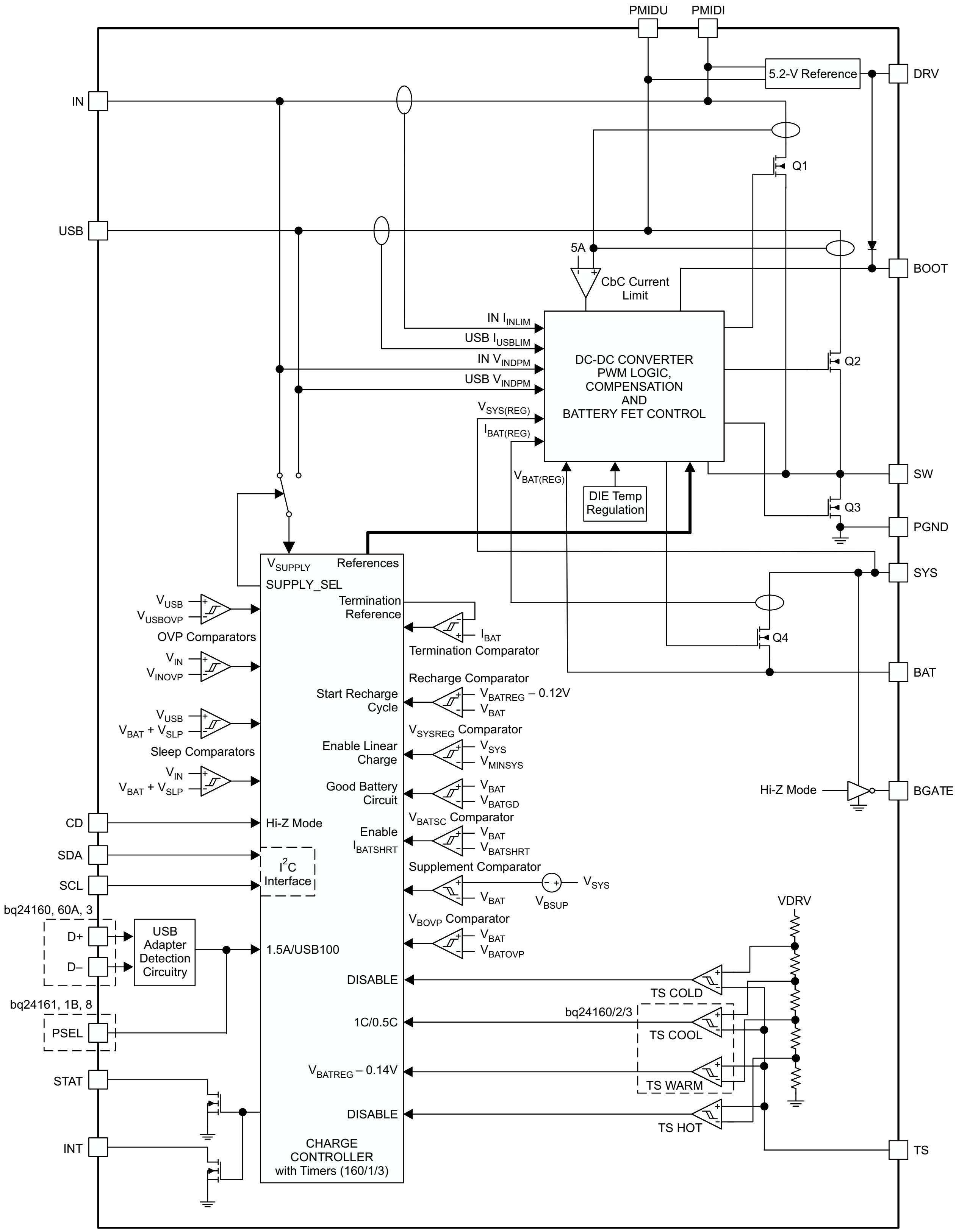
9 Detailed Description

9.1 Overview

The bq24160/bq24160A/bq24161/bq24161B/bq24163/bq24168 devices are highly integrated single-cell Li-Ion battery chargers and system power path management devices targeted for space-limited, portable applications with high-capacity batteries. The dual-input, single-cell charger operates from either a USB port or alternate power source (that is, wall adapter or wireless power input) for a versatile solution.

The power path management feature allows the bq2416xx to power the system from a high-efficiency DC-DC converter while simultaneously and independently charging the battery. The charger monitors the battery current at all times and reduces the charge current when the system load requires current above the input current limit. This allows proper charge termination and enables the system to run with a defective or absent battery pack. Additionally, this enables instant system turnon even with a totally discharged battery or no battery. The power-path management architecture also permits the battery to supplement the system current requirements when the adapter cannot deliver the peak system currents. This enables the use of a smaller adapter. The 2.5-A current capability allows for GSM phone calls as soon as the adapter is plugged in regardless of the battery voltage. The charge parameters are programmable using the I^2C interface.

9.2 Functional Block Diagram



9.3 Feature Description

9.3.1 Charge Mode Operation

9.3.1.1 Charge Profile

The internal battery MOSFET is used to charge the battery. When the battery is above the MINSYS voltage, the internal FET is on to maximize efficiency and the PWM converter regulates the charge current into the battery. When battery is less than MINSYS, the SYS is regulated to $V_{SYS(REG)}$ and battery is charged using the battery FET to regulate the charge current. There are 5 loops that influence the charge current:

- Constant current loop (CC)
- Constant voltage loop (CV)
- Thermal-regulation loop
- Minimum system-voltage loop (MINSYS)
- Input-voltage dynamic power-management loop (V_{IN}-DPM)

During the charging process, all five loops are enabled and the one that is dominant takes control. The bq2416xx supports a precision Li-Ion or Li-Polymer charging system for single-cell applications. The Dynamic Power Path Management (DPPM) feature regulates the system voltage to a minimum of V_{MINSYS}, so that startup is enabled even for a missing or deeply discharged battery. Figure 10 shows a typical charge profile including the minimum system output voltage feature.

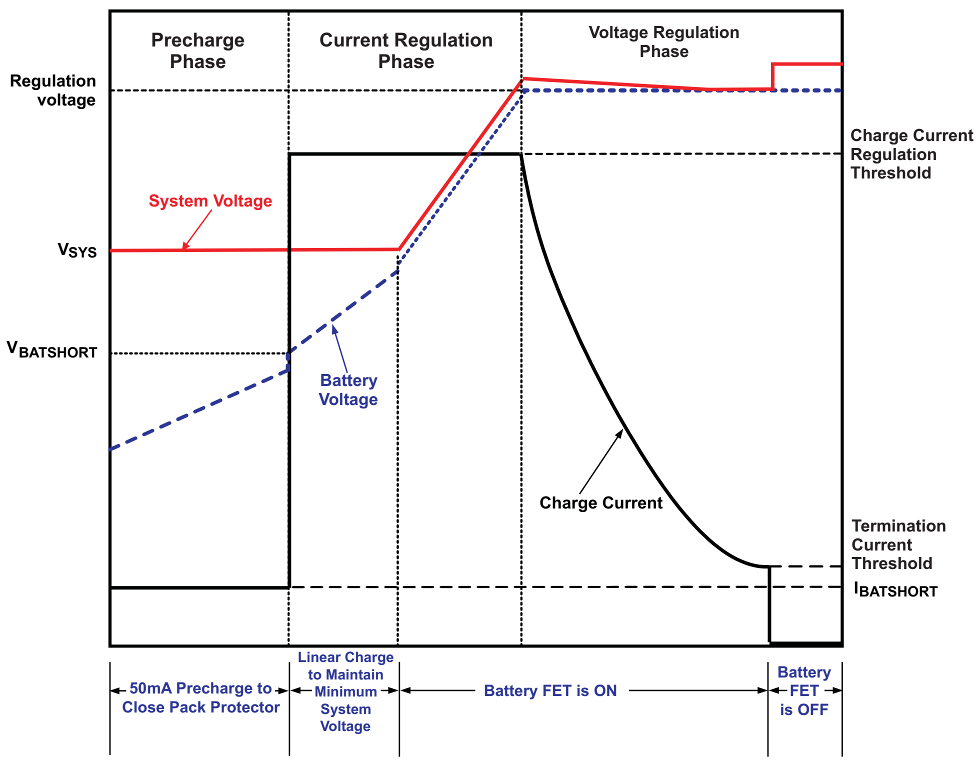


Figure 10. Typical bq2416xx Charging Profile

Feature Description (continued)

9.3.1.2 PWM Controller in Charge Mode

The bq2416xx provides an integrated, fixed-frequency 1.5MHz voltage-mode controller to power the system and supply the charge current. The voltage loop is internally compensated and provides enough phase margin for stable operation, allowing the use of small ceramic capacitors with low ESR. When starting up, the bq2416xx uses a "soft-start" function to help limit inrush current. When coming out of High Impedance mode, the bq2416xx starts up with the input current limit set to 40% of the value programmed in the I^2C register. After 80ms, the input current limit threshold steps up in 256µs steps. The steps are 40% to 50%, then 50% to 60%, then 60% to 70%, then 70% to 80%, and finally 80% to 100%. After the final step, soft start is complete and will not be restarted until the bq2416xx enters High Impedance mode.

The input scheme for the bq2416xx prevents battery discharge when the supply voltages are lower than VBAT and also isolates the two inputs from each other. The high-side N-MOSFET (Q1/Q2) switches to control the power delivered to the output. The DRV LDO provides a supply for the gate drive for the low side MOSFET, while a bootstrap circuit (BST) with an external bootstrap capacitor is used to boost up the gate drive voltage for Q1 and Q2.

Both inputs are protected by a cycle-by-cycle current limit that is sensed through the high-side MOSFETs for Q1 and Q2. The threshold for the current limit is set to a nominal 5A peak current. The inputs also utilize an input current limit that limits the current from the power source.

9.3.2 Battery Charging Process

Assuming a vaild input source is attached to IN or USB, as soon as a deeply discharged or shorted battery is attached to the BAT pin, ($V_{BAT} < V_{BATSHRT}$), the bq2416xx applies $I_{BATSHRT}$ to close the pack protector switch and bring the battery voltage up to acceptable charging levels. During this time, the battery FET is linearly regulated and the system output is regulated to $V_{SYS(REG)}$. Once the battery rises above $V_{BATSHRT}$, the charge current is regulated to the value set in the I^2C register. The battery FET is linearly regulated to maintain the system voltage at $V_{SYS(REG)}$. Under normal conditions, the time spent in this region is a very short percentage of the total charging time, so the linear regulation of the charge current does not affect the overall charging efficiency for very long. If the die temperature does rise, the thermal regulation circuit reduces the charge current to maintain a die temperature less than 120°C. If the current limit for the SYS output is reached (limited by the input current limit, or V_{IN_DPM}), the SYS output drops to the V_{MINSYS} output voltage. When this happens, the charge current is reduced to provide the system with all the current that is needed while maintaining the minimum system voltage. If the charge current is reduced to 0mA, pulling further current from SYS causes the output to fall to the battery voltage and enter supplement mode. (See the *Dynamic Power Path Management* section for more details.)

Once the battery is charged enough so that the system voltage begins to rise above $V_{SYS(REG)}$, the battery FET is turned on fully and the battery is charged with the full programmed charge current set by the I^2C interface, I_{CHARGE}. The slew rate for the fast-charge current is controlled to minimize current and voltage overshoot during transients. The charge current is regulated to I_{CHARGE} until the battery is charged to the regulation voltage. As the battery voltage rises above VRCH, the battery regulation loop is activated. This may result in a small step down in the charge current as the loops transition between the charge current and charge voltage loops. As the battery voltage charges up to the regulation voltage, V_{BATREG}, the charge current is tapered down as shown in Figure 10 while the SYS output remains connected to the battery. The voltage between the BAT and PGND pins is regulated to V_{BATREG}. The bq2416xx is a fixed single-cell voltage version, with adjustable regulation voltage (3.5V to 4.44V), programmed using the I^2C interface.

The bq2416xx monitors the charging current during the voltage-regulation phase. If the battery voltage is above the recharge threshold and the charge current has naturally tapered down to and remains below termination threshold, I_{TERM}, (without disturbance from events like supplement mode) for 32ms, the charger terminates charge, turns off the battery charging FET and enters battery detection. Termination is disabled when the charge current is reduced by a loop other than the voltage regulation loop or the input current limit is set to 100 mA. For example, when the bq2416xx is in half charge due to TS function, reverse boost protection is active, LOW_CHG bit is set, or the thermal regulation, V_{INDPM} or input current loops are active, termination will not occur. This prevents false termination events. During termination, the system output is regulated to the $V_{SYS(REG)}$ and supports the full current available from the input and the battery supplement mode is available. (See the *Dynamic*

Feature Description (continued)

Power Path Management section for more details.) The termination current level is programmable. When setting the termination threshold less than 150mA, the reverse boost protection may trip falsely with load transients and very fully charged batteries. This will prevent termination while in the reverse boost protection and may extend charge time. To disable the charge current termination, the host sets the charge termination bit (TE) of charge control register to 0, refer to I^2C section for details.

A new charge cycle is initiated if $\overline{CD}$ is low when either

1. V_{SUPPLY} rises above UVLO while a battery with $V_{BAT} < V_{BATREG} - V_{RCH}$ is attached or
2. a battery with $V_{BAT} < V_{BATREG} - V_{RCH}$ is attached while V_{SUPPLY} is above UVLO.

With V_{SUPPLY} above UVLO and V(BAT) < V_{BOVP}, a recharge cycle is initiated when one of the following conditions is detected:

1. The battery voltage falls below the $V_{BAT(REG)}$-V_{RCH} threshold.
2. $\overline{CE}$ bit toggle or RESET bit toggle
3. Supplement mode event occurs
4. $\overline{CD}$ pin or HI-Z bit toggle

$V_{BAT(REG)}$ should never be programmed less than V_{BAT}. If the battery is ever 5% above the regulation threshold, the battery OVP circuit shuts the PWM converter off immediately and the battery FET is turned on to discharge the battery to safe operating levels. If the battery OVP condition exists for the 1ms deglitch, a battery OVP fault is reported in the I^2C status registers. The battery OVP fault is cleared when the battery voltage discharges below V_{RCH} or if the IC enters hi-impedance mode (HZ_MODE=1 or CD=1). Always write bq2416xx to high impedance mode before changing V_{BATREG} to clear BOVP condition to ensure proper operation.

If the battery voltage is ever greater than VBATREG (for example, when an almost fully charged battery enters the JEITA WARM state due to the TS pin) but less than V_{BOVP}, the reverse boost protection circuitry may activate as explained later in this datasheet. If the battery is ever above V_{BOVP}, the buck converter turns off and the internal battery FET is turned on. This prevents further overcharging of the battery and allows the battery to discharge to safe operating levels. The battery OVP event does not clear until the battery voltage falls below V_{RCH}.

9.3.3 Battery Detection

When termination conditions are met, a battery detection cycle is started. During battery detection, I_{DETECT} is pulled from V_{BAT} for t_{DETECT} to verify there is a battery. If the battery voltage remains above V_{DETECT} for the full duration of t_{DETECT}, a battery is determined to present and the IC enters “Charge Done”. If V_{BAT} falls below V_{DETECT}, a “Battery Not Present” fault is signaled and battery detection continues. The next cycle of battery detection, the bq2416xx turns on $I_{BATSHORT}$ for t_{DETECT}. If V_{BAT} rises to V_{DETECT}, the current source is turned offand after t_{DETECT}, the battery detection continues through another current sink cycle. Battery detection continues until charge is disabled or a battery is detected. Once a battery is detected, the fault status clears and a new charge cycle begins. Battery detection is not run when termination is disabled.

9.3.4 Dynamic Power Path Management (DPPM)

The bq2416xx features a SYS output that powers the external system load connected to the battery. This output is active whenever a source is connected to IN, USB or BAT. The following sections discuss the behavior of SYS with a source connected to the supply or a battery source only.

9.3.5 Input Source Connected

When a valid input source is connected to IN or USB and the bq2416xx is NOT in High Impedance mode, the buck converter enters soft-start and turns on to power the load on SYS. The STAT/INT pin outputs a 128µs interrupt pulse to alert the host that an input has been connected. The FAULT bits indicate a normal condition, and the Supply Status register indicates that a new supply is connected. The $\overline{CE}$ bit (bit 1) in the control register (0x02) indicates whether a charge cycle is initiated. By default, the bq2416xx ($\overline{CE}$=0) enables a charge cycle when a valid input source is connected. When the $\overline{CE}$ bit is '1' and a valid input source is connected, the battery FET is turned off and the SYS output is regulated to the $V_{SYS(REG)}$ programmed by the V_{BATREG} threshold in the I^2C register. A charge cycle is initiated when the $\overline{CE}$ bit is written to a 0 value (cleared).

Feature Description (continued)

When the $\overline{CE}$ bit is a 0 and a valid source is connected to IN or USB, the buck converter starts up using soft-start. A charge cycle is initiated 64ms after the buck converter iniates startup. When V_{BAT} is high enough that $V_{SYS} > V_{SYS(REG)}$, the battery FET is turned on and the SYS output is connected to BAT. If the SYS voltage falls to $V_{SYS(REG)}$, it is regulated to that point to maintain the system output even with a deeply discharged or absent battery. In this mode, the SYS output voltage is regulated by the buck converter and the battery FET linearly regulates the charge current into the battery. The current from the supply is shared between charging the battery and powering the system load at SYS. The dynamic power-path management (DPPM) circuitry of the bq2416xx monitors the current limits continuously, and if the SYS voltage falls to the V_{MINSYS} voltage, it adjusts charge current to maintain the minimum system voltage and supply the load on SYS. If the charge current is reduced to zero and the load increases further, the bq2416xx enters battery-supplement mode. During supplement mode, the battery FET is turned on and the battery supplements the system load.

When an input is connected with no battery attached and termination enabled, the startup process proceeds as normal until the termination deglitch times out. After this, the bq2416xx enters battery detection and waits for a battery to be connected. Once a battery is connected and passes battery detection, a new charge cycle begins. Once the battery is applied, the HZMODE bit or $\overline{CD}$ pin must be toggled before writing the BATREG to a higher voltage and beginning a new charge cycle. Failure to do this can result in SYS unexpectedly regulating to 15% above V_{BATREG}.

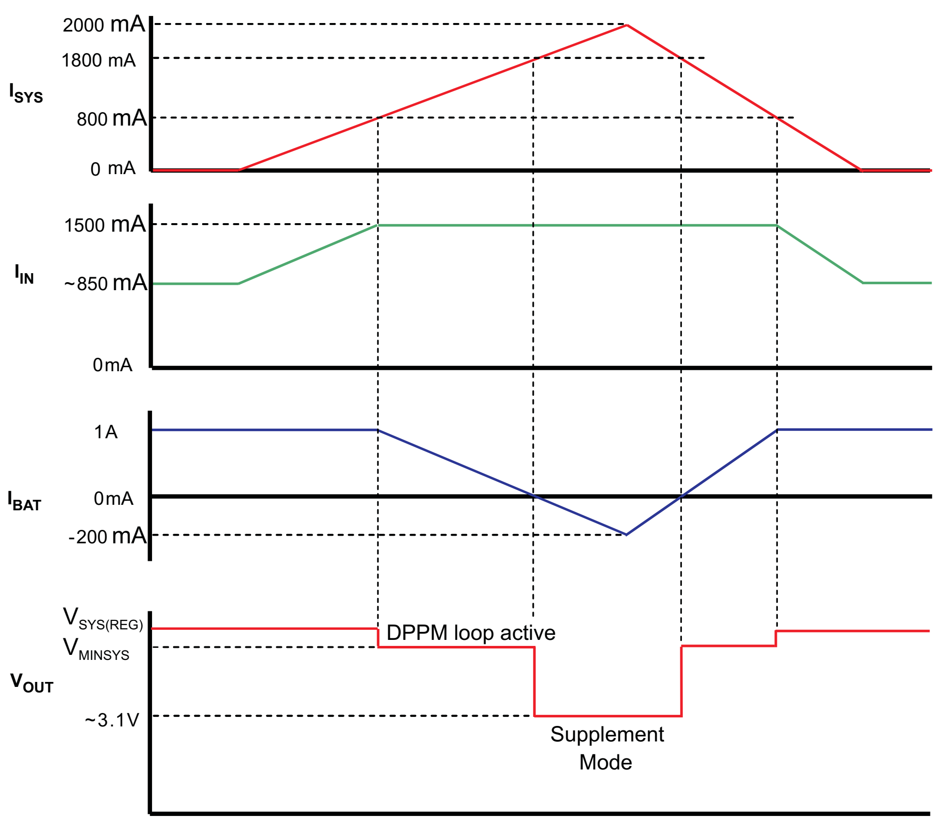


Figure 11. Example DPPM Response (V_{Supply}=5V, V_{BAT} = 3.1V, 1.5A Input Current Limit)

Feature Description (continued)

9.3.6 Battery Only Connected

When a battery with voltage greater than $V_{BATUVLO}$ is connected with no input source, the battery FET is turned on similar to supplement mode. In this mode, the current is not regulated; however, there is a short circuit current limit. If the short circuit limit is reached, the battery FET is turned off for the deglitch time ($t_{DGL(SC1)}$). After the recovery time ($t_{REC(SC1)}$), the battery FET is turned on to test and see if the short has been removed. If it has not, the FET turns off and the process repeats until the short is removed. This process is to protect the internal FET from over current. If an external FET is used for discharge, the external FET's body diode prevents the load on SYS from being disconnected from the battery. If the battery voltage is less than $V_{BATUVLO}$, the internal battery FET (Q4) remains off and BAT is high-impedance. This prevents further discharging of deeply-discharged batteries.

9.3.7 Battery Discharge FET (BGATE)

The bq2416xx contains a MOSFET driver to drive the gate of an external discharge FET between the battery and the system output. This external FET provides a low impedance path when supplying the system from the battery. Connect BGATE to the gate of the external discharge MOSFET. BGATE is on under the following conditions:

1. No input supply connected.
2. HZ_MODE bit = 1
3. $\overline{CD}$ pin = 1

9.3.8 DEFAULT Mode

DEFAULT mode is used when I^2C communication is not available. DEFAULT mode is entered in the following situations:

1. When the charger is enabled and $V_{BAT} < V_{BATGD}$ before I^2C communication is established
2. When the watchdog timer expires without a reset from the I^2C interface and the safety timer has not expired.
3. When the device comes out of any fault condition (sleep mode, OVP, faulty adapter mode, etc.) before I^2C communication is established

In DEFAULT mode, the I^2C registers are reset to the default values. The 27-minute safety timer (no timer for bq24168) is reset and starts when DEFAULT mode is entered. The default value for VBATREG is 3.6V, and the default value for I_{CHARGE} is 1A. The input current limit for the IN input is set to 1.5A. The input current limit for the USB input is determined by the D+/D– detection (bq24160/3) or PSEL (bq24161/1B/8). PSEL and D+/D– detection have no effect on the IN input. Default mode is exited by programming the I^2C interface. Once I^2C communication is established, PSEL has no effect on the USB input. Note that if termination is enabled and charging has terminated, a new charge cycle is NOT initiated when entering DEFAULT mode.

9.3.9 Safety Timer and Watchdog Timer (bq24160/ bq24161/ bq24161B/ bq24163 only)

At the beginning of charging process, the bq24160/1/1B/3 starts the safety timer. This timer is active during the entire charging process. If charging has not terminated before the safety timer expires, charging is disabled, the charge parameters are reset to the default values and the $\overline{CE}$ bit is written to a “1”. The length of the safety timer is selectable using the I^2C interface. A single 128μs pulse is sent on the STAT and INT outputs and the STATx bits of the status registers are updated in the I^2C. In DEFAULT mode, the safety timer can be reset and a new charge cycle initiated by input supply power on reset, removing/inserting battery or toggling the $\overline{CD}$ pin. In HOST mode, the $\overline{CE}$ bit is set to a '1' when the safety timer expires. The $\overline{CE}$ bit must be cleared to a '0' in order to resume charging and clear the safety timer fault. The safety timer duration is selectable using the TMR_X bits in the Safety Timer Register/ NTC Monitor register. Changing the safety timer duration resets the safety timer. This function prevents continuous charging of a defective battery. During the fast charge (CC) phase, several events increase the timer duration by 2X if the EN_2X_TMR bit is set in the register.

1. The system load current reduces the available charging current.
2. The input current needed for the fast charge current is limited by the input current loop.
3. The input current is reduced because the VINDPM loop is preventing the supply from crashing.
4. The device has entered thermal regulation because the IC junction temperature has exceeded TJ(REG).
5. The LOW_CHG bit is set.

Feature Description (continued)

6. The battery voltage is less than VBATSHORT.
7. The battery has entered the JEITA WARM or COLD state via the TS pin

During these events, the timer is slowed by half to extend the timer and prevent any false timer faults. Starting a new charge cycle by VSUPPLY POR or removing/replacing the battery or resuming a charge by toggling the CE or HZ_MODE bits, resets the safety timer. Additionally, thermal shutdown events cause the safety timer to reset.

In addition to the safety timer, the bq24160/1/1B/3 contain a watchdog timer that monitors the host through the I^2C interface. Once a read/write is performed on the I^2C interface, a 30-second timer ($t_{WATCHDOG}$) is started. The 30-second timer is reset by the host using the I^2C interface. This is done by writing a “1” to the reset bit (TMR_RST) in the control register. The TMR_RST bit is automatically set to “0” when the 30-second timer is reset. This process continues until the battery is fully charged or the safety timer expires. If the 30-second timer expires, the IC enters DEFAULT mode where the default register values are loaded, the safety timer restarts at 27 minutes and charging continues. The I^2C may be accessed again to reinitialize the desired values and restart the watchdog timer. The watchdog timer flow chart is shown in Figure 12.

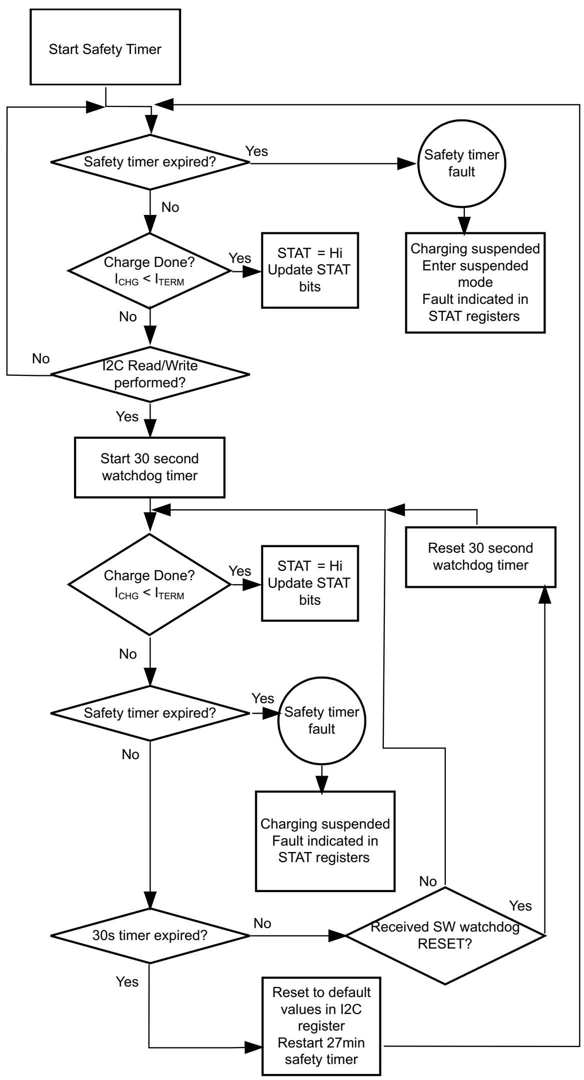


Figure 12. The Watchdog Timer Flow Chart for bq2416xx

Feature Description (continued)

9.3.10 D+, D– Based Adapter Detection for the USB Input (D+, D–, bq24160/0A/3)

The bq24160/0A/3 contain a D+, D– based adapter detection circuit that is used to program the input current limit for the USB input during DEFAULT mode. D+, D– detection is only performed in DEFAULT mode unless forced by the D+, D–_EN bit in host mode. Writing to register 2 during detection stops the detection routine.

By default the USB input current limit is set to 100mA. When a voltage higher than UVLO is applied to the USB input, the bq24160/0A/3 performs a charger source identification to determine if it is connected to an SDP (USB port) or CDP/DCP (dedicated charger). The first step is D+, D- line connection detection as described in BC1.2. Primary detection begins 10ms after the connection detection complete. The primary detection complies with the method described in BC1.2. During primary detection, the D+, D- lines are tested to determine if the port is an SDP or CDP/DCP. If a CDP/DCP is detected the input current limit is increased to 1.5A, if an SDP is detected the current limit remains at 100mA, until changed via the I^2C interface. These two steps require at least 90ms to complete but if they have not completed within 500ms, the D+, D- detection routine selects 100mA for the unknown input source. Secondary detection as described in BC1.2 is not performed.

Automatic detection is performed only if V_{D+} and V_{D-} are less than 0.6V to avoid interfering with the USB transceiver which may also perform D+, D– detection when the system is running normally. However, D+, D– can be initiated at any time by the host by setting the D+, D– EN bit in the Control/Battery Voltage Register to 1. After detection is complete the D+, D– EN bit is automatically reset to 0 and the detection circuitry is disconnected from the D+, D– pins to avoid interference with USB data transfer.

When a command is written to change the input current limit in the I^2C, this overrides the current limit selected by D+/D– detection. D+, D– detection has no effect on the IN input.

9.3.11 USB Input Current Limit Selector Input (PSEL, bq24161/ 161B/ 168 only)

The bq24161, bq24161B, and bq24168 contain a PSEL input that is used to program the input current limit for USB during DEFAULT mode. Drive PSEL high to indicate that a USB source is connected to the USB input and program the 100mA (bq24161/8) or 500mA (bq24161B) current limit for USB. Drive PSEL low to indicate that an AC Adapter is connected to the USB input. When PSEL is low, the IC starts up with a 1.5A current limit for USB. PSEL has no effect on the IN input. Once an I^2C write is done, the PSEL has no effect on the input current limit until the watchdog timer expires.

9.3.12 Hardware Chip Disable Input ($\overline{CD}$)

The bq2416xx contains a $\overline{CD}$ input that is used to disable the IC and place the bq2416xx into high-impedance mode. Drive $\overline{CD}$ low to enable charge and enter normal operation. Drive $\overline{CD}$ high to disable charge and place the bq2416xx into high-impedance mode. Driving $\overline{CD}$ high during DEFAULT mode resets the safety timer. Driving $\overline{CD}$ high during HOST mode resets the safety timer and places the bq2416xx into high impedance mode. The $\overline{CD}$ pin has precedence over the I^2C control.

9.3.13 LDO Output (DRV)

The bq2416xx contains a linear regulator (DRV) that is used to supply the internal MOSFET drivers and other circuitry. Additionally, DRV supplies up to 10mA external loads to power the STAT LED or the USB transceiver circuitry. The maximum value of the DRV output is 5.45V; ideal for protecting voltage sensitive USB circuits from high voltage fluctuations in the supply. The LDO is on whenever a supply is connected to the IN or USB inputs of the bq2416xx. The DRV is disabled under the following conditions:

1. V_{SUPPLY} < UVLO
2. V_{SUPPLY} < V_{SLP}
3. Thermal Shutdown

Feature Description (continued)

9.3.14 External NTC Monitoring (TS)

The I^2C interface allows the user to easily implement the JEITA standard for systems where the battery pack thermistor is monitored by the host. Additionally, the bq2416xx provides a flexible, voltage based TS input for monitoring the battery pack NTC thermistor. The voltage at TS is monitored to determine that the battery is at a safe temperature during charging. The bq24160, bq24160A, bq24161B, bq24163, and bq24168 enable the user to easily implement the JEITA standard for charging temperature while the bq24161 only monitors the hot and cold cutoff temperatures and leaves the JEITA control to the host. The JEITA specification is shown in.

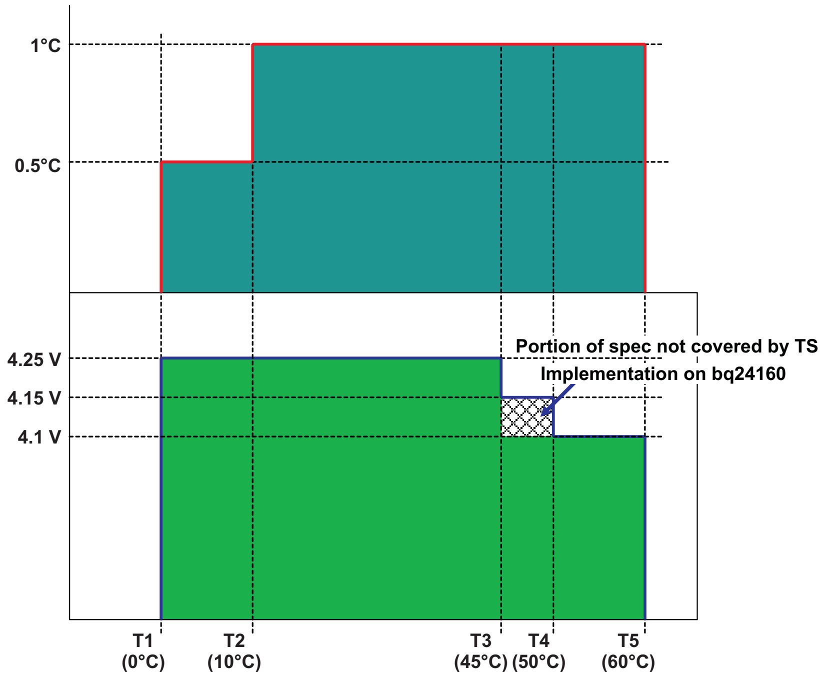


Figure 13. Charge Current During TS Conditions

To satisfy the JEITA requirements, four temperature thresholds are monitored; the cold battery threshold (T_{NTC} < 0°C), the cool battery threshold (0°C < T_{NTC} < 10°C), the warm battery threshold (45°C < T_{NTC} ≤ 60°C) and the hot battery threshold (T_{NTC} > 60°C). These temperatures correspond to the V_{COLD}, V_{COOL}, V_{WARM}, and V_{HOT} thresholds. Charging is suspended and timers are suspended when $V_{TS} < V_{HOT}$ or $V_{TS} > V_{COLD}$. When $V_{WARM} > V_{TS} > V_{HOT}$, the battery regulation voltage is reduced by 140mV from the programmed regulation threshold. When $V_{COLD} > V_{TS} > V_{COOL}$, the charging current is reduced to half of the programmed charge current.

The TS function is voltage based for maximum flexibility. Connect a resistor divider from DRV to GND with TS connected to the center tap to set the threshold. The connections are shown in Figure 20. The resistor values are calculated using the following equations:

$$RLO = \frac{V_{DRV} \times RCOLD \times RHOT \times \left[\frac{1}{V_{COLD}} - \frac{1}{V_{HOT}}\right]}{RHOT \times \left[\frac{V_{DRV}}{V_{HOT}} - 1\right] - RCOLD \times \left[\frac{V_{DRV}}{V_{COLD}} - 1\right]} \quad (1)$$

$$RHI = \frac{\frac{V_{DRV}}{V_{COLD}} - 1}{\frac{1}{RLO} + \frac{1}{RCOLD}} \quad (2)$$

Where:

$V_{COLD} = 0.60 \times V_{DRV}$

Feature Description (continued)

$V_{HOT} = 0.30 \times V_{DRV}$

Where R_{HOT} is the NTC resistance at the hot temperature and R_{COLD} is the NTC resistance at cold temperature.

For the bq24160, bq24161B, bq24163, and bq24168, the WARM and COOL thresholds are not independently programmable. The COOL and WARM NTC resistances for a selected resistor divider are calculated using the following equations:

$$RCOOL = \frac{RLO \times 0.564 \times RHI}{RLO - RLO \times 0.564 - RHI \times 0.564} \tag{3}$$

$$RWARM = \frac{RLO \times 0.383 \times RHI}{RLO - RLO \times 0.383 - RHI \times 0.383} \tag{4}$$

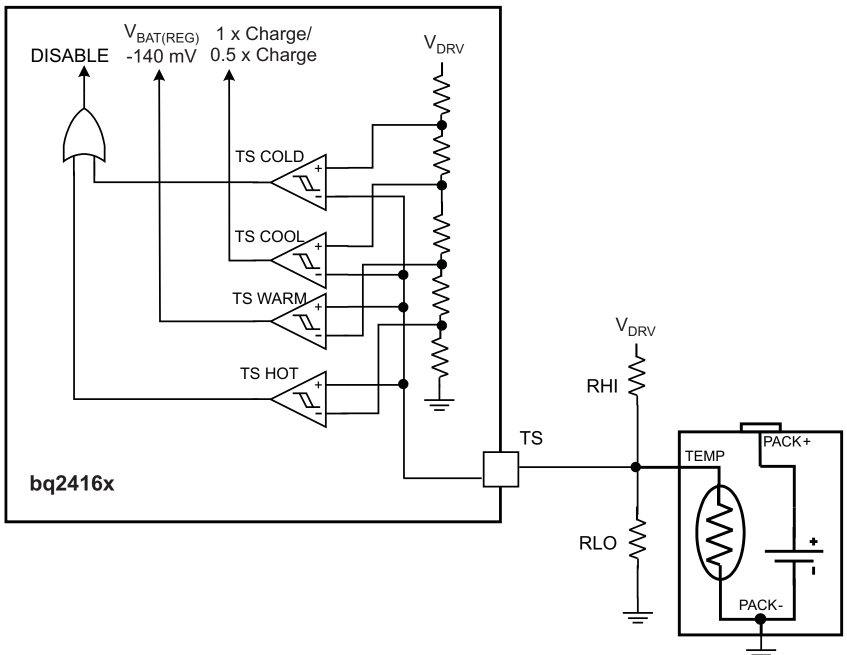


Figure 14. TS Circuit

9.3.15 Thermal Regulation and Protection

During the charging process, to prevent chip overheating, the bq2416xx monitors the junction temperature, T_J, of the die and begins to taper down the charge current once T_J reaches the thermal regulation threshold, T_{REG}. The charge current is reduced to zero when the junction temperature increases about 10°C above T_{REG}. Once the charge current is reduced, the system current is reduced while the battery supplements the load to supply the system. This may cause a thermal shutdown of the bq2416xx if the die temperature rises too high. At any state, if T_J exceeds T_{SHTDWN}, the bq2416xx suspends charging and disables the buck converter. During thermal shutdown mode, the buck converter is turned off, all timers are suspended, and a single 128μs pulse is sent on the STAT and INT outputs and the STATx and FAULT_x bits of the status registers are updated in the I^2C. A new charging cycle begins when T_J falls below T_{SHTDWN} by approximately 10°C.

Feature Description (continued)

9.3.16 Input Voltage Protection in Charge Mode

9.3.16.1 Sleep Mode

The bq2416xx enters the low-power sleep mode if the voltage on V_{SUPPLY} falls below the sleep-mode entry threshold, V_{BAT}+V_{SLP}, and V_{SUPPLY} is higher than the undervoltage lockout threshold, V_{UVLO}. This feature prevents draining the battery during the absence of V_{SUPPLY}. When V_{SUPPLY} < V_{BAT}+ V_{SLP}, the bq2416xx turns off the PWM converter, turns the battery FET on and drives BGATE to GND, sends a single 128μs pulse on the STAT and INT outputs and updates the STATx and FAULT_x bits in the status registers. Once V_{SUPPLY} > V_{BAT}+ V_{SLP}, the STATx and FAULT_x bits are cleared and the device initiates a new charge cycle.

9.3.16.2 Input Voltage Based DPM

During normal charging process, if the input power source is not able to support the programmed or default charging current, the supply voltage decreases. Once the supply drops to V_{IN_DPM} (default 4.2V for both inputs), the input current limit is reduced to prevent further supply droop. When the IC enters this mode, the charge current is lower than the set value and the DPM_STATUS bit is set (Bit 5 in Register 05H). This feature provides IC compatibility with adapters with different current capabilities without a hardware change. Figure 15 shows the $V_{IN_}$DPM behavior to a current-limited source. In this figure the input source has a 750mA current limit and the charging is set to 750mA. The SYS load is then increased to 1.2A.

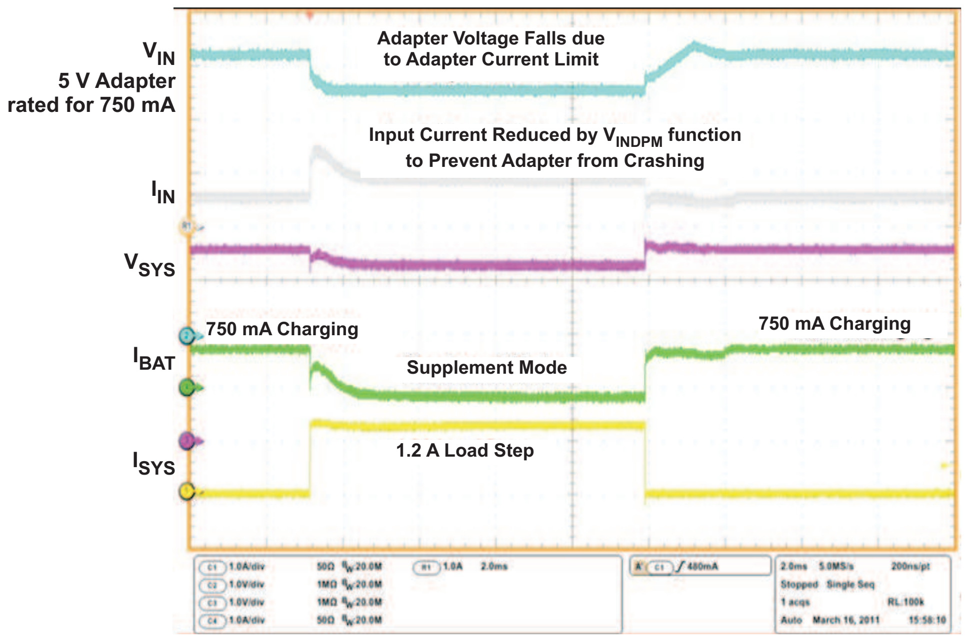


Figure 15. bq24160 V_{IN}-DPM

9.3.16.3 Bad Source Detection

When a source is connected to IN or USB, the bq2416xx runs a Bad Source Detection procedure to determine if the source is strong enough to provide some current to charge the battery. A current sink is turned on (30mA for USB input, 75mA for the IN input) for 32ms. If the source is valid after the 32ms ($V_{BADSOURCE}$ < V_{SUPPLY} < V_{OVP}), the buck converter starts up and normal operation continues. If the supply voltage falls below V_{BAD_SOURCE} during the detection, the current sink shuts off for two seconds and then retries, a single 128μs pulse is sent on the STAT and INT outputs and the STATx and FAULT_x bits of the status registers and the battery/supply status registers are updated. The detection circuits retry continuously until either a new source is connected to the other input or a valid source is detected after the detection time. If during normal operation the source falls to V_{BAD_SOURCE}, the bq2416xx turns off the PWM converter, turns the battery FET on, sends a single 128μs pulse is sent on the STAT and INT outputs and the STATx and FAULT_x bits of the status registers, and the battery/supply status registers are updated. Once a good source is detected, the STATx and FAULT_x bits are cleared and the device returns to normal operation.

Feature Description (continued)

If two supplies are connected, the supply with precedence is checked first. If the supply detection fails once, the device switches to the other supply for two seconds and then retries. This allows the priority supply to settle if the connection was jittery or the supply ramp was too slow to pass detection. If the priority supply fails the detection a second time, it is locked out and lower priority supply is used. Once the bad supply is locked out, it remains locked out until the supply voltage falls below UVLO. This prevents continuously switching between a weak supply and a good supply.

9.3.16.4 Input Overvoltage Protection

The built-in input overvoltage protection to protect the device and other downstream components against damage from overvoltage on the input supply (Voltage from V_{USB} or V_{IN} to PGND). During normal operation, if $V_{SUPPLY} > V_{OVP}$, the bq2416xx turns off the PWM converter, turns the battery FET and BGATE on, sends a single 128μs pulse is sent on the STAT and INT outputs and the STATx and FAULT_x bits of the status registers and the battery/supply status registers are updated. Once the OVP fault is removed, the STATx and FAULT_x bits are cleared and the device returns to normal operation.

To allow operation with some unregulated adapters, the OVP circuit is not active during Bad Source Detection. This provides some time for the current sink to pull the unregulated adapter down into an acceptable range. If the adapter voltage is high at the end of the detection, the startup of the PWM converter does not occur. The OVP circuit is active during normal operation, so if the system standby current plus the charge current is not enough to pull down the source, operation is suspended.

9.3.16.5 Reverse Boost (Boost Back) Prevention Circuit

A buck converter has two operating modes, continuous conduction mode (CCM) and discontinuous conduction mode (DCM). In DCM, the inductor current ramps down to zero during the switching cycle while in CCM the inductor maintains a DC level of current. Transitioning from DCM to CCM during load transients, slows down the converter's transient response for those load steps, which can result in the SYS rail drooping. To achieve the fastest possible transient reponse for this charger, this charger's synchronous buck converter is forced to run in CCM even at light loads when the buck converter would typically revert to DCM. The challenge that presents itself when forcing CCM with a charger is that the output of the buck converter now has a power source. Thus, if the battery voltage, V(BAT), is ever greater than V_{BATREG}, the inductor current goes fully negative and pushes current back to the input supply. This effect causes the input source voltage to rise if the input source cannot sink current. The input over-voltage protection circuit protects the IC from damage however some input sources may be damaged if the voltage rises. To prevent this, this charger has implemented a reverse boost prevention circuit. When reverse current is sensed that is not a result of the supplement comparator tripping, this circuit disables the internal battery FET and changes the feedback point to V_{SYSREG} for 1 ms. After the 1-ms timeout, the BATFET is turned on again and the battery is tested to see if it is higher than V_{BATREG} (negative current). The reverse current protection is only active when $V_{BOVP} > V_{BAT} > V_{BATREG} - V_{RCH}$. Having $V_{BOVP} > V_{BAT} > V_{BATREG} - V_{RCH}$ results in an approximately 100-mV, 1000-Hz ripple on SYS as seen in . The most common trigger for reverse boost prevention is a load transient on SYS that requires the charger to enter battery supplement mode. When the IC enters reverse boost prevention, the IC stops charging or exits charge done which may result in the battery never reaching full charge. With termination enabled and ITERM > 150mA or with a high line impedance to the battery, the likelihood of activating the reverse boost prevention circuit is small and even when activated, the charger typically exits reverse boost prevention as the battery relaxes. With termination enabled and ITERM < 150mA or with a low impedance battery, the likelihood of activating the reverse boost prevention circuit by a load transient or even the inductor ripple current is higher. In either case, the IC resumes charging until VBAT drops below VBATREG - VRCH, resulting in the battery always charging to at least 0.97 of full charge. If full charge is required with ITERM < 150mA then the recommended solution to ensure full charge is as follows

1. SET the charger’s enable no battery operation bit (EN_NOBATOP) = 1 to disable the reverse boost prevention circuits. Brief, low-amplitude voltage pulses on IN may be observed as the IC enters boost back to resolve instances where VBAT is greater than the VBATREG, for example when exiting supplement mode. The I2C communication software must ensure that VBATREG is never written below VBAT. The IC automatically rewrites the VBATREG register to the default value of 3.6V when existing HOST mode. For JEITA enabled ICs, the IC automatically lowers the voltage reference to 0.98 of the VBATREG value. The software must account for these instances as well.
2. Disable the charger’s termination function and TS functions and use a gas gauge to control termination and TS through its independent voltage and current measurements.

Feature Description (continued)

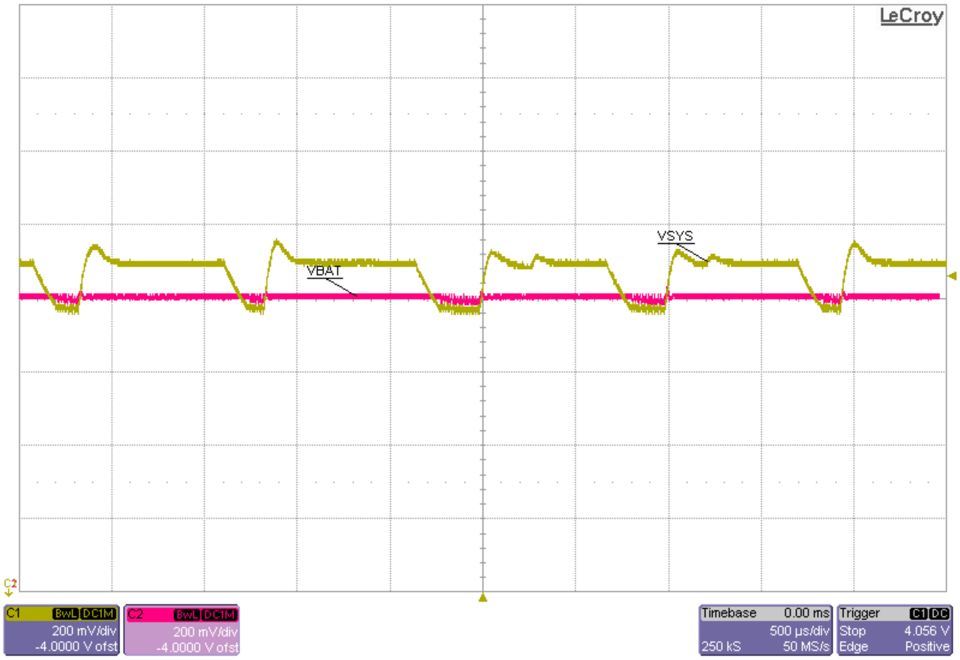


Figure 16. V(SYS) when Reverse Boost Prevention Circuit is Active

9.3.17 Charge Status Outputs (STAT, INT)

The STAT output is used to indicate operation conditions for bq2416xx. STAT is pulled low during charging when EN_STAT bit in the control register (0x02h) is set to “1”. When charge is complete or disabled, STAT is high impedance. When a fault occurs, a 128-μs pulse (interrupt) is sent out to notify the host. The status of STAT during different operation conditions is summarized in Table 1. STAT drives an LED for visual indication or can be connected to the logic rail for host communication. The EN_STAT bit in the control register (00H) is used to enable/disable the charge status for STAT. The interrupt pulses are unaffected by EN_STAT and will always be shown. The INT output is identical to STAT and is used to interface with a low voltage host processor.

Table 1. STAT Pin Summary

Charge State	STAT and INT behavior
Charge in progress and EN_STAT=1	Low
Other normal conditions	High-Impedance
Status Changes: Supply Status Change (plug in or removal), safety timer fault, watchdog expiration, sleep mode, battery temperature fault (TS), battery fault (OVP or absent), thermal shutdown	128-μs pulse, then High Impedance

9.3.18 Good Battery Monitor

The bq2416xx contains a good battery monitor circuit that places the bq2416xx into high-z mode if the battery voltage is above the BATGD threshold while in DEFAULT mode. This function is used to enable compliance to the battery charging standard that prevents charging from an un-enumerated USB host while the battery is above the good battery threshold. If the bq2416xx is in HOST mode, it is assumed that USB host has been enumerated and the good battery circuit has no effect on charging.

9.4 Device Functional Modes

The state machine of the bq2416x automatically changes primary states (Off, sleep, HiZ, charge disabled, charging, charge done, battery OVP, fault) based on data in the I2C registers, IN and USB pin voltages, BAT pin voltage and current flow, TS pin voltage, $\overline{CD}$ pin voltage and status of the safety timer. The BAT and TS pin voltages as well as current flow into the IN and USB pins, out of SYS pin and into/out of the BAT pin determine the charging sub-states, including conditioning, constant current (CC), CC with reduced charge current, constant voltage (CV) with reduced charge current.

9.5 Programming

9.5.1 Serial Interface Description

The bq2416xx uses an I^2C-compatible interface to program charge parameters. I^2C is a 2-wire serial interface developed by Philips Semiconductor (see I^2C-Bus Specification, Version 2.1, January 2000). The bus consists of a data line (SDA) and a clock line (SCL) with pull-up structures. When the bus is idle, both SDA and SCL lines are pulled high. All I^2C-compatible devices connect to the I^2C bus through open drain I/O pins, SDA and SCL. A master device, usually a microcontroller or a digital signal processor, controls the bus. The master is responsible for generating the SCL signal and device addresses. The master also generates specific conditions that indicate the START and STOP of data transfer. A slave device receives and/or transmits data on the bus under control of the master device.

The bq2416xx device works as a slave and supports the following data transfer modes, as defined in the I^2C Bus Specification: standard mode (100kbps) and fast mode (400kbps). The interface adds flexibility to the battery charging solution, enabling most functions to be programmed to new values depending on the instantaneous application requirements. Register contents remain intact as long as battery voltage remains above 2.5V (typical). The I^2C circuitry is powered from VBUS when a supply is connected. If the VBUS supply is not connected, the I^2C circuitry is powered from the battery through BAT. The battery voltage must stay above 2.5V with no input connected in order to maintain proper operation.

The data transfer protocol for standard and fast modes is exactly the same; therefore, they are referred to as the F/S-mode in this document. The bq2416xx devices only support 7-bit addressing. The device 7-bit address is defined as ‘1101011’ (6Bh).

9.5.1.1 F/S Mode Protocol

The master initiates data transfer by generating a start condition. The start condition is when a high-to-low transition occurs on the SDA line while SCL is high, as shown in Figure 17. All I^2C-compatible devices should recognize a start condition.

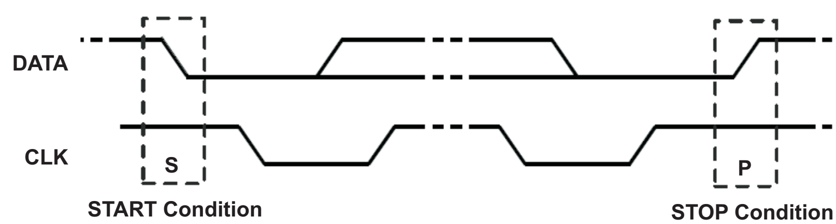


Figure 17. START and STOP Condition

The master then generates the SCL pulses, and transmits the 8-bit address and the read/write direction bit R/W on the SDA line. During all transmissions, the master ensures that data is valid. A valid data condition requires the SDA line to be stable during the entire high period of the clock pulse (see Figure 18). All devices recognize the address sent by the master and compare it to their internal fixed addresses. Only the slave device with a matching address generates an acknowledge (see Figure 19) by pulling the SDA line low during the entire high period of the ninth SCL cycle. Upon detecting this acknowledge, the master knows that communication link with a slave has been established.

Programming (continued)

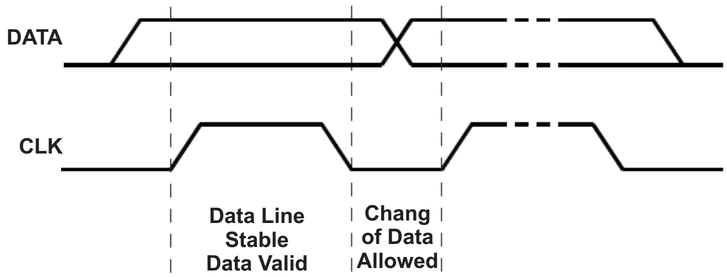


Figure 18. Bit Transfer on the Serial Interface

The master generates further SCL cycles to either transmit data to the slave (R/W bit 1) or receive data from the slave (R/W bit 0). In either case, the receiver needs to acknowledge the data sent by the transmitter. So an acknowledge signal can either be generated by the master or by the slave, depending on which one is the receiver. The 9-bit valid data sequences consisting of 8-bit data and 1-bit acknowledge can continue as long as necessary. To signal the end of the data transfer, the master generates a stop condition by pulling the SDA line from low to high while the SCL line is high (see Figure 20). This releases the bus and stops the communication link with the addressed slave. All I^2C compatible devices must recognize the stop condition. Upon the receipt of a stop condition, all devices know that the bus is released, and wait for a start condition followed by a matching address. If a transaction is terminated prematurely, the master needs sending a STOP condition to prevent the slave I^2C logic from remaining in an incorrect state. Attempting to read data from register addresses not listed in this section result in FFh being read out.

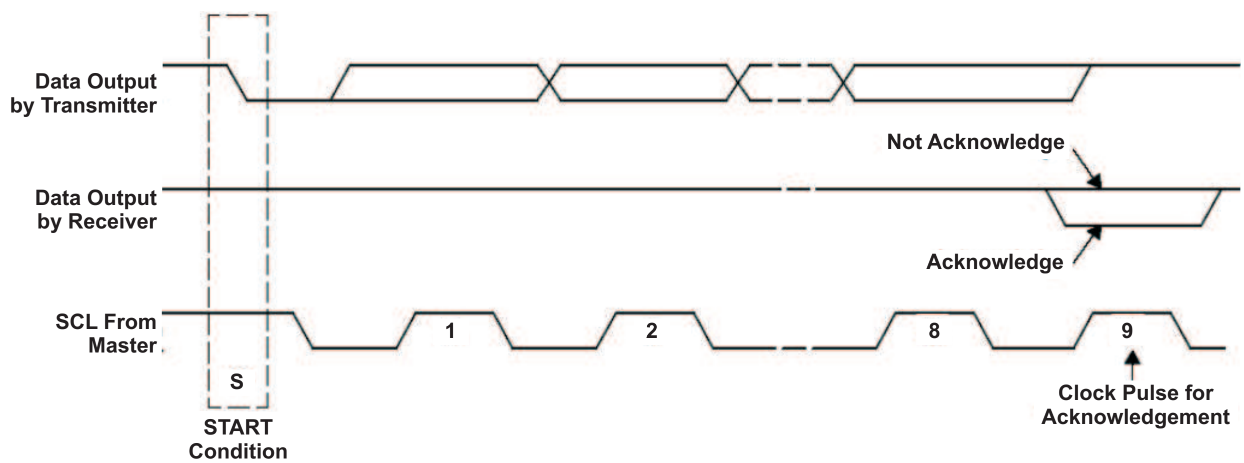


Figure 19. Acknowledge on the I2C Bus

Programming (continued)

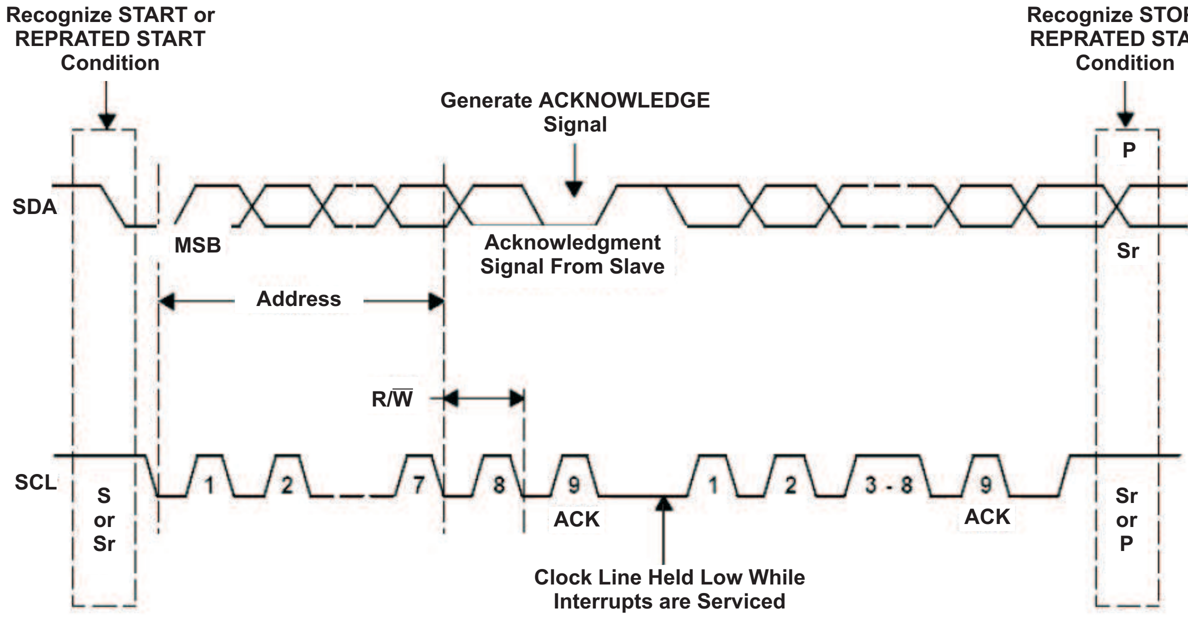


Figure 20. Bus Protocol

9.6 Register Maps

9.6.1 Status/Control Register (READ/WRITE)

Memory location: 00, Reset state: 0xxx 0xxx

BIT	NAME	Read/Write	FUNCTION
B7 (MSB)	TMR_RST	Read/Write	Write: TMR_RST function, write “1” to reset the watchdog timer (auto clear) Read: Always 0 (bq24160/1/3 only)
B6	STAT_2	Read only	000- No Valid Source Detected 001- IN Ready (shows preferred source when both connected) 010- USB Ready (shows preferred source when both connected) 011- Charging from IN 100- Charging from USB 101- Charge Done 110- NA 111- Fault
B5	STAT_1	Read only	
B4	STAT_0	Read only	
B3	SUPPLY_SEL	Read/Write	0-IN has precedence when both supplies are connected 1-USB has precedence when both supplies are connected (default 0)
B2	FAULT_2	Read only	000-Normal 001- Thermal Shutdown 010- Battery Temperature Fault 011- Watchdog Timer Expired (bq24160/1/1B/3 only) 100- Safety Timer Expired (bq24160/1/1B/3 only) 101- IN Supply Fault 110- USB Supply Fault 111- Battery Fault
B1	FAULT_1	Read only	
B0 (LSB)	FAULT_0	Read only	

SUPPLY_SEL Bit (Supply Precedence Selector)

The SUPPLY_SEL bit selects which supply has precedence when both supplies are present. In cases where both supplies are connected, they must remain isolated from each other which means only one is allowed to charge the battery. Write a “1” to SUPPLY_SEL to select the USB input to have precedence. Write a “0” to select the IN input.Note the following behavior when switching the SUPPLY_SEL bit with both supplies attached:

- The bq2416xx returns to high impedance mode
- The input supply is switched
- The bq2416xx begins a full startup cycle starting with bad adapter detection then proceeding to soft-start

Similarly, if charging from the non-preferred supply when the preferred supply is attached, the bq2416xx follows the same procedure.

STAT_x and FAULT_x Bits

The STAT_x show the current status of the device and are updated dynamically as the IC changes state. The FAULT_x bits show faults that have occurred and are only cleared by reading the bits, assuming the fault no longer exists. If multiple faults occur, the first one is the one that is shown.

9.6.2 Battery/ Supply Status Register (READ/WRITE)

Memory location: 01, Reset state: xxxx 0xxx

BIT	NAME	Read/Write	FUNCTION
B7 (MSB)	INSTAT1	Read Only	00-Normal 01-Supply OVP 10-Weak Source Connected (No Charging) 11- $V_{IN}<V_{UVLO}$
B6	INSTAT0	Read Only	
B5	USBSTAT1	Read Only	00-Normal 01-Supply OVP 01-Weak Source Connected (No Charging) 11- $V_{USB}<V_{UVLO}$
B4	USBSTAT0	Read Only	

BIT	NAME	Read/Write	FUNCTION
B3	OTG_LOCK	Read/Write	0 – No OTG supply present. Use USB input as normal. 1 – OTG supply present. Lockout USB input for charging. (default 0)
B2	BATSTAT1	Read Only	00-Battery Present and Normal 01-Battery OVP 10-Battery Not Present 11- NA
B1	BATSTAT0	Read Only	
B0 (LSB)	EN_NOBATOP	Read/ Write	0-Normal Operation 1-Enables No Battery Operation when termination is disabled (default 0)

OTG_LOCK Bit (USB Lockout)

The OTG_LOCK bit is used to prevent any charging from USB input regardless of the SUPPLY_SEL bit and IN supply status. For systems using OTG supplies, it is not desirable to charge from an OTG source. Doing so would mean draining the battery by allowing it to effectively charge itself. Write a “1” to OTG_LOCK to lock out the USB input. Write a “0” to OTG_LOCK to return to normal operation. During OTG lock, the USB input is ignored and DRV does not come up. The watchdog timer must be reset while in USB_LOCK to maintain the USB lockout state. This prevents the USB input from being permanently locked out for cases where the host loses I2C communication with OTG_LOCK set (i.e., discharged battery from OTG operation). See the *Safety Timer and Watchdog Timer* section for more details.

EN_NOBATOP (No Battery Operation)

The EN_NOBATOP bit enables no battery operation. When using the bq2416x without a battery attached, it is recommended to first disable charging, then disable charge termination and finally set this bit to 1. Setting this bit to 1 also disables the reverse boost prevention circuit and the BATOVP circuit. With a battery attached, setting this bit to 1 may be helpful to ensure full battery charging as explained in the reverse battery prevention circuit section. In the event of battery overvoltage (e.g., recovery from large SYS load transient requiring supplement), the BATOVP protection circuit turns off the buck converter to allow the battery to discharge through SYS.

9.6.3 Control Register (READ/WRITE)

Memory location: 02, Reset state: 1000 1100

BIT	NAME	Read/Write	FUNCTION
B7 (MSB)	RESET	Write only	Write: 1 – Reset all registers to default values 0 – No effect Read: always get “1”
B6	IUSB_LIMIT_2	Read/Write	000 – USB2.0 host with 100mA current limit 001 – USB3.0 host with 150mA current limit 010 – USB2.0 host with 500mA current limit 011 – USB host/charger with 800mA current limit 100 – USB3.0 host with 900mA current limit 101 – USB host/charger with 1500mA current limit 110–111 – NA (default 000[(1)])
B5	IUSB_LIMIT_1	Read/Write	
B4	IUSB_LIMIT _0	Read/Write	
B3	EN_STAT	Read/Write	1 – Enable STAT output to show charge status, 0-Disable STAT output for charge status. Fault interrupts are still show even when EN_STAT = 0. (default 1)
B2	TE	Read/Write	1 – Enable charge current termination, 0-Disable charge current termination (default 1)
B1	$\overline{CE}$	Read/Write	1 – Charging is disabled 0 – Charging enabled (default 0 bq24160/1/1B/3/8)
B0 (LSB)	HZ_MODE	Read/Write	1 – High impedance mode 0 – Not high impedance mode (default 0)

(1) When in DEFAULT mode, the D+/D– (bq24160) or PSEL (bq24161/8) inputs determine the input current limit for the USB input.

RESET Bit

The RESET bit in the control register (0x02h) is used to reset all the charge parameters. Write “1” to RESET bit to reset all the registers to default values and place the bq2416xx into DEFAULT mode and turn off the watchdog timer. The RESET bit is automatically cleared to zero once the bq2416xx enters DEFAULT mode.

$\overline{\text{CE}}$ Bit (Charge Enable)

The $\overline{\text{CE}}$ bit in the control register (0x02h) is used to disable or enable the charge process. A low logic level (0) on this bit enables the charge and a high logic level (1) disables the charge. When charge is disabled, the SYS output regulates to VSYS(REG) and battery is disconnected from the SYS. Supplement mode is still available if the system load demands cannot be met by the supply.

HZ_MODE Bit (High Impedance Mode Enable)

The HZ_MODE bit in the control register (0x02h) is used to disable or enable the high impedance mode. A low logic level (0) on this bit enables the IC and a high logic level (1) puts the IC in a low quiescent current state called high impedance mode. When in high impedance mode, the converter is off and the battery FET and BGATE are on. The load on SYS is supplied by the battery.

9.6.4 Control/Battery Voltage Register (READ/WRITE)

Memory location: 03, Reset state: 0001 0100

BIT	NAME	Read/Write	FUNCTION
B7 (MSB)	V_{BREG5}	Read/Write	Battery Regulation Voltage: 640 mV (default 0)
B6	V_{BREG4}	Read/Write	Battery Regulation Voltage: 320 mV (default 0)
B5	V_{BREG3}	Read/Write	Battery Regulation Voltage: 160 mV (default 0)
B4	V_{BREG2}	Read/Write	Battery Regulation Voltage: 80 mV (default 1)
B3	V_{BREG1}	Read/Write	Battery Regulation Voltage: 40 mV (default 0)
B2	V_{BREG0}	Read/Write	Battery Regulation Voltage: 20 mV (default 1)
B1	$I_{INLIMIT}$	Read/Write	Input Limit for IN input- 0 – 1.5A 1 – 2.5A (default 0)
B0 (LSB)	D+/D–_EN	Read/Write	0 – Normal state, D+/D- Detection done 1 – Force D+/D– Detection. Returns to “0” after detection is done. (default 0)

- Charge voltage range is 3.5V–4.44V with the offset of 3.5V and step of 20mV (default 3.6V).
- Before writing to increase VBATREG register following a BATOVP event (e.g., IN or USB voltage is applied, IC remains in DEFAULT mode and then VBAT>3.6V is attached), toggle the HiZ bit or CD pin to clear the BATOVP fault.

9.6.5 Vender/Part/Revision Register (READ only)

Memory location: 04, Reset state: 0100 0000

BIT	NAME	Read/Write	FUNCTION
B7 (MSB)	Vender2	Read only	Vender Code: bit 2 (default 0)
B6	Vender1	Read only	Vender Code: bit 1 (default 1)
B5	Vender0	Read only	Vender Code: bit 0 (default 0)
B4	PN1	Read only	For I^2C Address 6Bh: 00: bq2416xx 01–11: Future product spins
B3	PN0	Read only	

BIT	NAME	Read/Write	FUNCTION
B2	Revision2	Read only	000: Revision 1.0 001: Revision 1.1 010: Revision 2.0 011: Revision 2.1 100: Revision 2.2 101: Revision 2.3 110-111: Future Revisions
B1	Revision1	Read only	
B0 (LSB)	Revision0	Read only	

9.6.6 Battery Termination/Fast Charge Current Register (READ/WRITE)

Memory location: 05, Reset state: 0011 0010

BIT	NAME	Read/Write	FUNCTION
B7 (MSB)	I_{CHRG4}	Read/Write	Charge current: 1200mA – (default 0)
B6	I_{CHRG3}	Read/Write	Charge current: 600mA – (default 0)
B5	I_{CHRG2}	Read/Write	Charge current: 300mA – (default 1)
B4	I_{CHRG1}	Read/Write	Charge current: 150mA – (default 1)
B3	I_{CHRG0}	Read/Write	Charge current: 75 mA (default 0)
B2	I_{TERM2}	Read/Write	Termination current sense voltage: 200mA (default 0)
B1	I_{TERM1}	Read/Write	Termination current sense voltage: 100mA (default 1)
B0 (LSB)	I_{TERM0}	Read/Write	Termination current sense voltage: 50mA (default 0)

- Charge current sense offset is 550mA and default charge current is 1000mA.
- Termination threshold offset is 50mA and default termination current is 150mA

9.6.7 V_{IN-DPM} Voltage/ DPPM Status Register

Memory location: 06, Reset state: xx00 0000

BIT	NAME	Read/Write	FUNCTION
B7(MSB)	MINSYS_STATUS	Read Only	1 – Minimum System Voltage mode is active (V_{BAT}<V_{MINSYS}) 0 – Minimum System Voltage mode is not active
B6	DPM_STATUS	Read Only	1 – V_{IN}-DPM mode is active 0 – V_{IN}-DPM mode is not active
B5	$V_{INDPM2(USB)}$	Read/Write	USB input V_{IN-DPM} voltage: 320mV (default 0)
B4	$V_{INDPM1(USB)}$	Read/Write	USB input V_{IN-DPM} voltage: 160mV (default 0)
B3	$V_{INDPM0(USB)}$	Read/Write	USB input V_{IN-DPM} voltage: 80mV (default 0)
B2	$V_{INDPM2(IN)}$	Read/Write	IN input V_{IN-DPM} voltage: 320mV (default 0)
B1	$V_{INDPM1(IN)}$	Read/Write	IN input V_{IN-DPM} voltage: 160mV (default 0)
B0(LSB)	$V_{INDPM0(IN)}$	Read/Write	IN input V_{IN-DPM} voltage: 80mV (default 0)

- V_{IN-DPM} voltage offset is 4.20V and default V_{IN-DPM} threshold is 4.20V.

9.6.8 Safety Timer/ NTC Monitor Register (READ/WRITE)

Memory location: 07, Reset state: 1001 1xxx

BIT	NAME	Read/Write	FUNCTION
B7 (MSB)	2XTMR_EN	Read/Write	1 – Timer slowed by 2x when in thermal regulation, input current limit, V_{IN_DPM} or DPPM 0 – Timer not slowed at any time (default 0) (bq24160/1 only)
B6	TMR_1	Read/Write	Safety Timer Time Limit – 00 – 27 minute fast charge 01 – 6 hour fast charge 10 – 9 hour fast charge 11 – Disable safety timers (default 00) (bq24160/1 only)
B5	TMR_2	Read/Write	
B4	NA	Read/Write	NA

BIT	NAME	Read/Write	FUNCTION
B3	TS_EN	Read/Write	0 – TS function disabled 1 – TS function enabled (default 1)
B2	TS_FAULT1	Read only	TS Fault Mode: 00 – Normal, No TS fault 01 – TS temp < T_{COLD} or TS temp > T_{HOT}(Charging suspended) 10 – T_{COOL} > TS temp > T_{COLD} (Charge current reduced by half, bq24160 only) 11 – T_{WARM} < TS temp < T_{HOT} (Charge voltage reduced by 140mV, bq24160 only)
B1	TS_FAULT0	Read only	
B0 (LSB)	LOW_CHG	Read/ Write	0 – Charge current as programmed in Register 0x05 1 – Charge current is half programmed value in Register 0x05 (default 0)

2xTMR_EN Bit (2x Timer Enable)

The 2xTMR_EN bit is used to slow down the timer when charge current is reduced by the system load. When 2xTMR_EN is a "1", the safety timer is slowed to half speed effectively doubling the timer time. The conditions that activate the 2x timer are: Input Current Limit, V_{INDPM}, Thermal Regulation, LOW_CHG, BATSHRT and TS Cool. When 2xTMR_EN is a "0", the timer operates at normal speed in all conditions.

LOW_CHG Bit (Low Charge Mode Enable)

The LOW_CHG bit is used to reduce the charge current from the programmed value. This feature is used by systems where battery NTC is monitored by the host and requires a reduced charge current setting or by systems that need a “preconditioning” current for low battery voltages. Write a “1” to this bit to charge at half of the programmed charge current (bq24160/1/3/8). Write a “0” to this bit to charge at the programmed charge current.

10 Application and Implementation

10.1 Application Information

A typical application circuit using the bq24160 with a smartphone's GSM power amplifier (PA) powered directly from the battery is shown in Figure 21. A typical application circuit using the bq24161 with a smartphone's GSM PA powered from the SYS rail, to allow for calls even with a deeply discharged battery, is shown in Figure 22. Each circuit shows the minimum capacitance requirements for each pin and typical recommended inductance value of 1.5 µH. The TS resistor divider for configuring the TS function for the battery's specific thermistor can be computed from equations Equation 1 and Equation 2. The resistor on STAT is sized per the LED current requirements. All other configuration settings for VINDPM, input current limit, charge current and charge voltage are made in EEPROM registers using I2C commands. Options for sizing the inductor outside the 1.5 µH recommended value and additional SYS pin capacitance are explained in the next section.

10.2 Typical Application

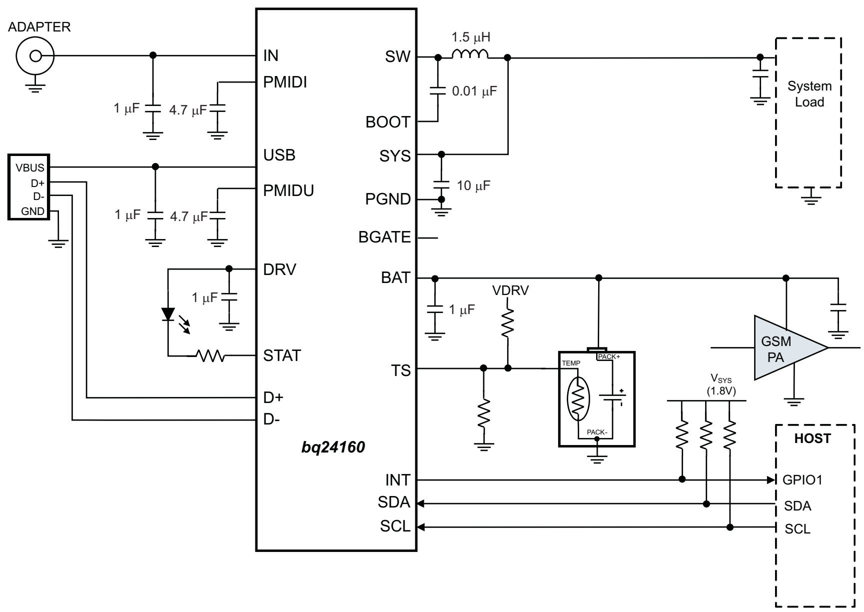


Figure 21. bq24160, Shown with no External Discharge FET, PA Connected to Battery

Typical Application (continued)

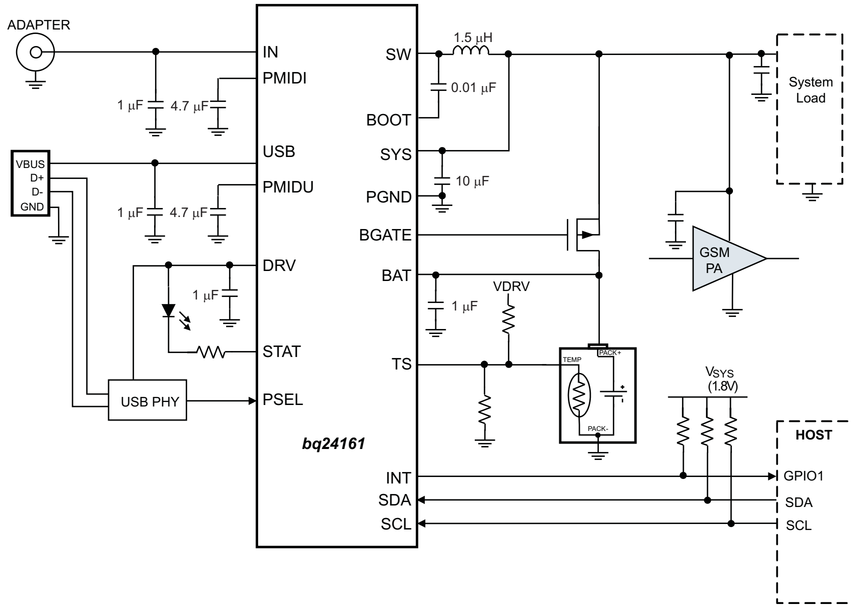


Figure 22. bq24161, Shown with External Discharge FET, PA Connected to System for GSM Call Support with a Deeply Discharged or No Battery

10.2.1 Design Requirements

		Min	Typ	Max	Unit
Supply voltage, V_{IN}	Input voltage from ac adapter	4.2		10	V
USB voltage, V_{USB}	Input voltage from USB or equivalent supply	4.2		6	V
System voltage, V_{SYS}	Voltage output at SYS terminal (depends on VBAT voltage and status of V_{INDPM})	3.3		VBATREG+4.17%	V
Battery voltage, V_{BAT}	Voltage output at VBAT terminal (registers set via I2C communication)	2	4.2	4.44	V
Supply current, $I_{IN(MAX)}$	Maximum input current from ac adapter input (registers set via I2C communication)	1.5		2.5	A
Supply current, $I_{USB(MAX)}$	Maximum input current from USB input (registers set via I2C communication)	0.1	0.5	1.5	A
Fast charge current, $I_{CHRG(MAX)}$	Battery charge current (registers set via I2C communication)	0.550		2.5	A
Operating junction temperature range, T_J		-40		125	°C

10.2.2 Detailed Design Procedure

10.2.2.1 Output Inductor and Capacitor Selection Guidelines

When selecting an inductor, several attributes must be examined to find the right part for the application. First, the inductance value should be selected. The bq2416xx is designed to work with 1.5µH to 2.2µH inductors. The chosen value will have an effect on efficiency and package size. Due to the smaller current ripple, some efficiency gain is reached using the 2.2µH inductor, however, due to the physical size of the inductor, this may not be a viable option. The 1.5µH inductor provides a good tradeoff between size and efficiency.

Once the inductance has been selected, the peak current must be calculated in order to choose the current rating of the inductor. Use Equation 5 to calculate the peak current.

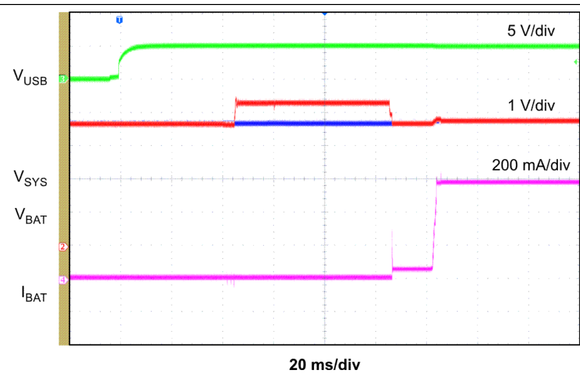
$$I_{PEAK} = I_{LOAD(MAX)} \times \left(1 + \frac{\%_{RIPPPLE}}{2}\right) \tag{5}$$

The inductor selected must have a saturation current rating greater than or equal to the calculated I_{PEAK}. Due to the high currents possible with the bq2416xx, a thermal analysis must also be done for the inductor. Many inductors have a 40°C temperature-rise rating. The DC component of the current can cause a 40°C temperature rise above the ambient temperature in the inductor. For this analysis, the typical load current may be used adjusted for the duty cycle of the load transients. For example, if the application requires a 1.5A DC load with peaks at 2.5A 20% of the time, a Δ40°C temperature rise current must be greater than 1.7A:

$$I_{TEMPRISE} = I_{LOAD} + D \times \left(I_{PEAK} - I_{LOAD}\right) = 1.5A + 0.2 \times \left(2.5A - 1.5A\right) = 1.7A \quad (6)$$

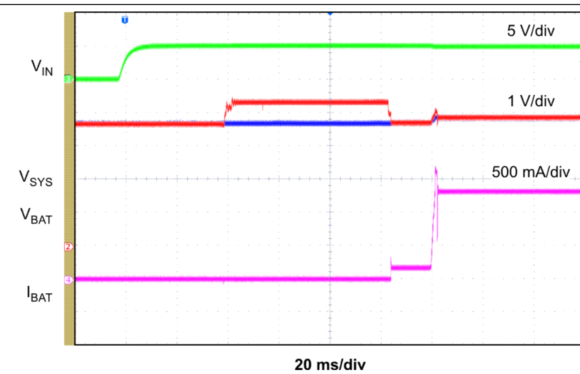
The bq2416xx provides internal loop compensation. Using this scheme, the bq2416xx is stable with 10µF to 200µF of local capacitance on the SYS output. The capacitance on the SYS rail can be higher if distributed amongst the rail. To reduce the output voltage ripple, a ceramic capacitor with the capacitance between 10µF and 47µF is recommended for local bypass to SYS. A 47µF bypass capacitor is recommended for optimal transient response.

10.2.3 Application Curves



USB500
925mA Charge Setting

Figure 23. USB Plug-In with Battery Connected



1500mA ILIM
1300mA Charge Setting

Figure 24. IN Plug-in with Battery Connected

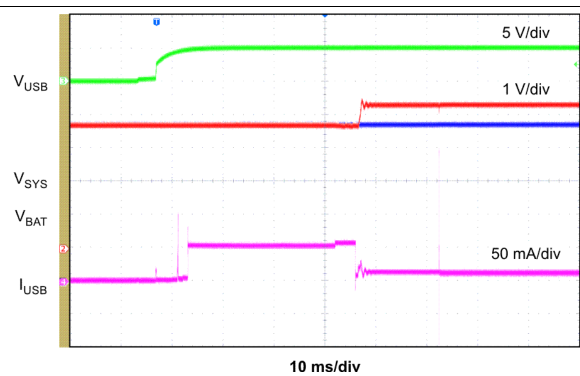
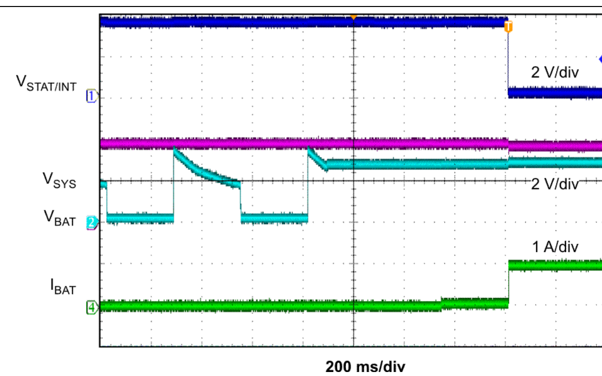
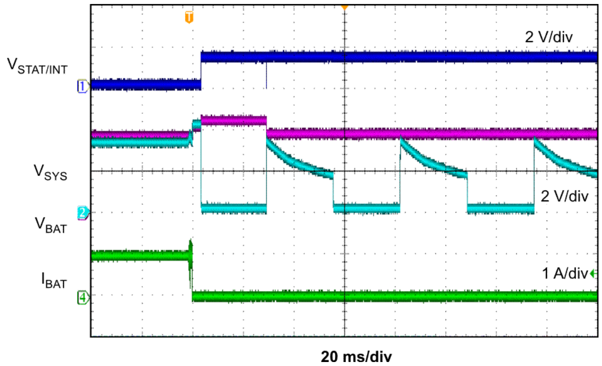


Figure 25. Adapter Detection USB



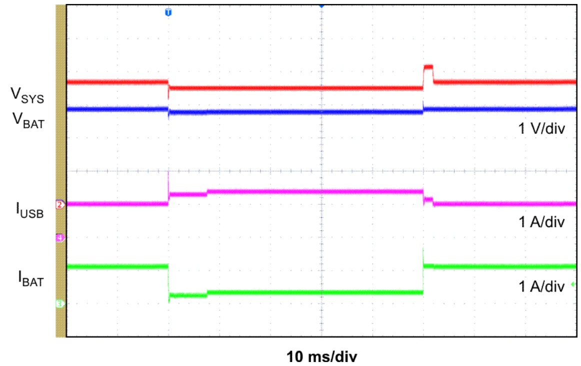
Termination Enabled

Figure 26. Battery Insert During Battery Detection



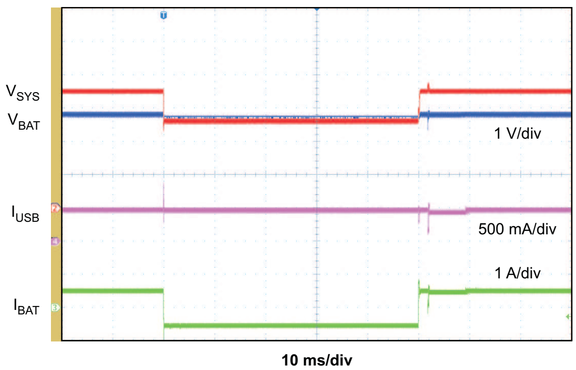
Termination Enabled

Figure 27. Battery Pull During Charging



MINSYS Operation
USB1500
200mA-1400mA Load Step on SYS

Figure 28. Load Transient into DPPM



MINSYS Operation
USB500
200mA - 1400mA Load Step on SYS

Figure 29. Load Transient into Supplement Mode

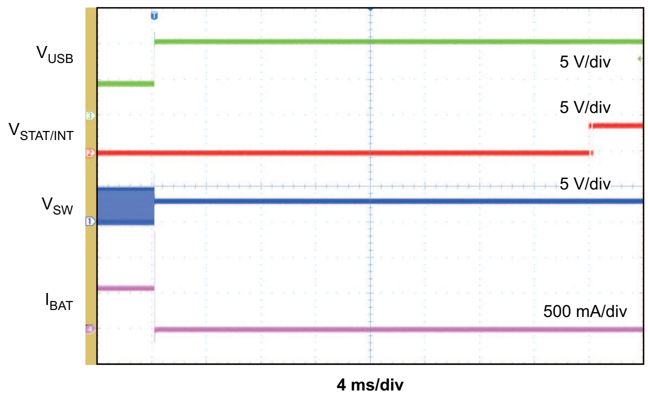
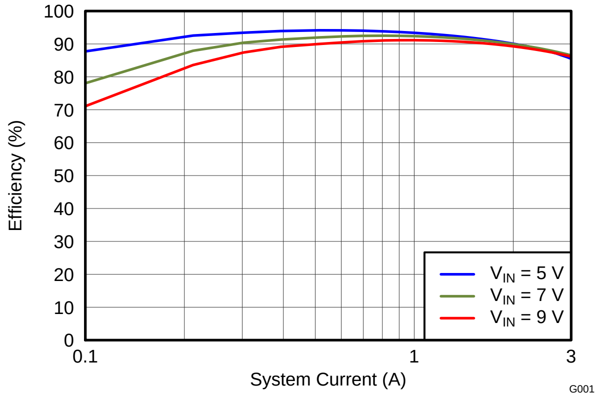
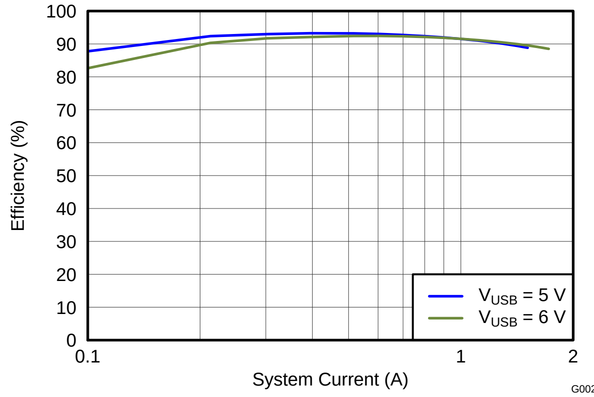


Figure 30. OVP Fault USB Input



Charge Disabled
SYS loaded
V_{BATREG} = 3.6V
IN2500 ILIM

Figure 31. IN Efficiency



Charge Disabled
SYS loaded
V_{BATREG} = 3.6V
USB1500 ILIM

Figure 32. USB Efficiency

11 Power Supply Recommendations

11.1 Requirements for SYS Output

In order to provide an output voltage on SYS, the bq2416xx requires either a power supply between 4.2 V and 6.0 V for USB input on all versions, 4.2 V and 6.0 V for IN input on bq24168 and 4.2 V and 10.0 V on the remaining versions with at least 100 mA current rating connected to IN or USB OR a single-cell LiIon battery with voltage > $V_{BATUVLO}$ connected to BAT. The source current rating needs to be at least 2.5 A in order for the charger's buck converter to provide maximum output power to SYS.

11.2 Requirements for Charging

In order for charging to occur, the source voltage as measured at the IC's USB or IN pins (factoring in cable/trace losses from the source) must be greater than the VINDPM threshold (but less than the maximum values above) and the source's current rating must be higher than the buck converter needs to provide the load on SYS. For charging at a desired charge current of I_{CHRG}, $V_{USBorIN}$x $I_{USBorIN}$ x η > V_{SYS} x (I_{SYS}+ I_{CHRG}) where η is the efficiency estimate from Figure 1 or Figure 2 and V_{SYS} = V_{BAT} when V_{BAT} charges above V_{MINSYS}. The charger limits $I_{USBorIN}$ to that input's current limit setting. With I_{SYS} = 0 A, the charger consumes maximum power at the end of CC mode, when the voltage at the BAT pin is near V_{BATREG} but I_{CHRG} has not started to taper off toward I_{TERM}.

12 Layout

12.1 Layout Guidelines

It is important to pay special attention to the PCB layout. Figure 33 provides a sample layout for the high current paths of the bq2416xx. A list of layout guidelines follows.

- To obtain optimal performance, the power input capacitors, connected from the PMID input to PGND, must be placed as close as possible to the bq2416xx
- Minimize the amount of inductance between BAT and the postive connection of the battery terminal. If a large parasitic board inductance on BAT is expected, increase the bypass capacitance on BAT.
- Place 4.7µF input capacitor as close to PMID_ pin and PGND pin as possible to make high frequency current loop area as small as possible. Place 1µF input capacitor GNDs as close to the respective PMID cap GND and PGND pins as possible to minimize the ground difference between the input and PMID_.
- The traces from the input connector to the inputs of the bq2416xx should be as wide as possible to minimize the impedance in the line. Although the VINDPM feature will allow operation from input sources having high resistances(impedances), the bq2416xx input pins (IN and USB) have been optimized to connect to input sources with no more than 350mohm of input resistance, including cables and PCB traces
- The local bypass capacitor from SYS to GND should be connected between the SYS pin and PGND of the IC. The intent is to minimize the current path loop area from the SW pin through the LC filter and back to the PGND pin.
- Place all decoupling capacitors close to their respective IC pins and as close as to PGND (do not place components such that routing interrupts power stage currents). All small control signals should be routed away from the high-current paths.
- The PCB should have a ground plane (return) connected directly to the return of all components through vias (two vias per capacitor for power-stage capacitors, one via per capacitor for small-signal components). It is also recommended to put vias inside the PGND pads for the IC, if possible. A star ground design approach is typically used to keep circuit block currents isolated (high-power/low-power small-signal) which reduces noise-coupling and ground-bounce issues. A single ground plane for this design gives good results. With this small layout and a single ground plane, there is no ground-bounce issue, and having the components segregated minimizes coupling between signals.
- The high-current charge paths into IN, USB, BAT, SYS and from the SW pins must be sized appropriately for the maximum charge current in order to avoid voltage drops in these traces. The PGND pins should be connected to the ground plane to return current through the internal low-side FET.
- For high-current applications, the balls for the power paths should be connected to as much copper in the board as possible. This allows better thermal performance because the board conducts heat away from the IC.

12.2 Layout Example

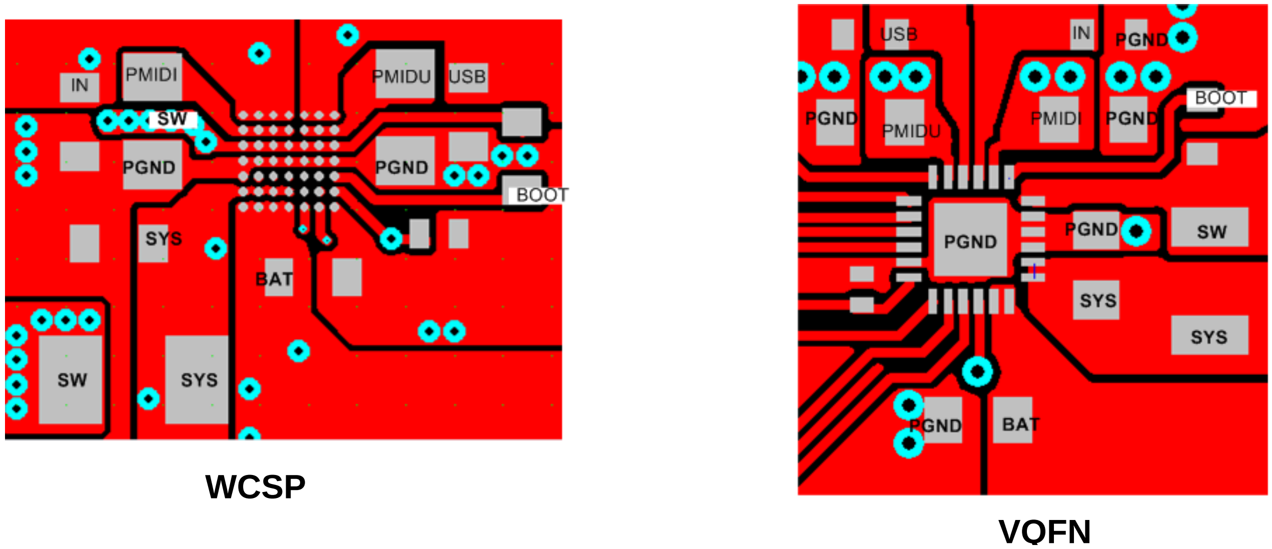


Figure 33. Recommended bq2416xx PCB Layout

13 器件和文档支持

13.1 相关链接

下面的表格列出了快速访问链接。类别包括技术文档、支持与社区资源、工具和软件，以及申请样片或购买产品的快速链接。

表 **2.** 相关链接

器件	产品文件夹	样片与购买	技术文档	工具和软件	支持和社区
bq24160	请单击此处	请单击此处	请单击此处	请单击此处	请单击此处
bq24160A	请单击此处	请单击此处	请单击此处	请单击此处	请单击此处
bq24161	请单击此处	请单击此处	请单击此处	请单击此处	请单击此处
bq24161B	请单击此处	请单击此处	请单击此处	请单击此处	请单击此处
bq24163	请单击此处	请单击此处	请单击此处	请单击此处	请单击此处
bq24168	请单击此处	请单击此处	请单击此处	请单击此处	请单击此处

13.2 社区资源

下列链接提供到 TI 社区资源的连接。链接的内容由各个分销商"按照原样"提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的 《使用条款》。

TI E2E™ 在线社区 ***TI 的工程师对工程师 (E2E) 社区。***此社区的创建目的在于促进工程师之间的协作。在 e2e.ti.com 中，您可以咨询问题、分享知识、拓展思路并与同行工程师一道帮助解决问题。

设计支持 ***TI 参考设计支持*** 可帮助您快速查找有帮助的 E2E 论坛、设计支持工具以及技术支持的联系信息。

13.3 商标

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

13.4 静电放电警告

这些装置包含有限的内置 ESD 保护。 存储或装卸时，应将导线一起截短或将装置放置于导电泡棉中，以防止 MOS 门极遭受静电损伤。

13.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

14 机械、封装和可订购信息

以下页中包括机械封装、封装和可订购信息。这些信息是针对指定器件可提供的最新数据。这些数据发生变化时，我们可能不会另行通知或修订此文档。如欲获取此产品说明书的浏览器版本，请参阅左侧的导航栏。

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
BQ24160ARGER	ACTIVE	VQFN	RGE	24	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR		BQ 24160A	Samples
BQ24160ARGET	ACTIVE	VQFN	RGE	24	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR		BQ 24160A	Samples
BQ24160RGER	ACTIVE	VQFN	RGE	24	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	BQ 24160	Samples
BQ24160RGET	ACTIVE	VQFN	RGE	24	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	BQ 24160	Samples
BQ24160YFFR	ACTIVE	DSBGA	YFF	49	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 85	BQ24160	Samples
BQ24160YFFT	ACTIVE	DSBGA	YFF	49	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 85	BQ24160	Samples
BQ24161BRGER	ACTIVE	VQFN	RGE	24	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	BQ 24161B	Samples
BQ24161BRGET	ACTIVE	VQFN	RGE	24	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	BQ 24161B	Samples
BQ24161RGER	ACTIVE	VQFN	RGE	24	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	BQ 24161	Samples
BQ24161RGET	ACTIVE	VQFN	RGE	24	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	BQ 24161	Samples
BQ24161YFFR	ACTIVE	DSBGA	YFF	49	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 85	BQ24161	Samples
BQ24161YFFT	ACTIVE	DSBGA	YFF	49	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 85	BQ24161	Samples
BQ24163RGER	ACTIVE	VQFN	RGE	24	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	BQ 24163	Samples
BQ24163RGET	ACTIVE	VQFN	RGE	24	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	BQ 24163	Samples
BQ24163YFFR	ACTIVE	DSBGA	YFF	49	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 85	BQ24163	Samples
BQ24163YFFT	ACTIVE	DSBGA	YFF	49	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 85	BQ24163	Samples
BQ24168RGER	ACTIVE	VQFN	RGE	24	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	BQ 24168	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
BQ24168RGET	ACTIVE	VQFN	RGE	24	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	BQ 24168	Samples
BQ24168YFFR	ACTIVE	DSBGA	YFF	49	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 85	BQ24168	Samples
BQ24168YFFT	ACTIVE	DSBGA	YFF	49	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 85	BQ24168	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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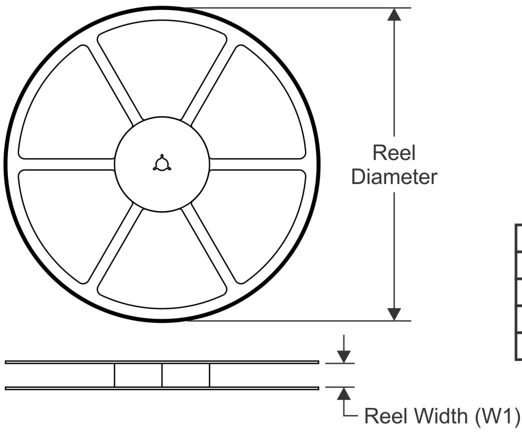
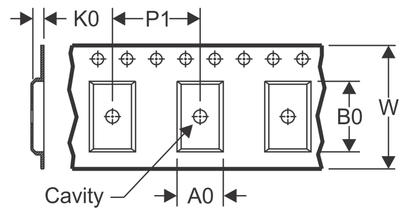
TAPE AND REEL INFORMATION

REEL DIMENSIONS

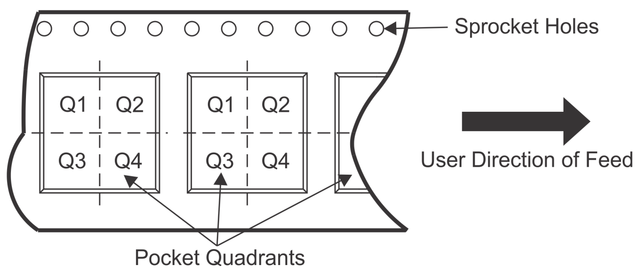


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

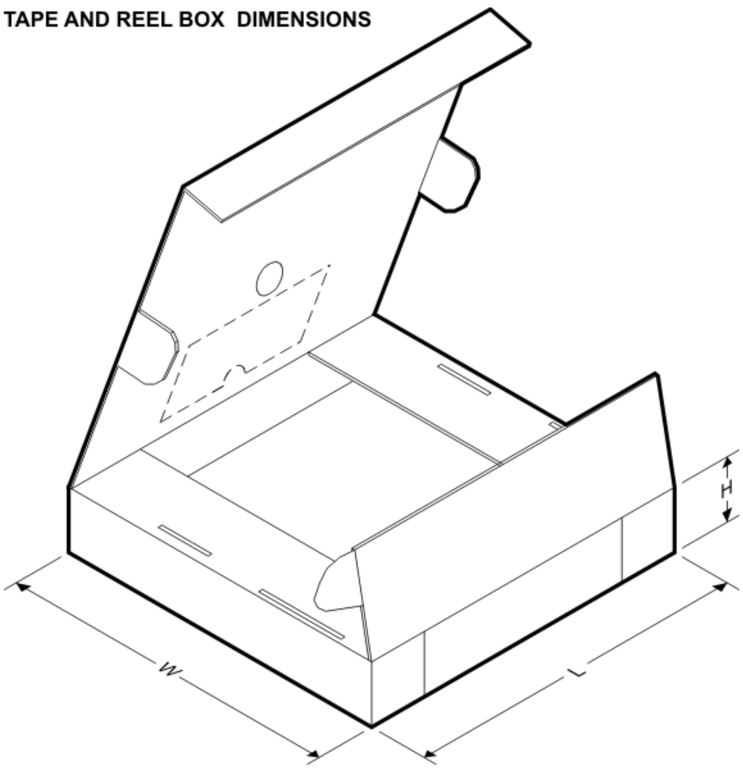


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
BQ24160ARGER	VQFN	RGE	24	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
BQ24160ARGET	VQFN	RGE	24	250	180.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
BQ24160RGER	VQFN	RGE	24	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
BQ24160RGET	VQFN	RGE	24	250	180.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
BQ24160YFFR	DSBGA	YFF	49	3000	180.0	8.4	2.93	2.93	0.81	4.0	8.0	Q1
BQ24160YFFT	DSBGA	YFF	49	250	180.0	8.4	2.93	2.93	0.81	4.0	8.0	Q1
BQ24161BRGER	VQFN	RGE	24	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
BQ24161BRGET	VQFN	RGE	24	250	180.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
BQ24161RGER	VQFN	RGE	24	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
BQ24161RGET	VQFN	RGE	24	250	180.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
BQ24161YFFR	DSBGA	YFF	49	3000	180.0	8.4	2.93	2.93	0.81	4.0	8.0	Q1
BQ24161YFFT	DSBGA	YFF	49	250	180.0	8.4	2.93	2.93	0.81	4.0	8.0	Q1
BQ24163RGER	VQFN	RGE	24	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
BQ24163RGET	VQFN	RGE	24	250	180.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
BQ24163YFFR	DSBGA	YFF	49	3000	180.0	8.4	2.93	2.93	0.81	4.0	8.0	Q1
BQ24163YFFT	DSBGA	YFF	49	250	180.0	8.4	2.93	2.93	0.81	4.0	8.0	Q1
BQ24168RGER	VQFN	RGE	24	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
BQ24168RGET	VQFN	RGE	24	250	180.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
BQ24168YFFR	DSBGA	YFF	49	3000	180.0	8.4	2.93	2.93	0.81	4.0	8.0	Q1
BQ24168YFFT	DSBGA	YFF	49	250	180.0	8.4	2.93	2.93	0.81	4.0	8.0	Q1

TAPE AND REEL BOX DIMENSIONS

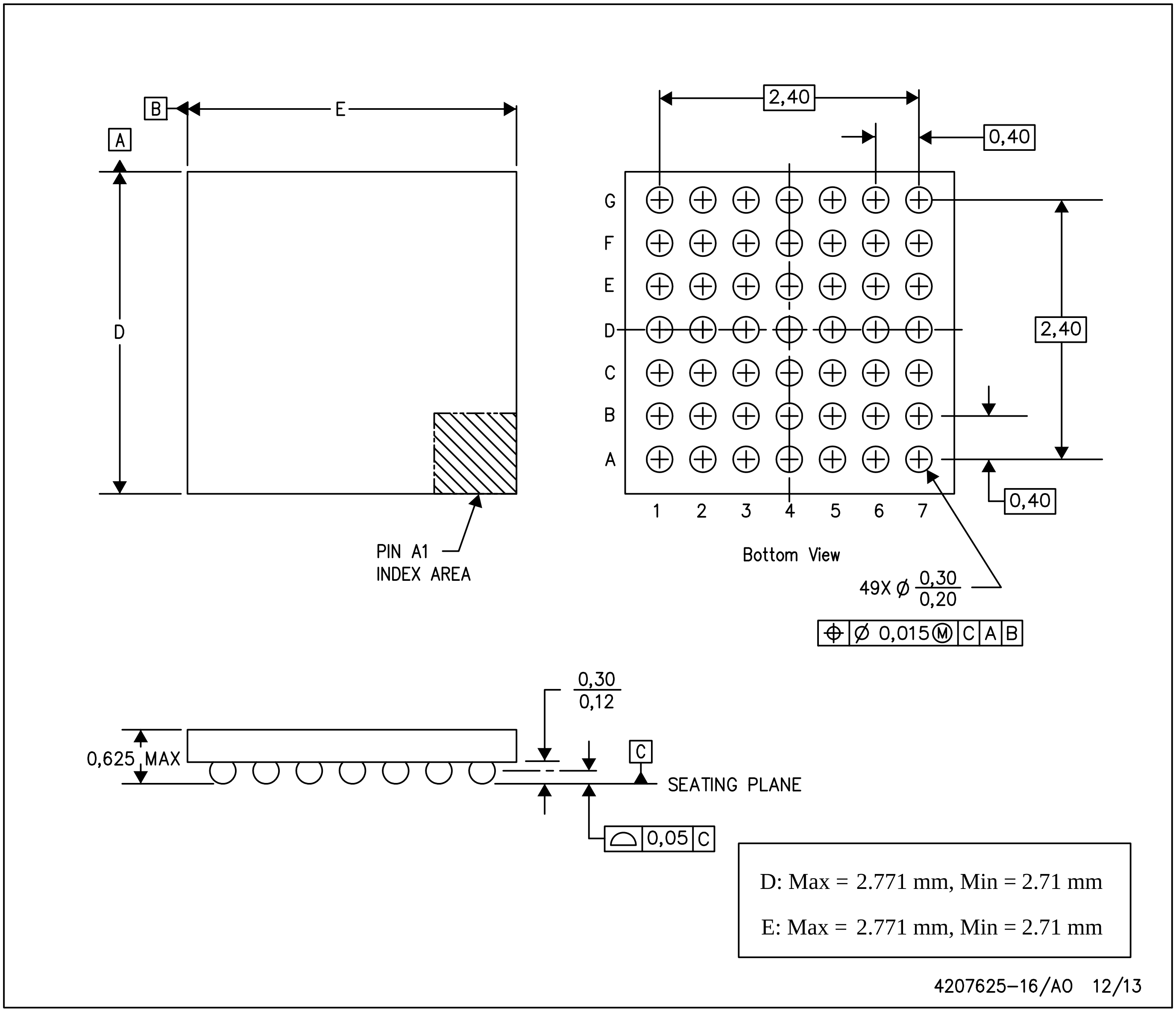


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
BQ24160ARGER	VQFN	RGE	24	3000	367.0	367.0	35.0
BQ24160ARGET	VQFN	RGE	24	250	210.0	185.0	35.0
BQ24160RGER	VQFN	RGE	24	3000	367.0	367.0	35.0
BQ24160RGET	VQFN	RGE	24	250	210.0	185.0	35.0
BQ24160YFFR	DSBGA	YFF	49	3000	182.0	182.0	20.0
BQ24160YFFT	DSBGA	YFF	49	250	182.0	182.0	20.0
BQ24161BRGER	VQFN	RGE	24	3000	367.0	367.0	35.0
BQ24161BRGET	VQFN	RGE	24	250	210.0	185.0	35.0
BQ24161RGER	VQFN	RGE	24	3000	367.0	367.0	35.0
BQ24161RGET	VQFN	RGE	24	250	210.0	185.0	35.0
BQ24161YFFR	DSBGA	YFF	49	3000	182.0	182.0	20.0
BQ24161YFFT	DSBGA	YFF	49	250	182.0	182.0	20.0
BQ24163RGER	VQFN	RGE	24	3000	367.0	367.0	35.0
BQ24163RGET	VQFN	RGE	24	250	210.0	185.0	35.0
BQ24163YFFR	DSBGA	YFF	49	3000	182.0	182.0	20.0

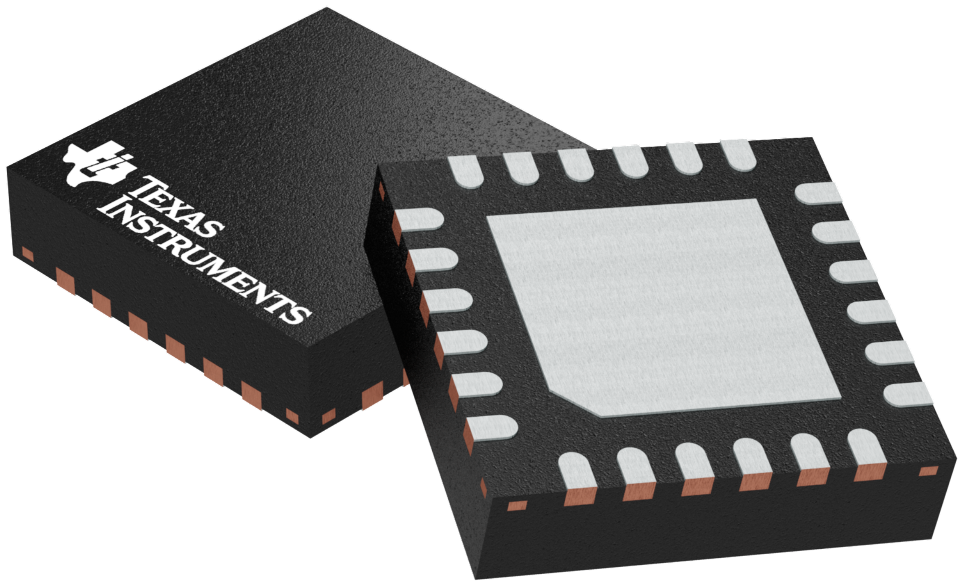
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
BQ24163YFFT	DSBGA	YFF	49	250	182.0	182.0	20.0
BQ24168RGER	VQFN	RGE	24	3000	367.0	367.0	35.0
BQ24168RGET	VQFN	RGE	24	250	210.0	185.0	35.0
BQ24168YFFR	DSBGA	YFF	49	3000	182.0	182.0	20.0
BQ24168YFFT	DSBGA	YFF	49	250	182.0	182.0	20.0

YFF (R–XBGA–N49) DIE–SIZE BALL GRID ARRAY

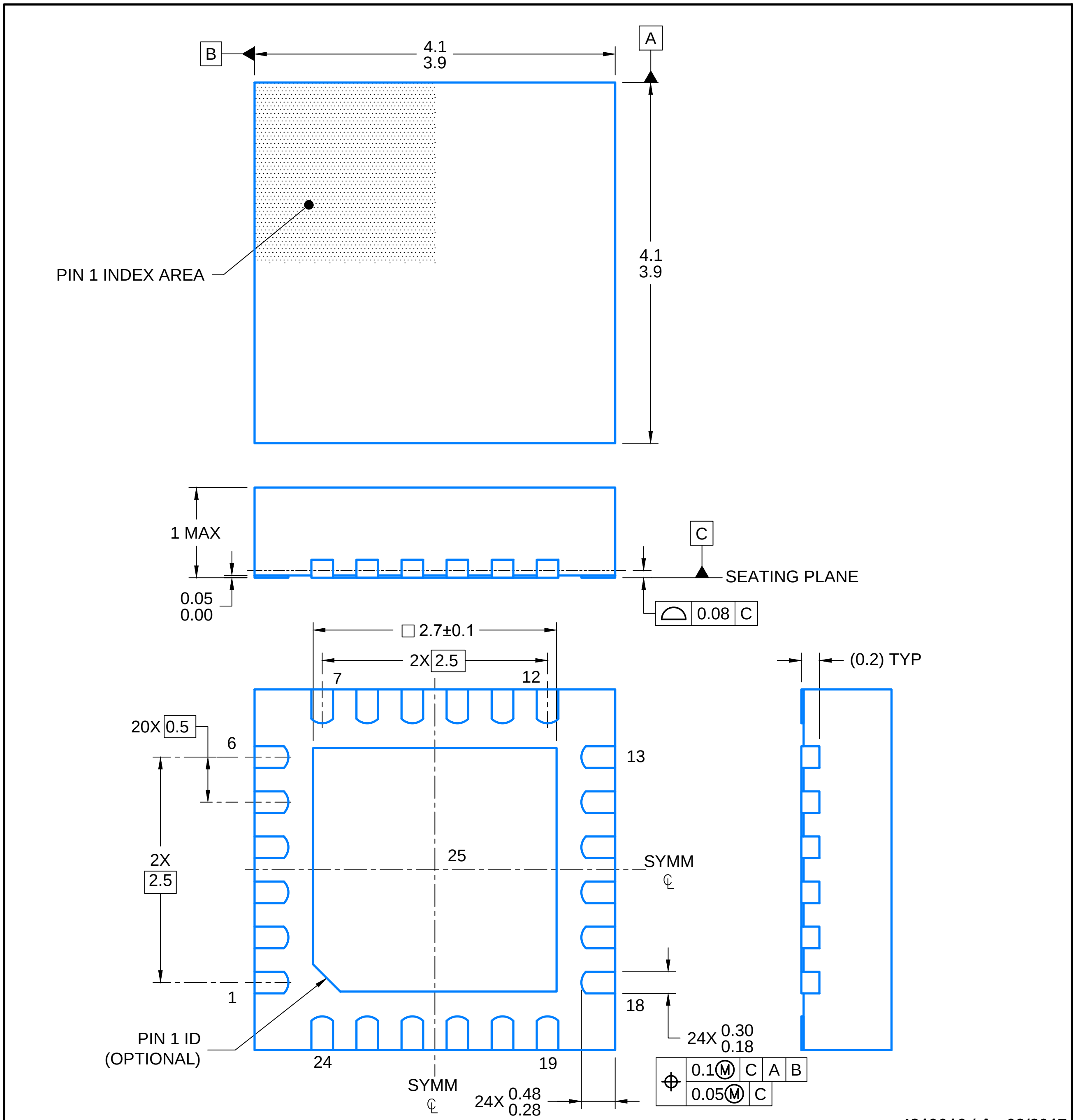


NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. NanoFree™ package configuration.

NanoFree is a trademark of Texas Instruments.



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



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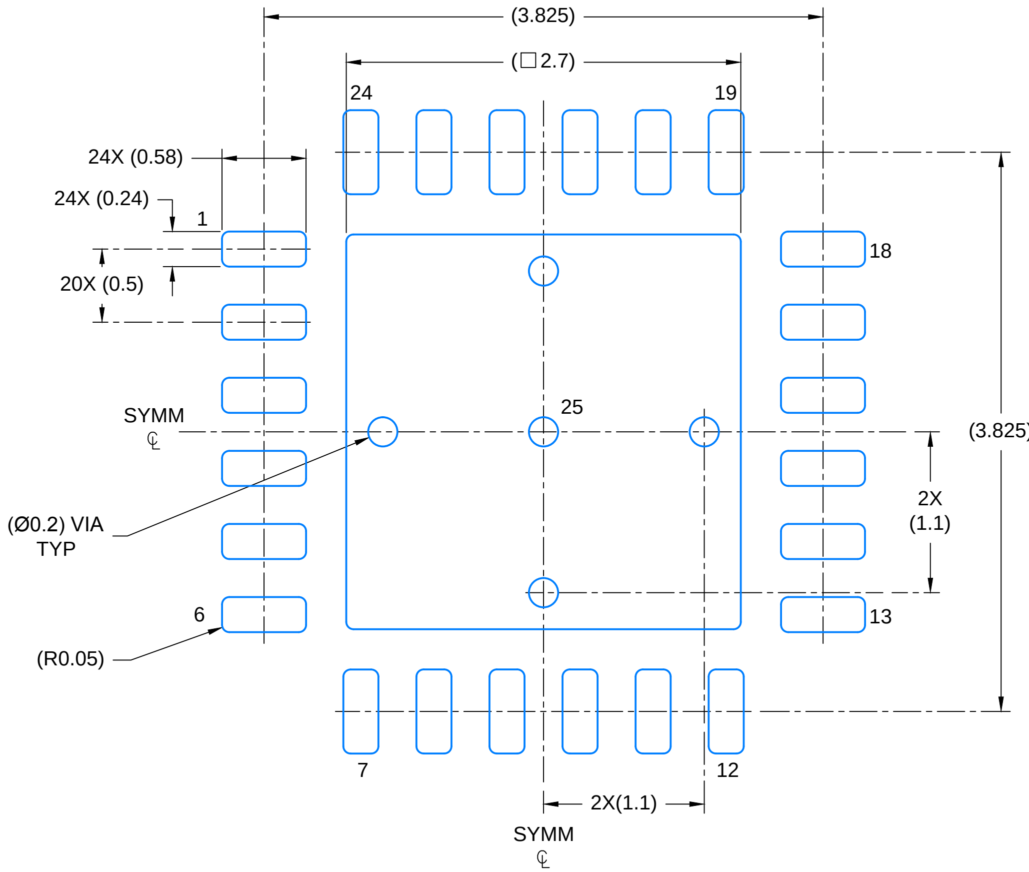
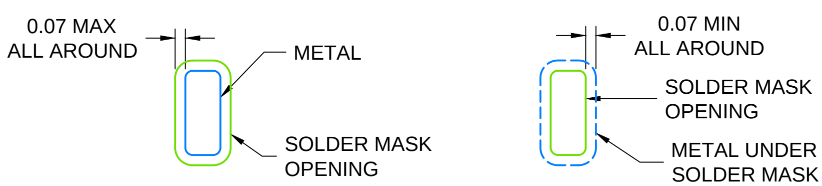
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
SCALE: 20X



NON SOLDER MASK
DEFINED
(PREFERRED)

SOLDER MASK
DEFINED

SOLDER MASK DETAILS

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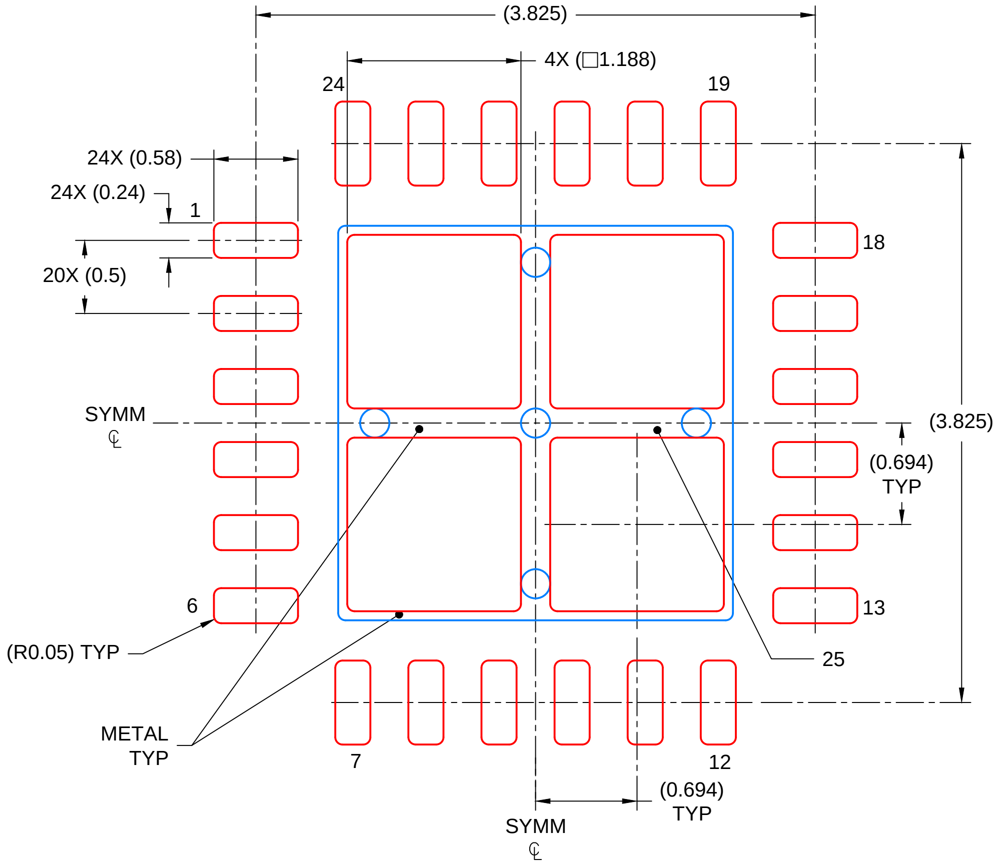
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
78% PRINTED COVERAGE BY AREA
SCALE: 20X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations..

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