LM2907 and LM2917 Frequency to Voltage Converter

1 Features

- Ground Referenced Tachometer Input Interfaces Directly With Variable Reluctance Magnetic Pickups
- Op Amp Has Floating Transistor Output
- 50-mA Sink or Source to Operate Relays, Solenoids, Meters, or LEDs
- Frequency Doubling For Low Ripple
- Tachometer Has Built-In Hysteresis With Either Differential Input or Ground Referenced Input
- ±0.3% Linearity (Typical)
- Ground-Referenced Tachometer is Fully Protected From Damage Due to Swings Above V_{CC} and Below Ground
- Output Swings to Ground For Zero Frequency Input
- Easy to Use; $V_{OUT} = f_{IN} \times V_{CC} \times R1 \times C1$
- Zener Regulator on Chip allows Accurate and Stable Frequency to Voltage or Current Conversion (LM2917)

2 Applications

- Over- and Under-Speed Sensing
- Frequency-to-Voltage Conversion (Tachometer)
- Speedometers
- Breaker Point Dwell Meters
- Hand-Held Tachometers
- Speed Governors
- Cruise Control
- Automotive Door Lock Control
- Clutch Control
- Horn Control
- Touch or Sound Switches

3 Description

The LM2907 and LM2917 devices are monolithic frequency-to-voltage converters with a high gain op amp designed to operate a relay, lamp, or other load when the input frequency reaches or exceeds a selected rate. The tachometer uses a charge pump technique and offers frequency doubling for low-ripple, full-input protection in two versions (8-pin LM2907 and LM2917), and its output swings to ground for a zero frequency input.

The op amp is fully compatible with the tachometer and has a floating transistor as its output. This feature allows either a ground or supply referred load of up to 50 mA. The collector may be taken above V_{CC} up to a maximum V_{CE} of 28 V.

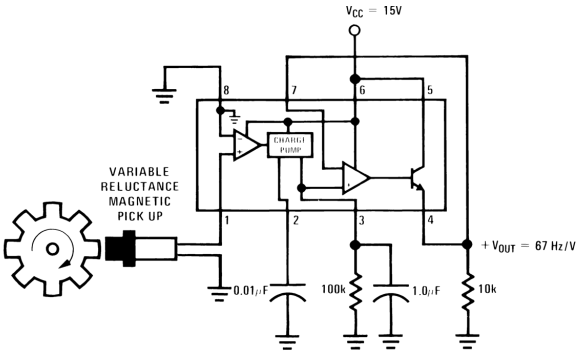
The two basic configurations offered include an 8-pin device with a *ground-referenced tachometer* input and an internal connection between the tachometer output and the op amp noninverting input. This version is well suited for single speed or frequency switching or fully buffered frequency-to-voltage conversion applications.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
LM2907-N, LM2917-N	PDIP (8)	6.35 mm × 9.81 mm
	PDIP (14)	6.35 mm × 19.177 mm
	SOIC (8)	3.91 mm × 4.90 mm
	SOIC (14)	3.91 mm × 8.65 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Minimum Component Tachometer Diagram



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision C (March 2013) to Revision D	Page
• Added *Device Information* table, *Pin Configuration and Functions* section, *ESD Ratings* table, *Recommended Operating Conditions* table, *Thermal Information* table, *Parameter Measurement Information* section, *Detailed Description* section, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section	1
• Deleted Built-In Zener on LM2917 from *Features*	1
• Deleted Only One RC Network Provides Frequency Doubling from *Features*	1
• Added *Thermal Information* table	6
• Changed tablenote text From: C2 = 0.22 mFd To: C2 = 0.22 µF	6

Changes from Revision B (March 2013) to Revision C	Page
• Changed layout of National Semiconductor Data Sheet to TI format	1

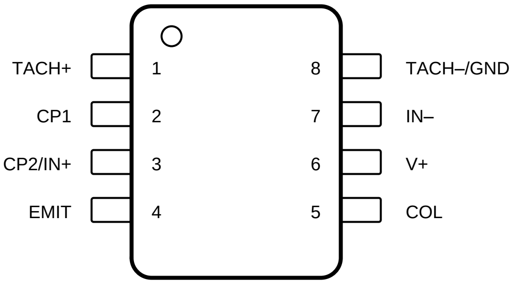
5 Description (continued)

The more versatile configurations provide differential tachometer input and uncommitted op amp inputs. With this version the tachometer input may be floated and the op amp becomes suitable for active filter conditioning of the tachometer output.

Both of these configurations are available with an active shunt regulator connected across the power leads. The regulator clamps the supply such that stable frequency-to-voltage and frequency-to-current operations are possible with any supply voltage and a suitable resistor.

6 Pin Configuration and Functions

P and D Package
8-Pin PDIP and SOIC
Top View

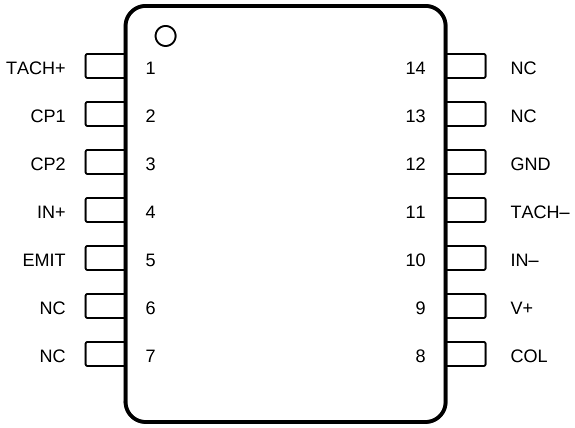


Not to scale

Pin Functions: 8 Pins

PIN		I/O	DESCRIPTION
NAME	NO.		
COL	5	I	The collector of the bipolar junction transistor
CP1	2	O	A capacitor placed on this pin will be charged up to $V_{CC}/2$ by a constant current source of 180 µA typical at the start of every positive half cycle. At the beginning of negative half cycles this capacitor is discharged the same amount at the same rate.
CP2/IN+	3	I/O	See pins CP1 and IN+. On 8-pin devices (8-pin LM2907 and LM2917) these two nodes share a pin and are internally connected.
EMIT	4	O	The emitter of the bipolar junction transistor
GND	—	G	Ground
IN+	—	I	The noninverting input to the high gain op amp
IN–	7	I	The inverting input to the high gain op amp
NC	—	—	No connect
TACH+	1	I	Positive terminal for the input signal that leads to the noninverting terminal of the internal Schmitt-Trigger comparator.
TACH–/GND	8	I	Negative terminal for the input signal that leads to the noninverting terminal of the internal Schmitt-Trigger comparator. (NOTE: On 8-pin devices, LM2907 and LM2917, this pin is internally connected to ground and must be tied to ground externally to provide the reference voltage of the device).
V+	6	I	Supply voltage

NFF and D Package
14-Pin PDIP and SOIC
Top View



Not to scale

Pin Functions: 14 Pins

PIN		I/O	DESCRIPTION
NAME	NO.		
COL	8	I	The collector of the bipolar junction transistor
CP1	2	O	A capacitor placed on this pin will be charged up to $V_{CC}/2$ by a constant current source of 180 µA typical at the start of every positive half cycle. At the beginning of negative half cycles this capacitor is discharged the same amount at the same rate.
CP2	3	O	The charge pump sources current out of this pin equal to the absolute value of the capacitor current on CP1. A resistor and capacitor in parallel connected to this pin filters the current pulses into the output voltage.
EMIT	5	O	The emitter of the bipolar junction transistor
GND	12	G	Ground
IN+	4	I	The noninverting input to the high gain op amp
IN–	10	I	The inverting input to the high gain op amp
NC	6, 7, 13, 14	—	No connect
TACH+	1	I	Positive terminal for the input signal that leads to the noninverting terminal of the internal Schmitt-Trigger comparator.
TACH–	11	I	Negative terminal for the input signal that leads to the noninverting terminal of the internal Schmitt-Trigger comparator.
V+	9	I	Supply voltage

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)(2)

			MIN	MAX	UNIT
Supply voltage				28	V
Supply current (Zener options)				25	mA
Collector voltage				28	V
Differential input voltage	Tachometer, op amp, and comparator			28	V
Input voltage	Tachometer	LM2907 (8), LM2917 (8)	–28	28	V
		LM2907 (14), LM2917 (14)	0	28	
	Op amp and comparator		0	28	
Power dissipation	LM29x7 (8)			1200	mW
	LM29x7 (14)			1580	
Soldering information	PDIP package	Soldering (10 s)		260	°C
	SOIC package	Vapor phase (60 s)		215	
		Infrared (15 s)		220	
Operating temperature, T_J			–40	85	°C
Storage temperature, T_{stg}			–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/Distributors for availability and specifications.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JESD22-A114(1)	±1000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±250	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
Input voltage	LM2907 (8), LM2917 (8)	–28		28	V
	LM2907 (14), LM2917 (14)	0		28	V
Output sink current				50	mA

7.4 Thermal Information

THERMAL METRIC(1)		LM2907, LM2917				UNIT
		P (PDIP)	D (SOIC)	NFF (PDIP)	D (SOIC)	
		8 PINS	8 PINS	14 PINS	14 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	77.6	110	69.1	83.7	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	80.5	53.9	64.8	42.1	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	54.8	50.4	49.1	38	°C/W
ψ_{JT}	Junction-to-top characterization parameter	37.6	9.1	35.1	7.7	°C/W
ψ_{JB}	Junction-to-board characterization parameter	54.8	49.9	49	37.7	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	—	—	—	—	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

7.5 Electrical Characteristics

V_{CC} = 12 V_{DC}, T_A = 25°C, see test circuit

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
TACHOMETER						
	Input thresholds	V_{IN} = 250 mVp-p at 1 kHz(1)	±10	±25	±40	mV
	Hysteresis	V_{IN} = 250 mVp-p at 1 kHz(1)		30		mV
	LM29x7 offset voltage	V_{IN} = 250 mVp-p at 1 kHz(1)		3.5	10	mV
		V_{IN} = 250 mVp-p at 1 kHz (8-pin LM29x7)(1)		5	15	
	Input bias current	V_{IN} = ±50 mV_{DC}		0.1	1	µA
V_{OH}	High level output voltage	For CP1, V_{IN} = 125 mV_{DC}(2)		8.3		V
V_{OL}	Low level output voltage	For CP1, V_{IN} = –125 mV_{DC}(2)		2.3		V
I_2, I_3	Output current	V2 = V3 = 6 V(3)	140	180	240	µA
I_3	Leakage current	I2 = 0, V3 = 0			0.1	µA
K	Gain constant	See(2)	0.9	1	1.1	
	Linearity	f_{IN} = 1 kHz, 5 kHz, or 10 kHz(4)	–1%	0.3%	1%	
OP AMP AND COMPARATOR						
V_{OS}	Input offset voltage	V_{IN} = 6 V		3	10	mV
I_{BIAS}	Bias current	V_{IN} = 6 V		50	500	nA
	Input common-mode voltage		0		V_{CC}–1.5	V
	Voltage gain			200		V/mV
	Output sink current	V_C = 1	40	50		mA
	Output source current	V_E = V_{CC} –2		10		mA
	Saturation voltage	I_{SINK} = 5 mA		0.1	0.5	V
		I_{SINK} = 20 mA			1	V
		I_{SINK} = 50 mA		1	1.5	V
ZENER REGULATOR						
	Regulator voltage	R_{DROP} = 470 Ω		7.56		V
	Series resistance			10.5	15	Ω
	Temperature stability			1		mV/°C
	Total supply current			3.8	6	mA

(1) Hysteresis is the sum V_{TH} – ($–V_{TH}$), offset voltage is their difference. See test circuit.
(2) $V_{OH} = 0.75 \times V_{CC} - 1\ V_{BE}$ and $V_{OL} = 0.25 \times V_{CC} - 1\ V_{BE}$, therefore $V_{OH} - V_{OL} = V_{CC} / 2$. The difference ($V_{OH} - V_{OL}$) and the mirror gain ($I_2 / I_3$) are the two factors that cause the tachometer gain constant to vary from 1.
(3) Ensure that when choosing the time constant R1 × C1 that the maximum anticipated output voltage at CP2/IN+ can be reached with $I_3 \times R1$. The maximum value for R1 is limited by the output resistance of CP2/IN+ which is greater than 10 MΩ typically.
(4) Nonlinearity is defined as the deviation of V_{OUT} (at CP2/IN+) for f_{IN} = 5 kHz from a straight line defined by the V_{OUT} at 1 kHz and V_{OUT} at 10 kHz. C1 = 1000 pF, R1 = 68 kΩ and C2 = 0.22 µF.

7.6 Typical Characteristics

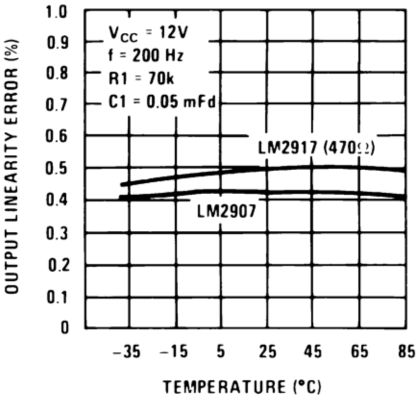


Figure 1. Tachometer Linearity vs Temperature

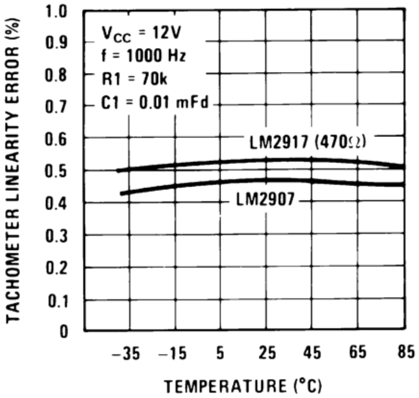


Figure 2. Tachometer Linearity vs Temperature

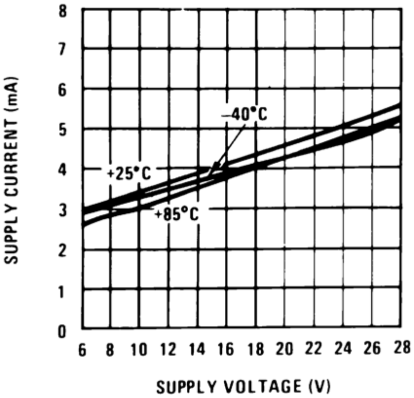


Figure 3. Total Supply Current

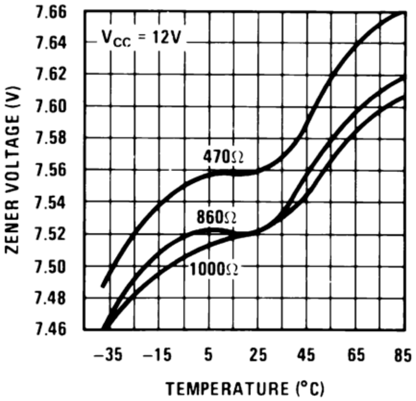


Figure 4. Zener Voltage vs Temperature

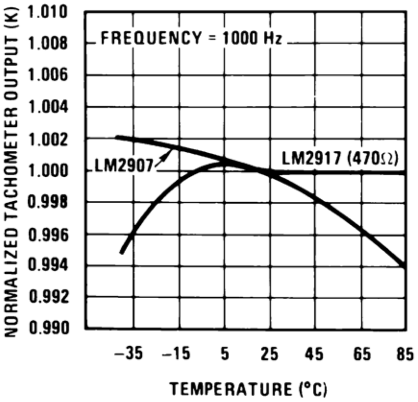


Figure 5. Normalized Tachometer Output (K) vs Temperature

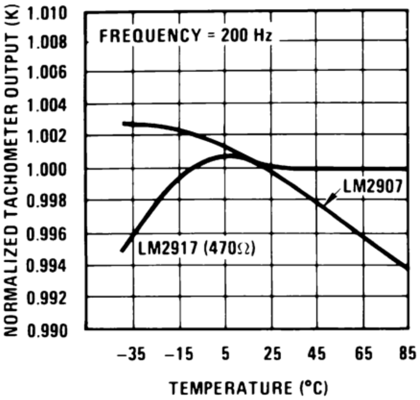


Figure 6. Normalized Tachometer Output (K) vs Temperature

Typical Characteristics (continued)

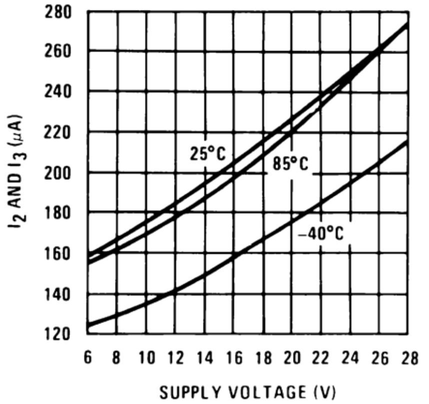


Figure 7. Tachometer Currents I_2 and I_3 vs Supply Voltage

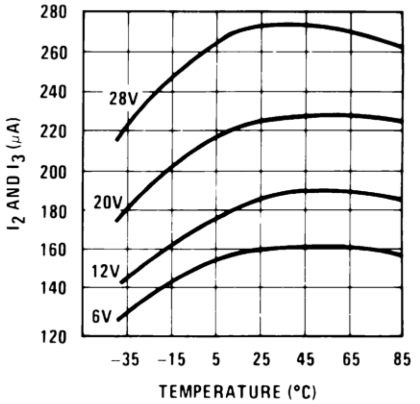


Figure 8. Tachometer Currents I_2 and I_3 vs Temperature

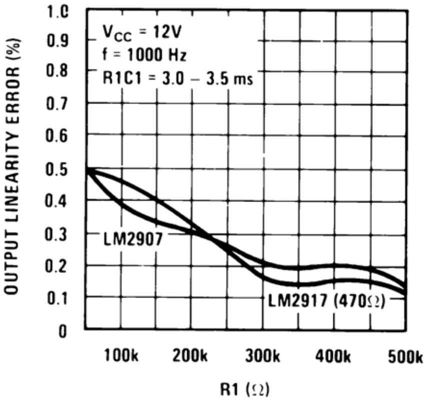


Figure 9. Tachometer Linearity vs R1

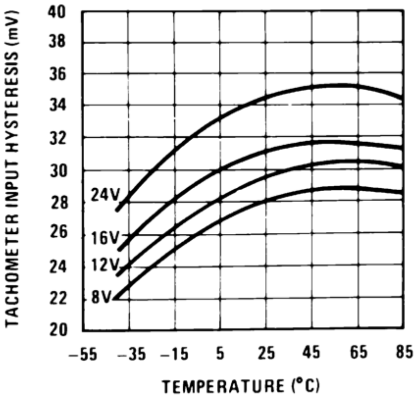


Figure 10. Tachometer Input Hysteresis vs Temperature

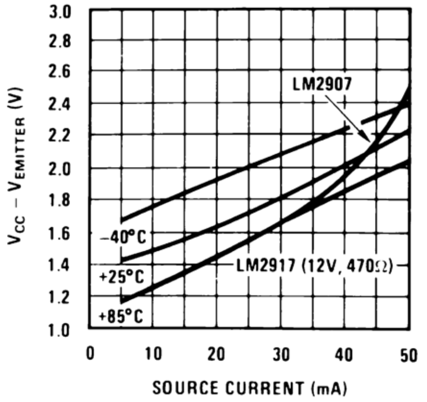


Figure 11. Op Amp Output Transistor Characteristics

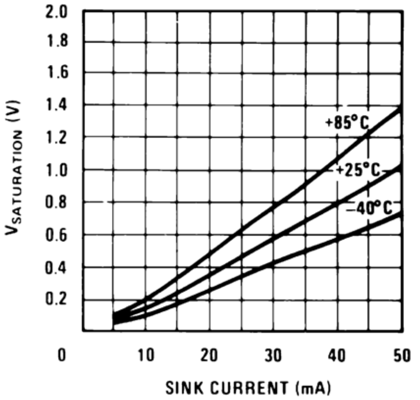


Figure 12. Op Amp Output Transistor Characteristics

8 Parameter Measurement Information

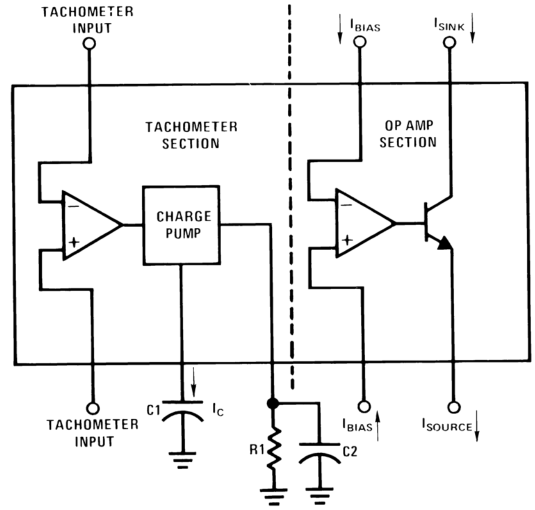


Figure 13. Test Circuit

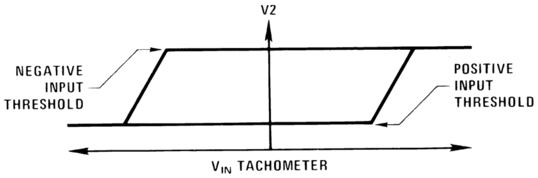


Figure 14. Tachometer Input Threshold Measurement

9 Detailed Description

9.1 Overview

The LM29x7 frequency-to-voltage converter features two separate inputs to monitor the signal. In the 8-pin devices, one of these inputs is internally grounded and therefore it monitors the remaining input for zero crossings. In the 14-pin devices, both of these inputs are open and it instead detects whenever the differential voltage switches polarity. Therefore, the input comparator outputs a square wave of equal frequency to the input.

A charge pump system is used to translate the frequency of this square wave to a voltage. At the start of every positive half cycle of the input signal a 180-µA constant current charges C1 until its voltage has increased by $V_{CC}/2$. The capacitor is held at that voltage until the input signal begins a negative half cycle. Then the 180-µA constant current discharges capacitor C1 until its voltage has dropped by $V_{CC}/2$. This voltage is held until the next positive half cycle and the process repeats. This generates pulses of current flowing into and out of capacitor C1 at the same frequency as the input signal. For every full cycle, the charge pump mirrors both current pulses as positive current pulses into the parallel combination of resistor R1 and capacitor C2. Therefore every full cycle, the amount of charge leaving pin 3 is equal to the sum of the charge entering C1 and leaving C1. Because the voltage at pin 3 is equal to I3(avg) × R1, I(avg) is calculated in Equation 1.

$$I3(avg) = Q/t = (Qcharge + Qdischarge) / (1 / f) = 2 \times Q \times f = 2 \times C1 \times (V_{CC}/2) \times f = C1 \times V_{CC} \times f \quad (1)$$

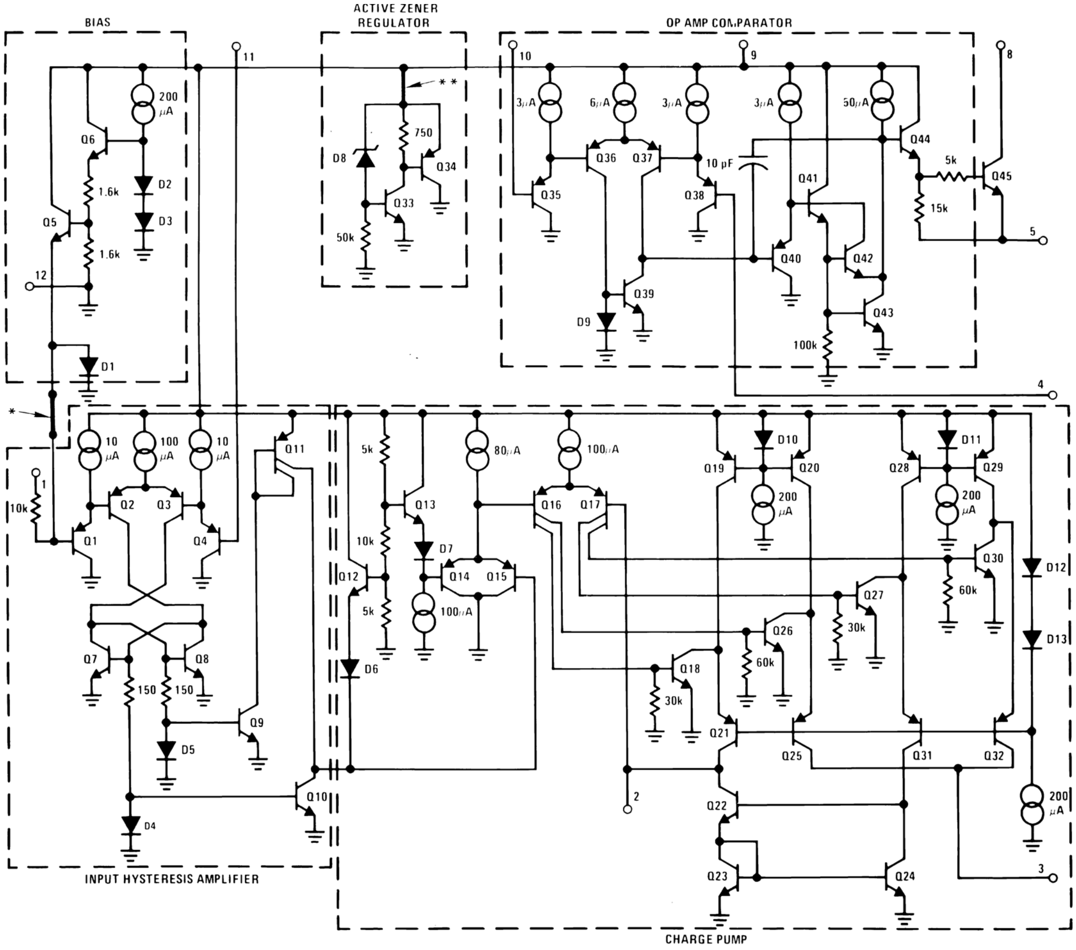
This average current will be flowing across R1, giving the output voltage in Equation 2.

$$Vo = R1 \times C1 \times V_{CC} \times f \quad (2)$$

C2 acts as a filter to smooth the pulses of current and does not affect the output voltage. However, the size of C2 determines both the output response time for changes in frequency and the amount of output voltage ripple.

The voltage generated is then fed in a high gain op amp. This op amp drives a bipolar transistor whose collector and emitter are each broken out to a pin. The LM29x7 has the flexibility to be configured a variety of ways to meet system requirements including voltage output, driving loads, operating a relay, and more.

9.2 Functional Block Diagram



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*This connection made on 8-pin LM2907 and LM2917 only.

**This connection made on LM2917 and 8-pin LM2917 only.

9.3 Feature Description

9.3.1 Differential Input

This device features a Schmitt-Trigger comparator that is the first stage in converting the input signal. Every time the output of the comparator flips between high and low correlates to a half cycle elapsing on the input signal. On the LM29x7-8 devices, one terminal of this comparator is internally connected to ground. This requires that the input signal cross zero volts in order for device to detect the frequency. On the LM29x7 devices, the input terminals to the Schmitt-Trigger comparator are both available for use. This open terminal allows the potential at which the comparator's output is flipped to be applied externally. This allows the device to accept signals with DC offset or compare differential inputs.

9.3.2 Configurable

While the ratio of output voltage to input frequency is dependent on supply voltage, it is easily adjusted through the combination of one resistor and one capacitor, R1 and C1. The formula for calculating the expected output voltage is in Equation 3.

$$V_{OUT} = V_{CC} \times f \times C1 \times R1. \quad (3)$$

The sizes of R1 and C1 have other effects on the system such as maximum frequency and output linearity. See *Choosing R1 and C1* for detailed instructions on sizing components.

Feature Description (continued)

9.3.3 Output Stage

The output voltage generated by the charge pump is fed in the noninverting terminal of a high gain op amp. This op amp then drives and uncommitted bipolar junction transistor. This allows the LM2907 to be configured a variety of ways to meet system needs. The output voltage can be buffered and used to drive a load (see Figure 15) or an output threshold can be given to trigger a load switch (see Figure 18).

9.4 Device Functional Modes

9.4.1 Grounded Input Devices (8-Pin LM2907 and LM2917)

These devices have one of the two Schmitt-Trigger comparator inputs internally grounded and must be externally connected to the system ground as well. This configuration monitors the remaining terminal for zero crossings.

9.4.2 Differential Input Devices (LM2907 and LM2917)

These devices have both inputs to the Schmitt-Trigger comparator available and broken out to pins 1 and 11. This configuration allows a new switching threshold provided in the case of signals with DC offset or to intake a differential pair and switch based on voltage difference.

10 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

10.1 Application Information

The LM2907 series of tachometer circuits is designed for minimum external part count applications and maximum versatility. To fully exploit its features and advantages, first examine its theory of operation. The first stage of operation is a differential amplifier driving a positive feedback flip-flop circuit. The input threshold voltage is the amount of differential input voltage at which the output of this stage changes state. Two options (8-pin LM2907 and LM2917) have one input internally grounded so that an input signal must swing above and below ground and exceed the input thresholds to produce an output. This is offered specifically for magnetic variable reluctance pickups which typically provide a single-ended AC output. This single input is also fully protected against voltage swings to ±28 V, which are easily attained with these types of pickups.

The differential input options (LM2907, LM2917) give the user the option of setting his own input switching level and still have the hysteresis around that level for excellent noise rejection in any application. Of course to allow the inputs to attain common-mode voltages above ground, input protection is removed and neither input should be taken outside the limits of the supply voltage being used. It is very important that an input not go below ground without some resistance in its lead to limit the current that will then flow in the epi-substrate diode.

Following the input stage is the charge pump where the input frequency is converted to a DC voltage. To do this requires one timing capacitor, one output resistor, and an integrating or filter capacitor. When the input stage changes state (due to a suitable zero crossing or differential voltage on the input) the timing capacitor is either charged or discharged linearly between two voltages whose difference is $V_{CC}/2$. Then in one half cycle of the input frequency or a time equal to 1/2 f_{IN} the change in charge on the timing capacitor is equal to $V_{CC}/2 \times C1$. The average amount of current pumped into or out of the capacitor is shown in Equation 4.

$$\frac{\Delta Q}{T} = i_{c(AVG)} = C1 \times \frac{V_{CC}}{2} \times (2 f_{IN}) = V_{CC} \times f_{IN} \times C1 \tag{4}$$

The output circuit mirrors this current very accurately into the load resistor R1, connected to ground, such that if the pulses of current are integrated with a filter capacitor, then $V_O = i_c \times R1$, and the total conversion formula becomes Equation 5.

$$V_O = V_{CC} \times f_{IN} \times C1 \times R1 \times K \tag{5}$$

where

- K is the gain constant (typically 1)

The size of C2 is dependent only on the amount of ripple voltage allowable and the required response time.

10.2 Typical Applications

10.2.1 Minimum Component Tachometer

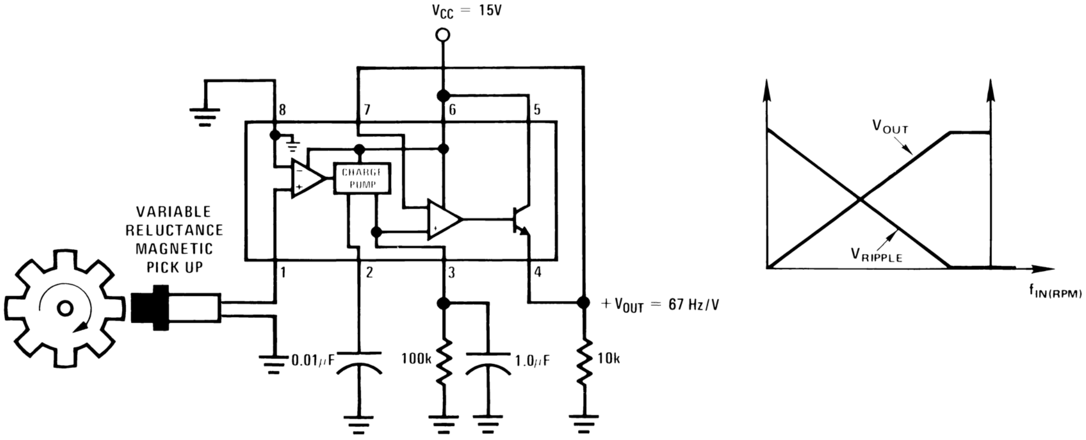


Figure 15. Minimum Component Tachometer Diagram

10.2.1.1 Design Requirements

- C1: This capacitor is charged and discharged every cycle by a 180-µA typical current source. Smaller capacitors can be charged quicker therefore increasing the maximum readable frequency. However, lower capacitors values reduce the output voltage produced for a given frequency. C1 must not be sized lower than 500-pF die to its role in internal compensation.
- R1: This resistor produces the output voltage from current pulses source by the internal charge pump. Higher values increase the output voltage for a given frequency, but too large will degrade the output's linearity. Because the current pulses are a fixed magnitude of 180 µA typical, R1 must be big enough to produce the maximum desired output voltage at maximum input frequency. At maximum input frequency the pulse train duty cycle is 100%, therefore the average current is 180 µA and R1 = Vo(max) / 180 µA.
- C2: This capacitor filters the ripple produced by the current pulses sourced by the charge pump. Large values reduce the output voltage ripple but increase the output's response time to changes in input frequency.
- Rload: The load resistance must be large enough that at maximum output voltage, the current is under the rated value of 50 mA.

10.2.1.2 Detailed Design Procedure

10.2.1.2.1 Choosing R1 and C1

There are some limitations on the choice of R1 and C1 which should be considered for optimum performance. The timing capacitor also provides internal compensation for the charge pump and must be kept larger than 500 pF for very accurate operation. Smaller values can cause an error current on R1, especially at low temperatures. Several considerations must be met when choosing R1. The output current at pin 3 is internally fixed and therefore V_O/R1 must be less than or equal to this value. If R1 is too large, it can become a significant fraction of the output impedance at pin 3 which degrades linearity. Also output ripple voltage must be considered and the size of C2 is affected by R1. An expression that describes the ripple content on pin 3 for a single R1C2 combination is in Equation 6.

$$V_{RIPPLE} = \frac{V_{CC}}{2} \times \frac{C1}{C2} \times \left(1 - \frac{V_{CC} \times f_{IN} \times C1}{I_2}\right) \text{pk-pk} \tag{6}$$

R1 can be chosen independent of ripple. However, response time, or the time it takes V_{OUT} to stabilize at a new voltage, increases as the size of C2 increases, so a compromise between ripple, response time, and linearity must be chosen carefully.

As a final consideration, the maximum attainable input frequency is determined by V_{CC}, C1, and I_2 in Equation 7.

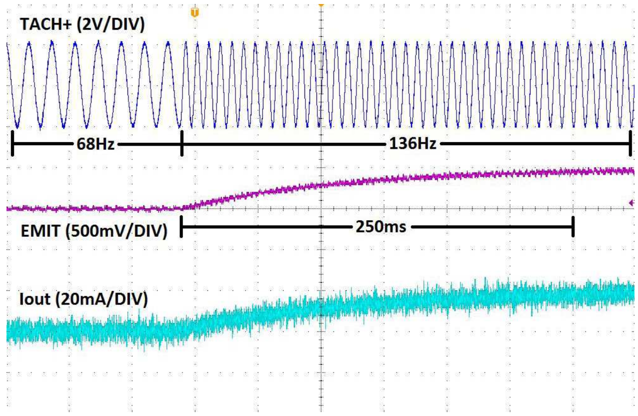
Typical Applications (continued)

$$f_{MAX} = \frac{I_2}{C1 \times V_{CC}} \qquad (7)$$

10.2.1.2.2 Using Zener Regulated Options (LM2917)

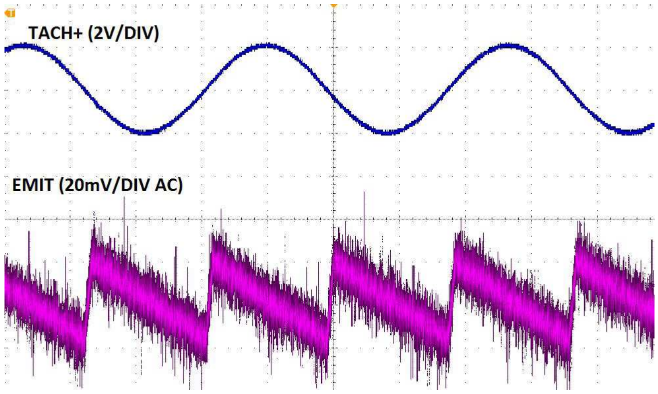
For those applications where an output voltage or current must be obtained independent of supply voltage variations, the LM2917 is offered. The most important consideration in choosing a dropping resistor from the unregulated supply to the device is that the tachometer and op amp circuitry alone require about 3 mA at the voltage level provided by the Zener. At low supply voltages there must be some current flowing in the resistor above the 3-mA circuit current to operate the regulator. As an example, if the raw supply varies from 9 V to 16 V, a resistance of 470 Ω minimizes the Zener voltage variation to 160 mV. If the resistance goes under 400 Ω or over 600 Ω, the Zener variation quickly rises above 200 mV for the same input variation.

10.2.1.3 Application Curves



C1 = .01 µF C2 = 1 µF R1 = 100 kΩ
Rdrop = 910 Ω Zener Regulated V_{CC} = 7.58 V

Figure 16. Output Response to an Increase in Input Frequency

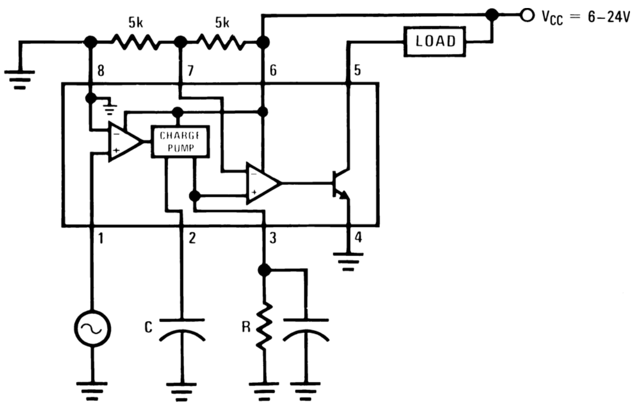


C1 = .01 µF C2 = 1 µF R1 = 100 kΩ
Rdrop = 910 Ω Zener Regulated V_{CC} = 7.58 V

Figure 17. Output Voltage Ripple

10.2.2 Other Application Circuits

This section shows application circuit examples using the LM2907-N and LM2917-N devices. Customers must fully validate and test these circuits before implementing a design based on these examples.



Load is energized when $f_{IN} \geq (1 / (2 \times R_C))$

Figure 18. Speed Switch

Typical Applications (continued)

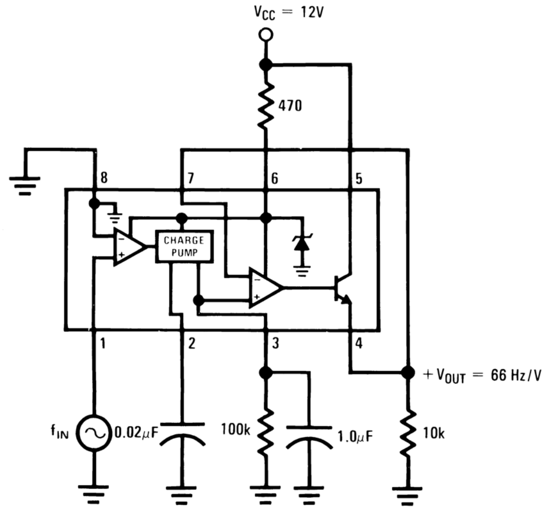


Figure 19. Zener Regulated Frequency to Voltage Converter

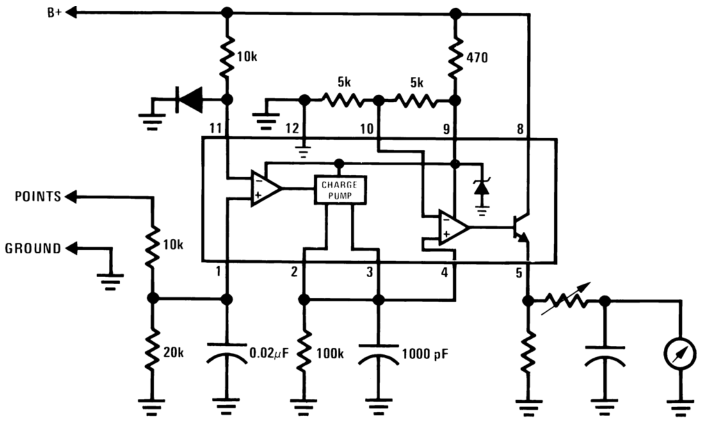
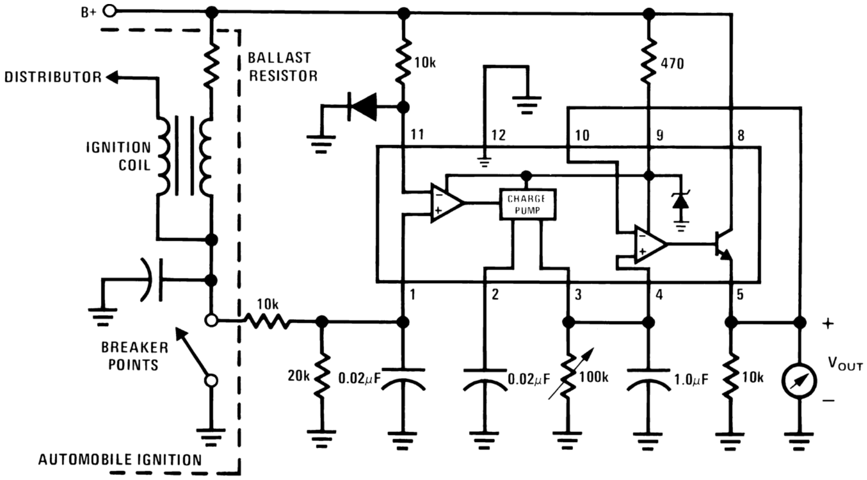


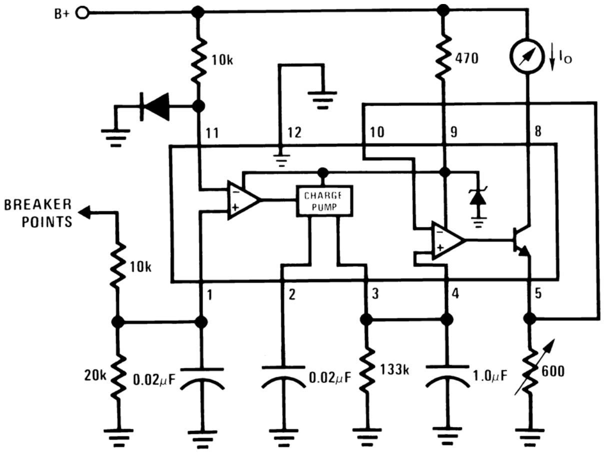
Figure 20. Breaker Point Dwell Meter

Typical Applications (continued)



V_O = 6 V at 400 Hz or 6000 ERPM (8 Cylinder Engine)

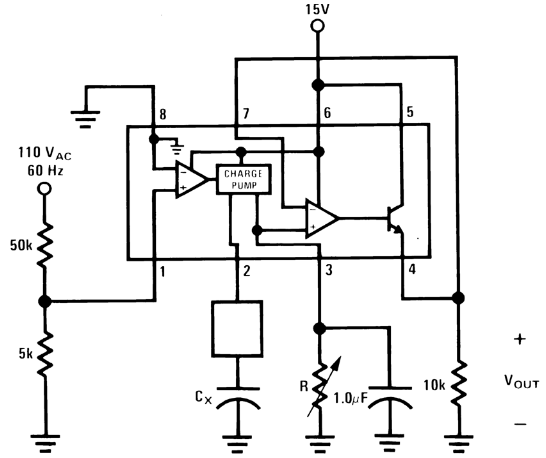
Figure 21. Voltage Driven Meter Indicating Engine RPM



I_O = 10 mA at 300 Hz or 6000 ERPM (6 Cylinder Engine)

Figure 22. Current Driven Meter Indicating Engine RPM

Typical Applications (continued)



V_{OUT} = 1 V to 10 V for CX = 0.01 to 0.1 mFd and R = 111 kΩ

Figure 23. Capacitance Meter

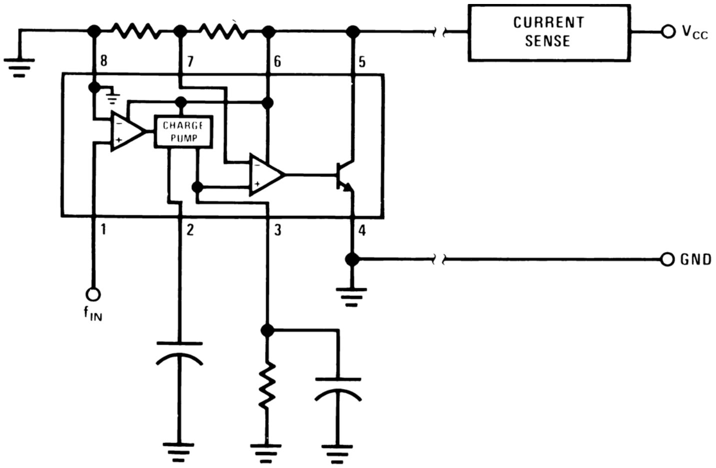
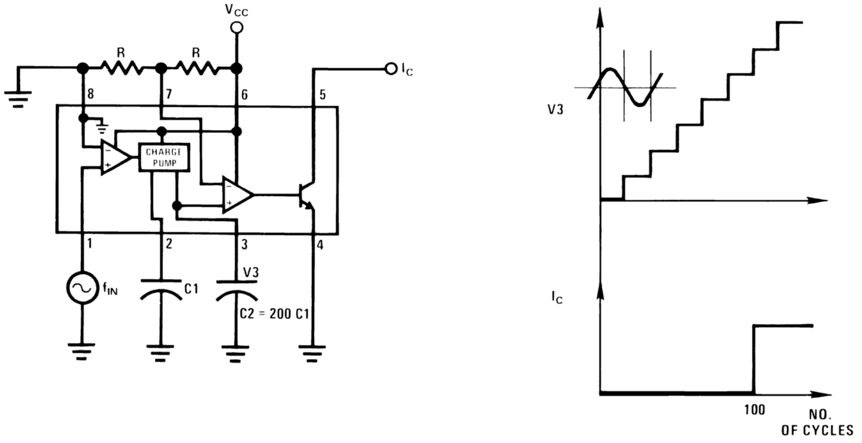


Figure 24. Two-Wire Remote Speed Switch

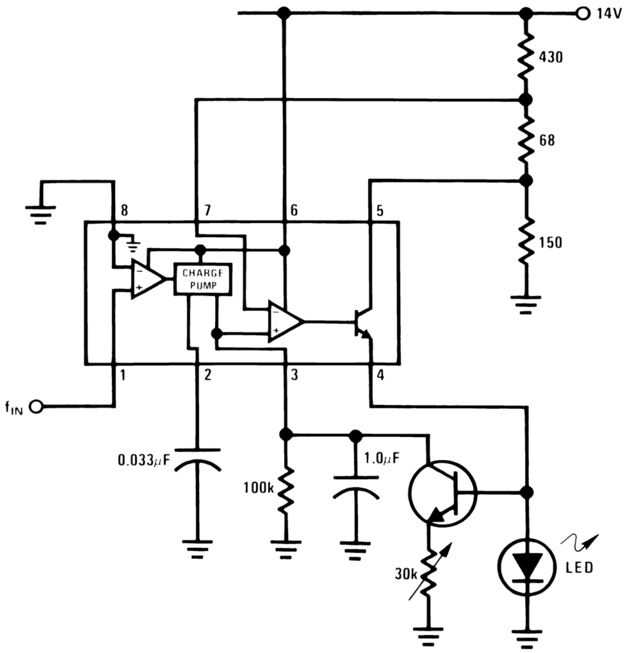
Typical Applications (continued)



V3 steps up in voltage by the amount of (V_{CC} × C1) / C2, for each complete input cycle (2 zero crossings).

For example: if C2 = 200 × C1 after 100 consecutive input cycles, then V3 = 1/2 × V_{CC}.

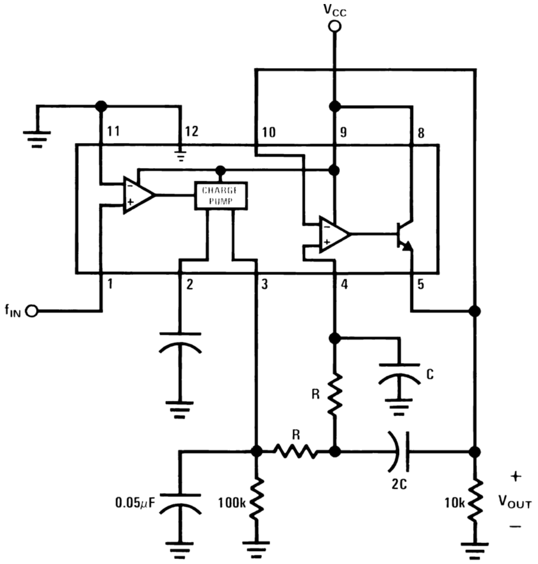
Figure 25. 100 Cycle Delay Switch



Flashing begins when f_{IN} ≥ 100 Hz

Flash rate increases with input frequency increase beyond trip point.

Figure 26. Flashing LED Indicates Over-Speed

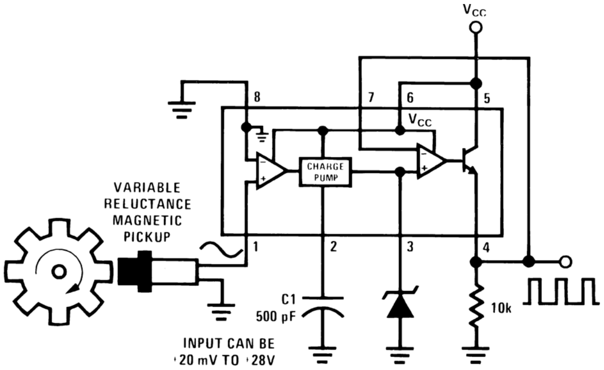


$f_{POLE} = 0.707 / (2 \times \pi \times RC)$

$\tau_{RESPONSE} = 2.57 / (2 \times \pi \times f_{POLE})$

Figure 27. Frequency to Voltage Converter With 2 Pole Butterworth Filter to Reduce Ripple

10.2.2.1 Variable Reluctance Magnetic Pickup Buffer Circuits



Precision two-shot output frequency is twice the input frequency

Pulse width = $(V_{CC} / 2) \times (C1 / 12)$

Pulse height = V_{ZENER}

Figure 28. Magnetic Pickup Buffer With Zener Regulated Output Magnitude

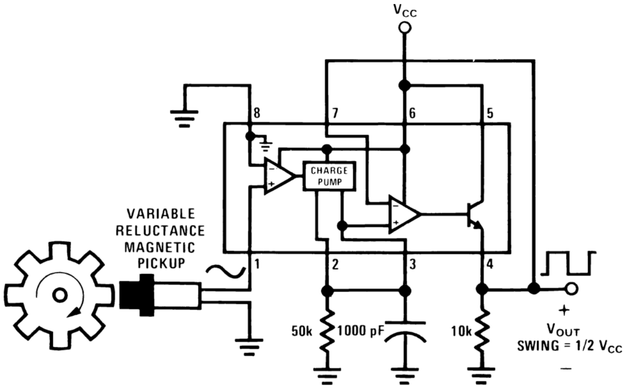


Figure 29. Magnetic Pickup Buffer With 1/2 V_{CC} Output Magnitude

10.2.2.2 Finger Touch or Contact Switch

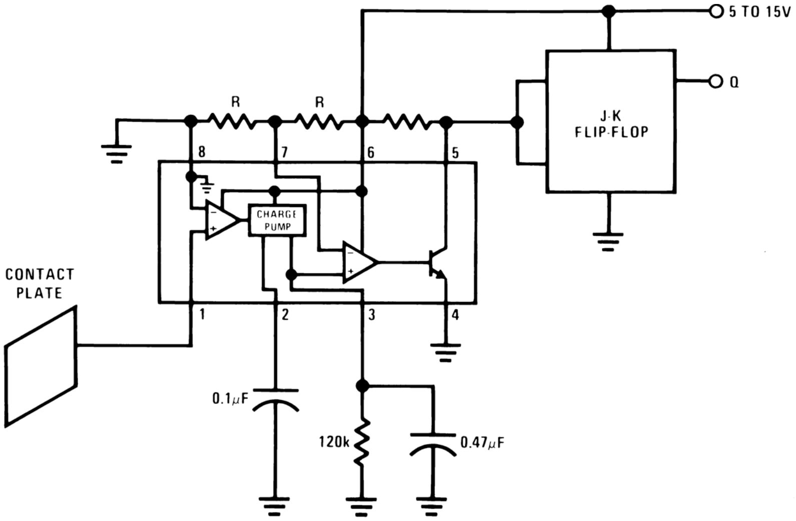


Figure 30. Finger Touch or Contact Switch Diagram

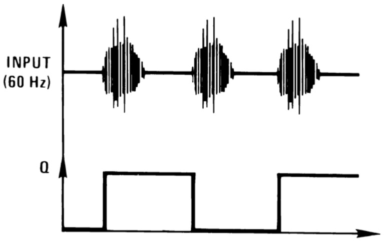
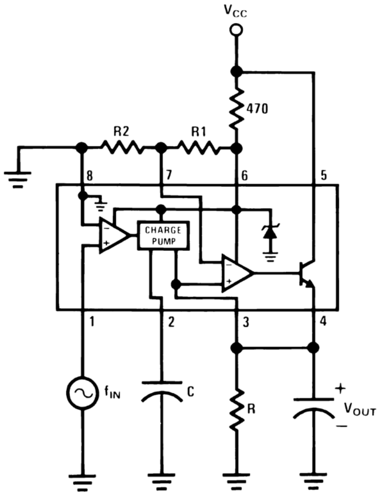


Figure 31. System Output in Response to Consecutive Button Presses

10.2.2.3 Over-Speed Latch



Output latches when $f_{IN} = (R2 / (R1 + R2)) \times (1 / RC)$.

Output is reset by removing V_{CC}.

Figure 32. Over-Speed Latch Circuit Diagram

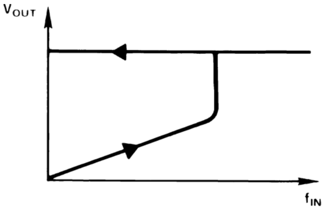


Figure 33. V_{OUT} vs F_{IN}

10.2.2.4 Frequency Switch Applications

Some frequency switch applications may require hysteresis in the comparator function which can be implemented in several ways. Example circuits are shown in Figure 34 to Figure 36.

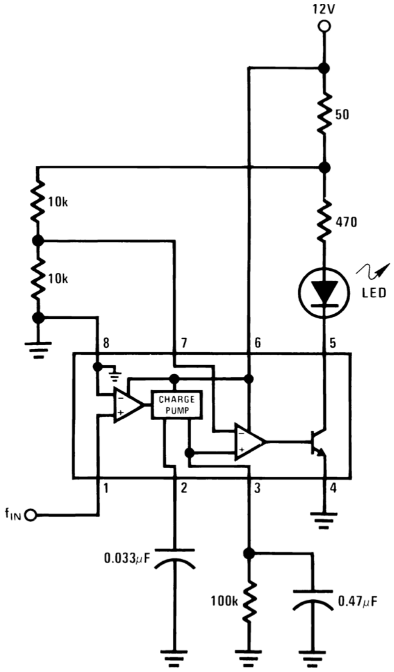


Figure 34. Frequency Switch With Resistor Divider Threshold

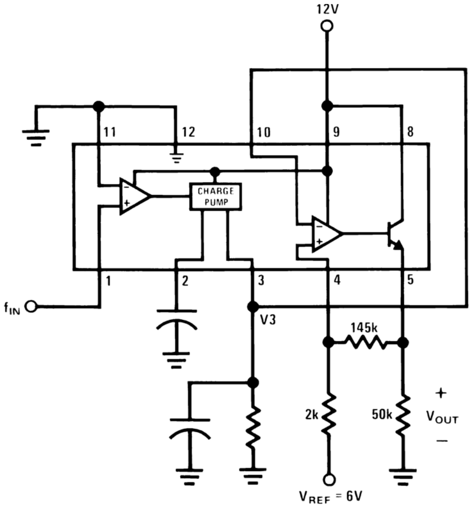


Figure 35. Frequency Switch With Added Hysteresis

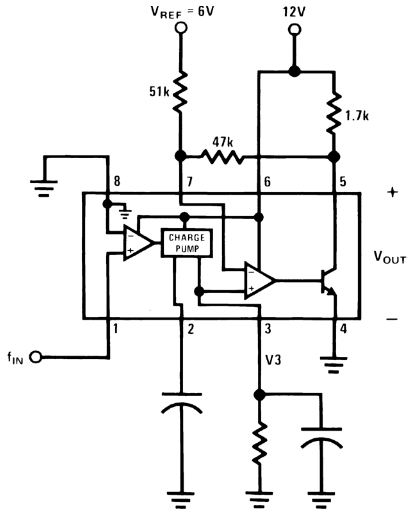


Figure 36. Frequency Switch With Added Hysteresis

10.2.2.4.1 Application Curves

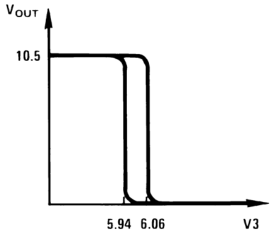


Figure 37. V_{OUT} vs V3

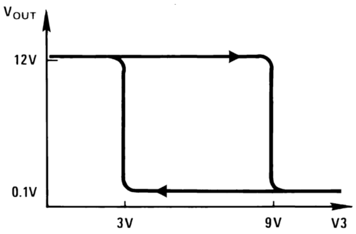


Figure 38. V_{OUT} vs V3

10.2.2.5 Anti-Skid Circuits

10.2.2.5.1 *Select-Low* Circuit

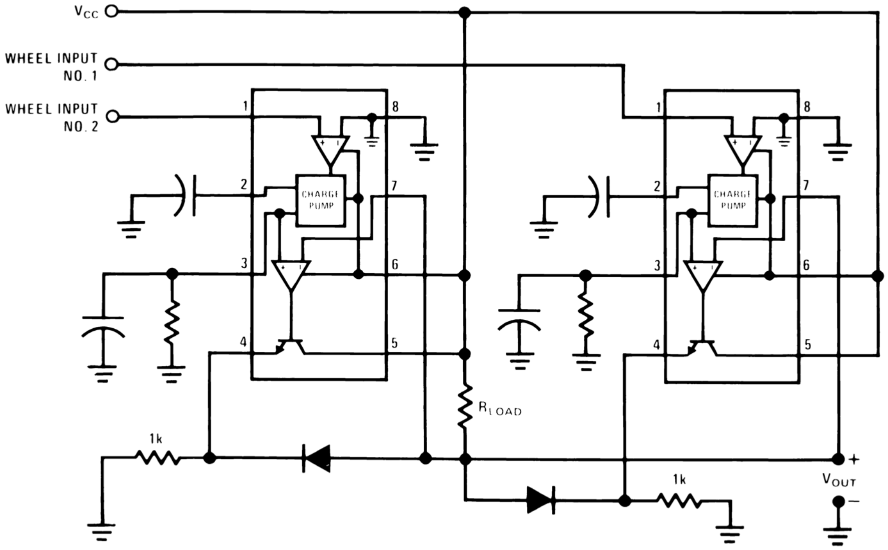
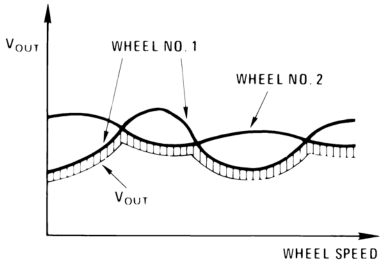


Figure 39. *Select-Low* Circuit Diagram



V_{OUT} is proportional to the lower of the two input wheel speeds

Figure 40. V_{OUT} vs Wheel Speed

10.2.2.5.2 *Select-High* Circuit

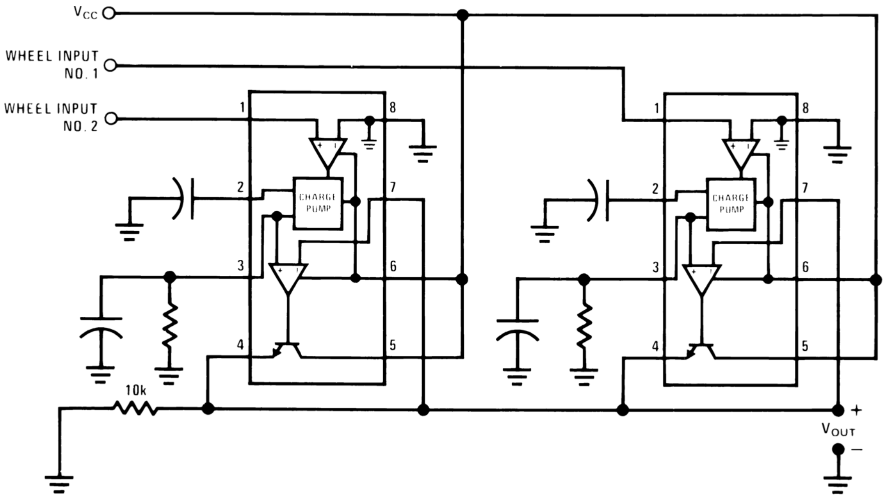
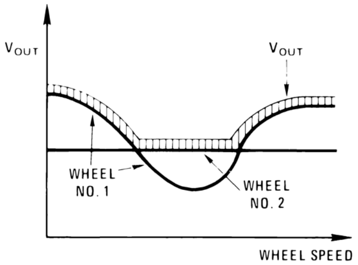


Figure 41. *Select-High* Circuit Diagram



V_{OUT} is proportional to the higher of the two input wheel speeds

Figure 42. V_{OUT} vs Wheel Speed

10.2.2.5.3 *Select-Average* Circuit

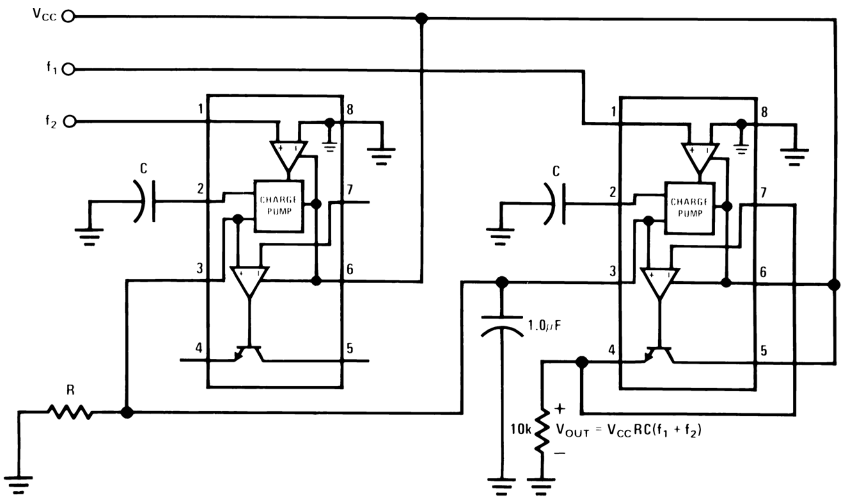


Figure 43. *Select-Average* Circuit Diagram

10.2.2.6 Changing the Output Voltage for an Input Frequency of Zero

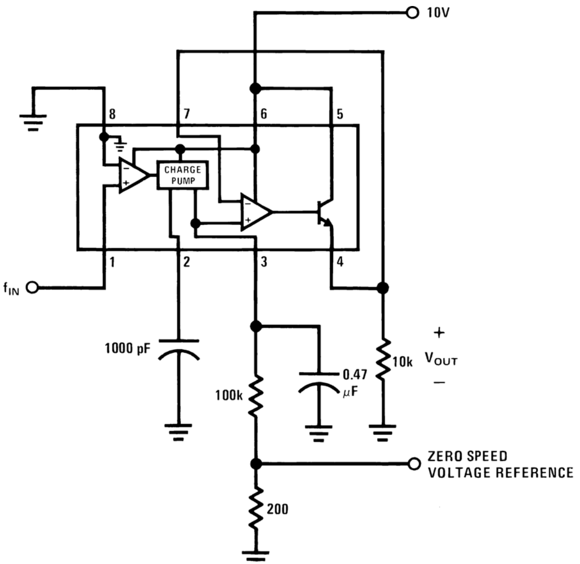


Figure 44. Tachometer With Adjustable Zero Speed Voltage Output

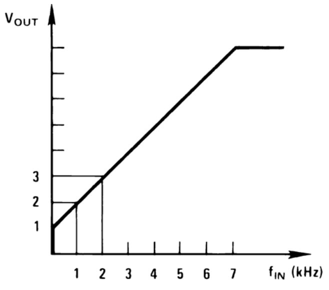


Figure 45. V_{OUT} vs Frequency Plot Shifted to Produce 1 V at Zero Speed

10.2.2.7 Changing Tachometer Gain Curve or Clamping the Minimum Output Voltage

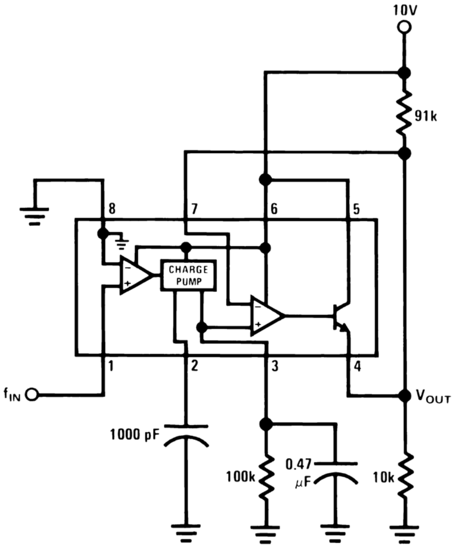


Figure 46. Tachometer With Output Clamped at Low Speeds

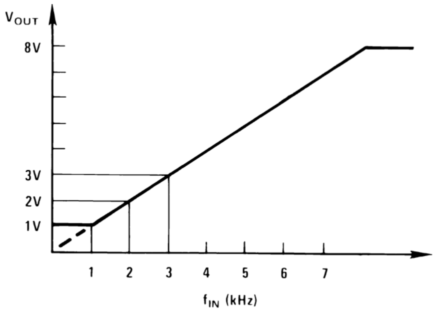


Figure 47. V_{OUT} vs Frequency Plot With Output Clamped at Low Speeds

11 Power Supply Recommendations

This family of devices is designed to operate from a supply voltage up to 28 V. For the 8-pin LM2907 and LM2917, devices with a fixed ground reference for TACH–, the tachometer inputs can intake voltages between ±28 V. LM2907 and LM2917 devices have both tachometer inputs available at the cost of input protection features. This means neither input should be taken outside of the supply voltage range without additional precautions (see *Application Information*).

12 Layout

12.1 Layout Guidelines

- Bypass capacitors must be placed as close as possible to the supply pin. When using a through-hole package, it is acceptable to place the bypass capacitor on the bottom layer. All other components must be placed as close to the device as possible.
- Use of a ground plane is recommended to provide a low-impedance ground across the circuit.
- Feedback loops must use short and wide traces.

12.2 Layout Example

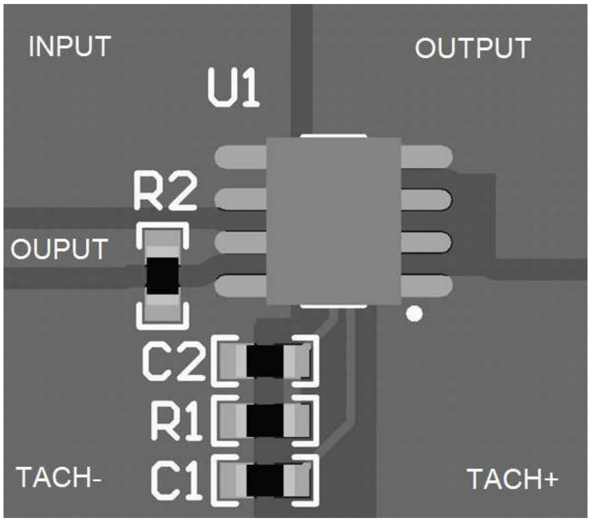


Figure 48. Layout Recommendation

13 Device and Documentation Support

13.1 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 1. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
LM2907-N	Click here	Click here	Click here	Click here	Click here
LM2917-N	Click here	Click here	Click here	Click here	Click here

13.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

13.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

13.4 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

13.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

13.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

14 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM2907M	NRND	SOIC	D	14	55	TBD	Call TI	Call TI	-40 to 85	LM2907M	
LM2907M-8	NRND	SOIC	D	8	95	TBD	Call TI	Call TI	-40 to 85	LM29 07M-8	
LM2907M-8/NOPB	ACTIVE	SOIC	D	8	95	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	LM29 07M-8	Samples
LM2907M/NOPB	ACTIVE	SOIC	D	14	55	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	LM2907M	Samples
LM2907MX	NRND	SOIC	D	14	2500	TBD	Call TI	Call TI	-40 to 85	LM2907M	
LM2907MX-8/NOPB	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	LM29 07M-8	Samples
LM2907MX/NOPB	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	LM2907M	Samples
LM2907N-8/NOPB	ACTIVE	PDIP	P	8	40	Green (RoHS & no Sb/Br)	CU SN	Level-1-NA-UNLIM	-40 to 85	LM 2907N-8	Samples
LM2907N/NOPB	ACTIVE	PDIP	NFF	14	25	Green (RoHS & no Sb/Br)	CU SN	Level-1-NA-UNLIM	-40 to 85	LM2907N	Samples
LM2917M-8	NRND	SOIC	D	8	95	TBD	Call TI	Call TI	-40 to 85	LM29 17M-8	
LM2917M-8/NOPB	ACTIVE	SOIC	D	8	95	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	LM29 17M-8	Samples
LM2917M/NOPB	ACTIVE	SOIC	D	14	55	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	LM2917M	Samples
LM2917MX-8	NRND	SOIC	D	8	2500	TBD	Call TI	Call TI	-40 to 85	LM29 17M-8	
LM2917MX-8/NOPB	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	LM29 17M-8	Samples
LM2917MX/NOPB	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	LM2917M	Samples
LM2917N-8/NOPB	ACTIVE	PDIP	P	8	40	Green (RoHS & no Sb/Br)	CU SN	Level-1-NA-UNLIM	-40 to 85	LM 2917N-8	Samples
LM2917N/NOPB	ACTIVE	PDIP	NFF	14	25	Green (RoHS & no Sb/Br)	CU SN	Level-1-NA-UNLIM	-40 to 85	LM2917N	Samples

[1] The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

[2] Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

[3] MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

[4] There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

[5] Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

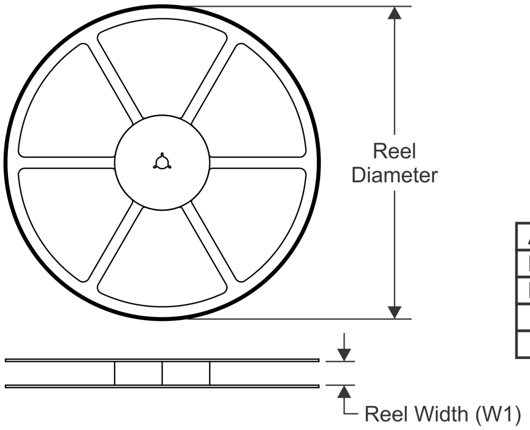
[6] Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

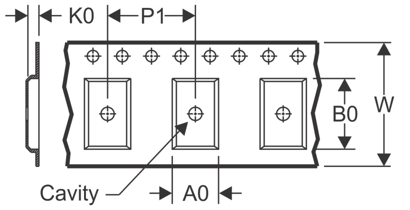
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

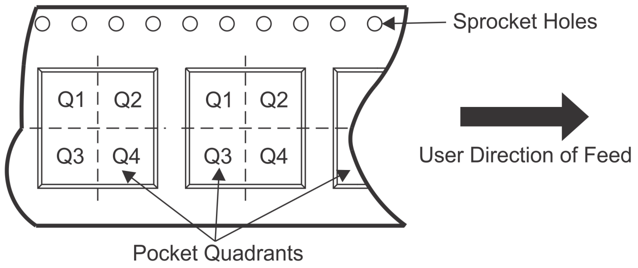


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

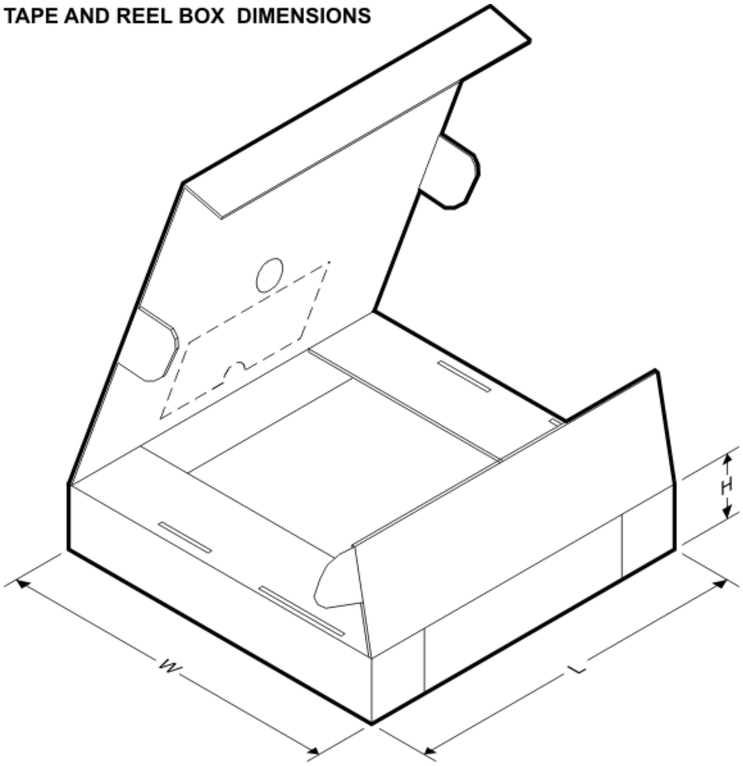
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM2907MX	SOIC	D	14	2500	330.0	16.4	6.5	9.35	2.3	8.0	16.0	Q1
LM2907MX-8/NOPB	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1
LM2907MX/NOPB	SOIC	D	14	2500	330.0	16.4	6.5	9.35	2.3	8.0	16.0	Q1
LM2917MX-8	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1
LM2917MX-8/NOPB	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1
LM2917MX/NOPB	SOIC	D	14	2500	330.0	16.4	6.5	9.35	2.3	8.0	16.0	Q1

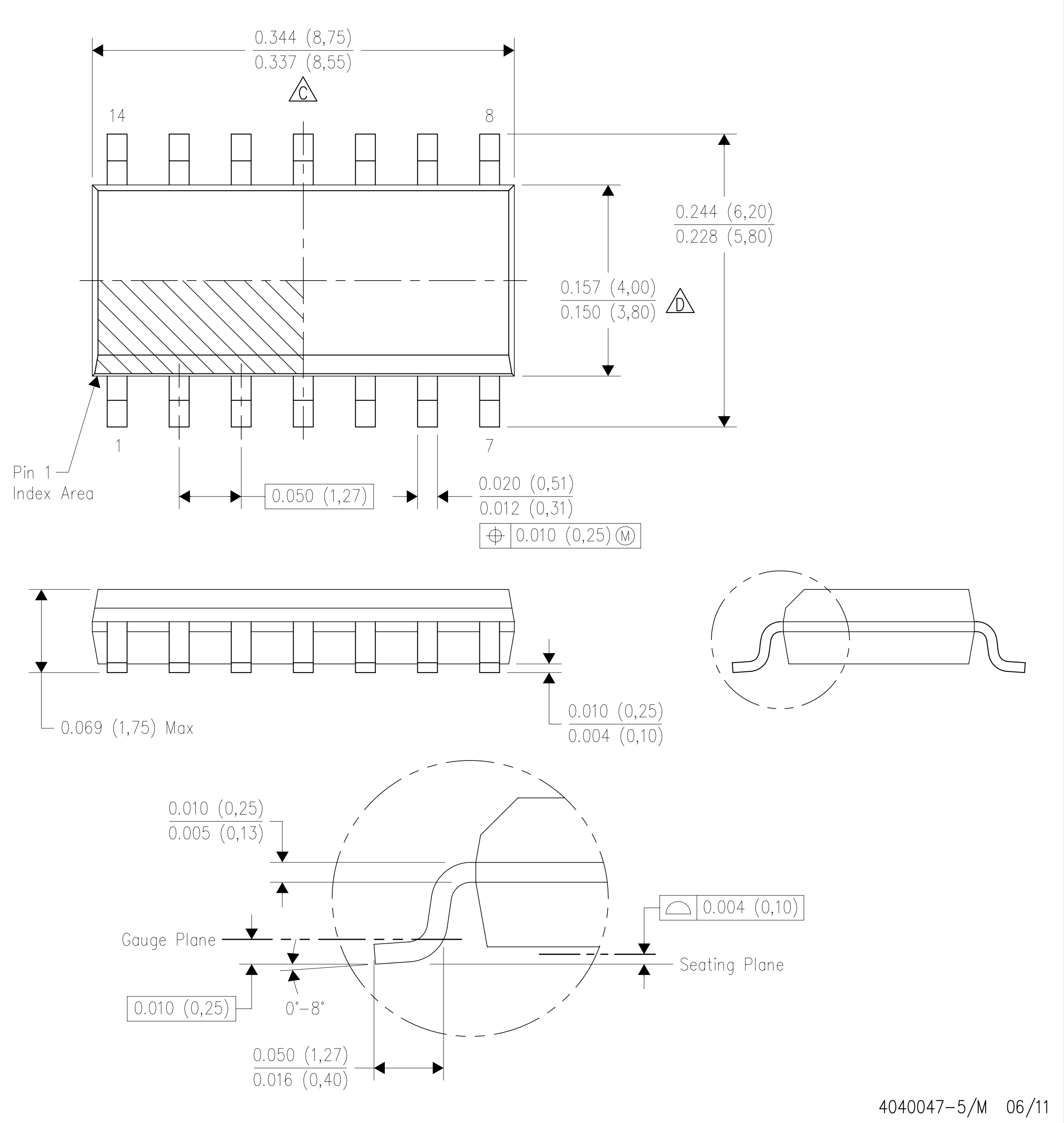
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

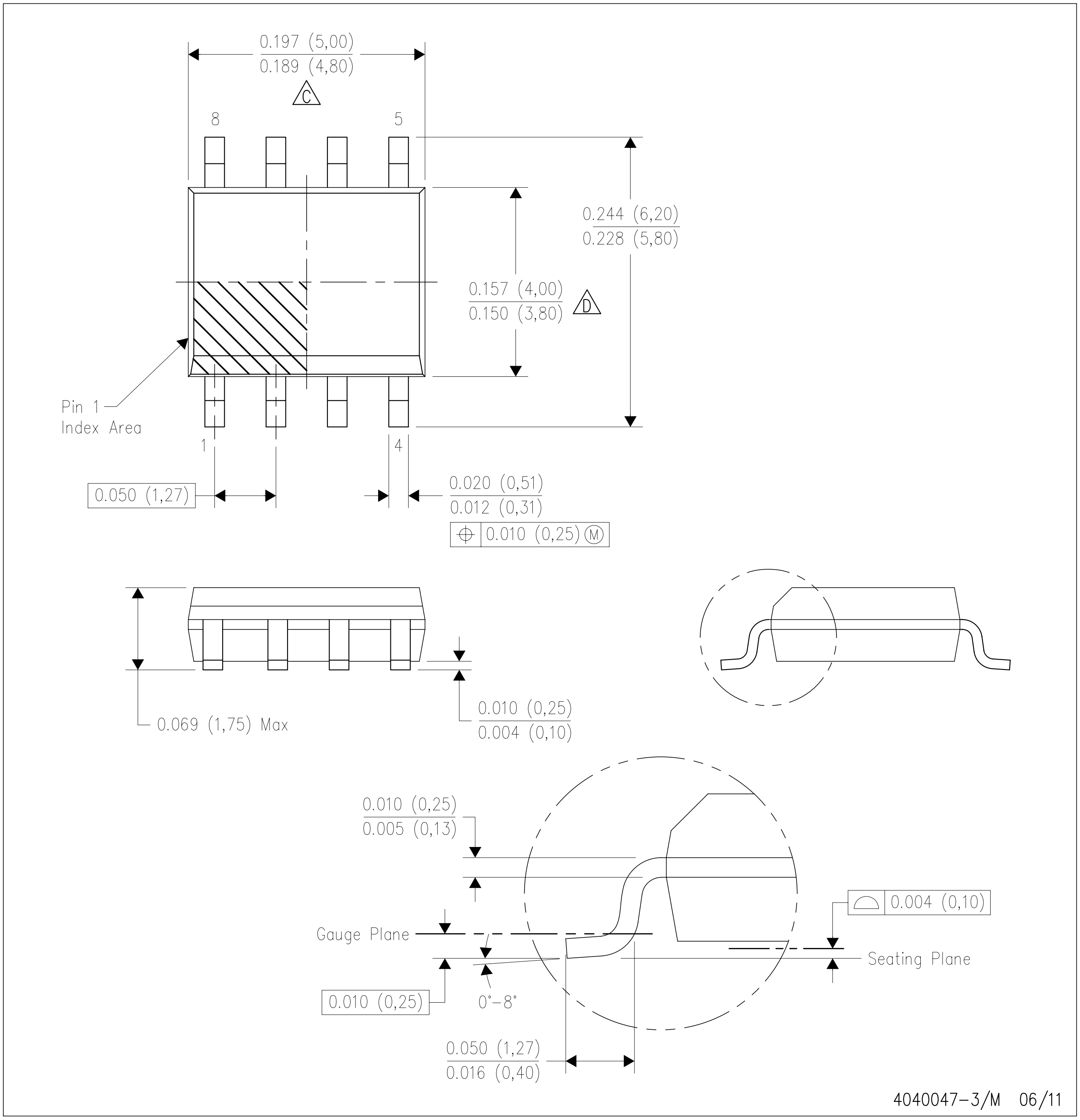
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM2907MX	SOIC	D	14	2500	367.0	367.0	35.0
LM2907MX-8/NOPB	SOIC	D	8	2500	367.0	367.0	35.0
LM2907MX/NOPB	SOIC	D	14	2500	367.0	367.0	35.0
LM2917MX-8	SOIC	D	8	2500	367.0	367.0	35.0
LM2917MX-8/NOPB	SOIC	D	8	2500	367.0	367.0	35.0
LM2917MX/NOPB	SOIC	D	14	2500	367.0	367.0	35.0

D (R–PDSO–G14) PLASTIC SMALL OUTLINE



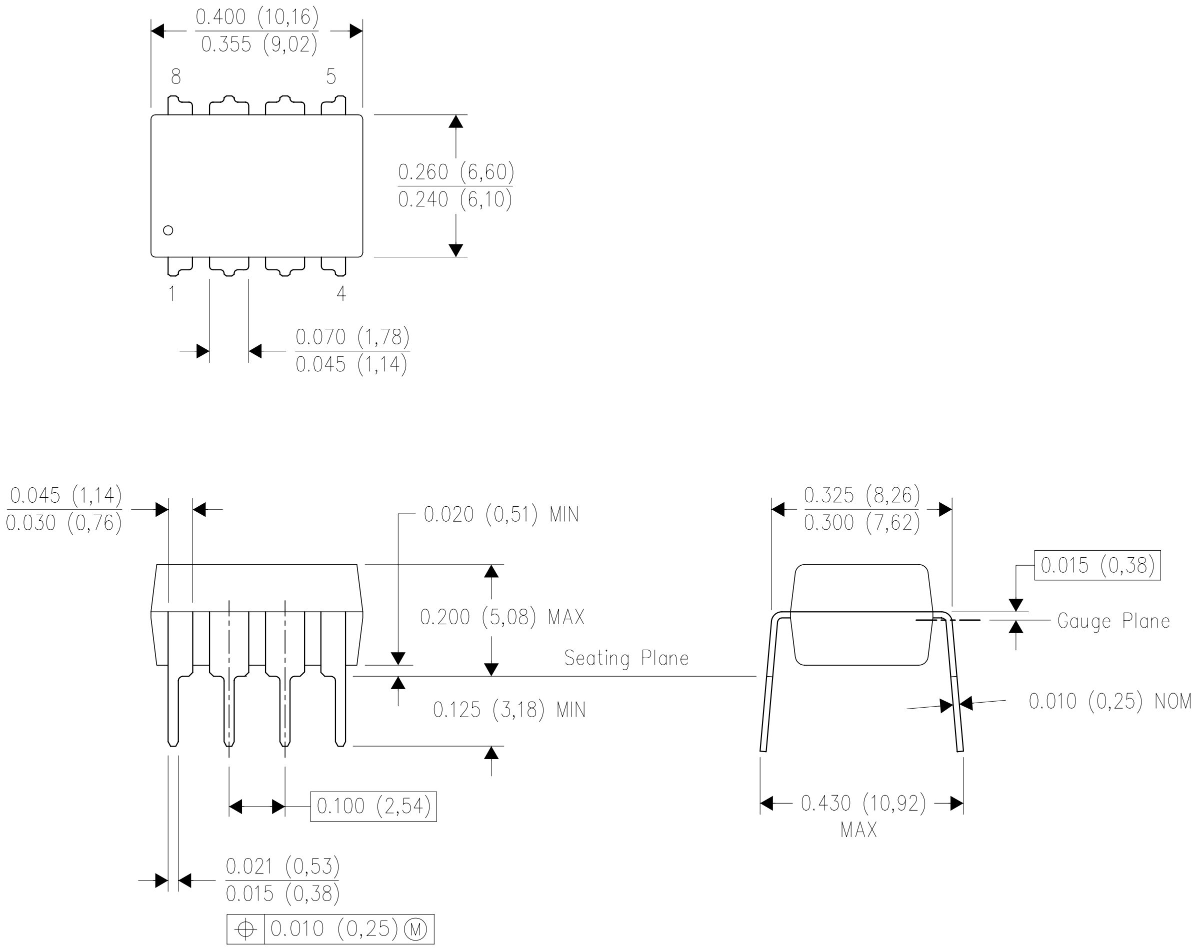
NOTES:
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
- D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
- E. Reference JEDEC MS–012 variation AB.

D (R-PDSO-G8) PLASTIC SMALL OUTLINE



NOTES:
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- △C Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
- △D Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
- E. Reference JEDEC MS–012 variation AA.

P (R–PDIP–T8) PLASTIC DUAL–IN–LINE PACKAGE



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NOTES:
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Falls within JEDEC MS–001 variation BA.

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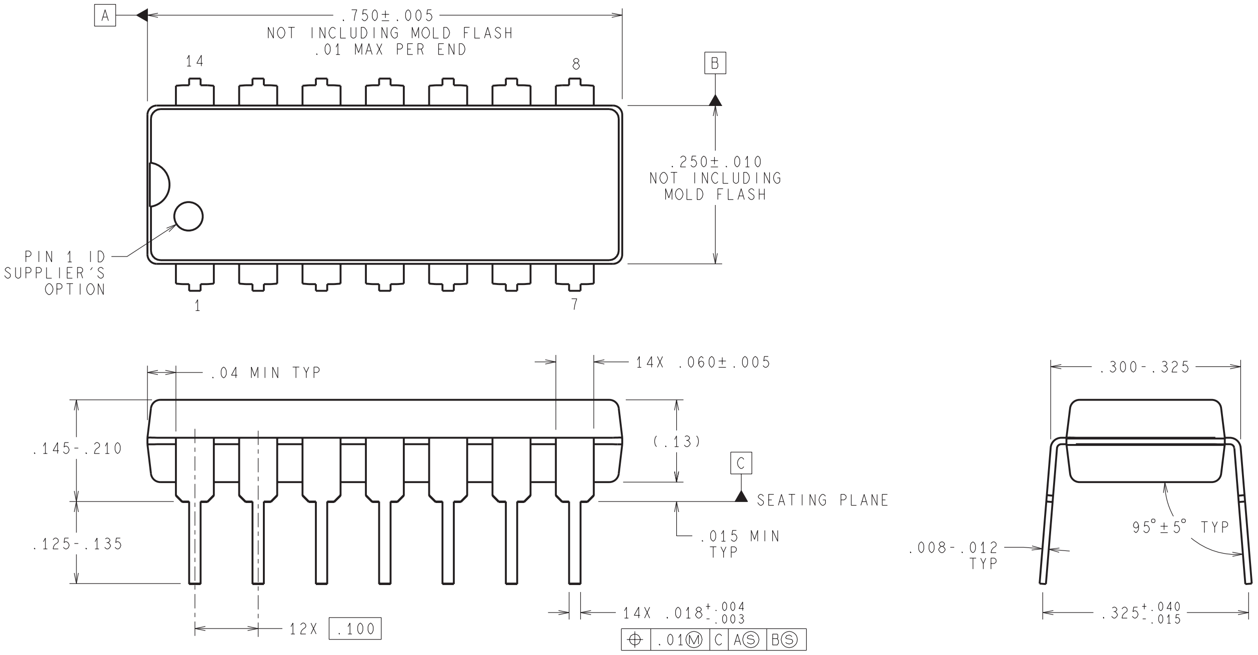

DIMENSIONS ARE IN INCHES

DIMENSIONS IN ( ) FOR REFERENCE ONLY

N14A (Rev G)

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