Dual 4-A Peak High-Speed Low-Side Power-MOSFET Drivers

Check for Samples: UCC27323, UCC27324, UCC27325, UCC37323, UCC37324, UCC37325

FEATURES

- Industry-Standard Pin-Out
- High Current-Drive Capability of ±4 A at the Miller Plateau Region
- Efficient Constant-Current Sourcing Even at Low Supply Voltages
- TTL/CMOS Compatible Inputs Independent of Supply Voltage
- 20-ns Typical Rise and 15-ns Typical Fall Times with 1.8-nF Load
- Typical Propagation-Delay Times of 25 ns with Input Falling and 35 ns with Input Rising
- 4.5-V to 15-V Supply Voltage
- Supply Current of 0.3 mA
- Dual Outputs are Paralleled for Higher Drive Current
- Available in Thermally Enhanced MSOP PowerPAD™ Package with 4.7°C/W θ_{JC}
- Rated From –40°C to +125°C
- TrueDrive™ Output Architecture Using Bipolar and CMOS Transistors in Parallel

APPLICATIONS

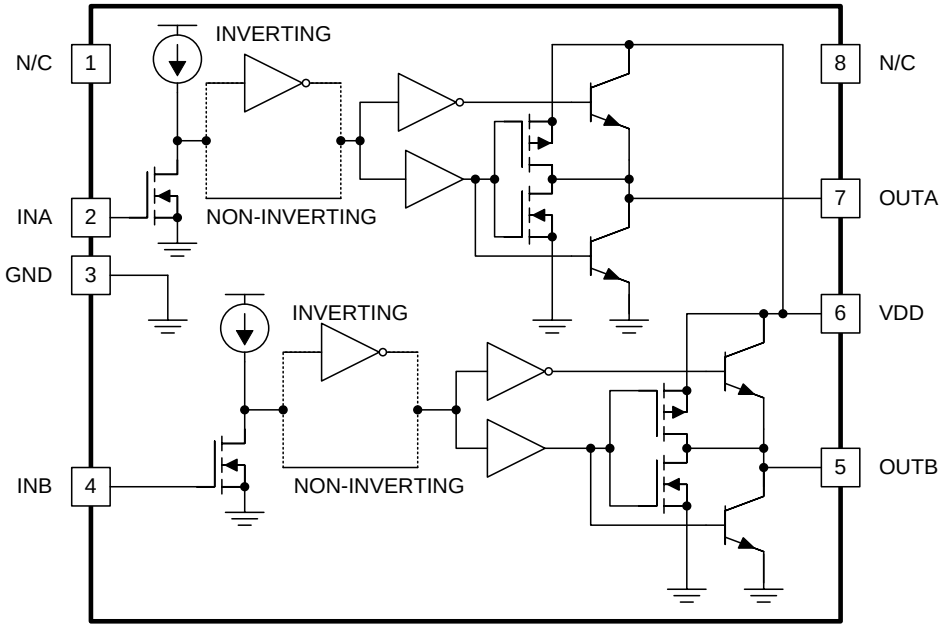
- Switch-Mode Power Supplies
- DC/DC Converters
- Motor Controllers
- Line Drivers
- Class D Switching Amplifiers

DESCRIPTION

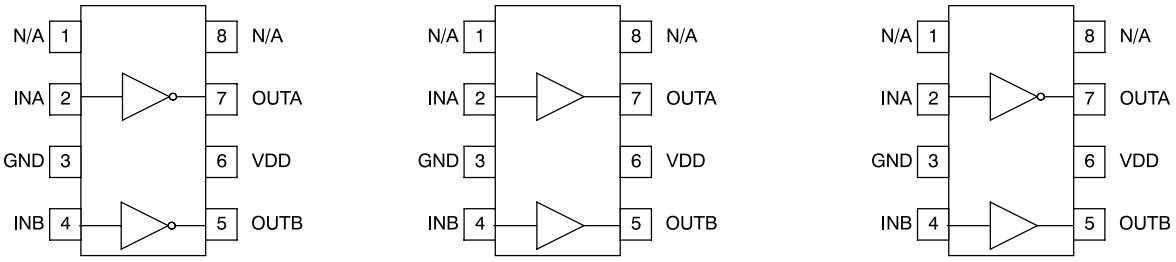
The UCC37323/4/5 family of high-speed dual-MOSFET drivers deliver large peak currents into capacitive loads. Three standard logic options are offered — dual-inverting, dual-noninverting, and one-inverting and one-noninverting driver. The thermally enhanced 8-pin PowerPAD MSOP package (DGN) drastically lowers the thermal resistance to improve long-term reliability. UCC3732x is also offered in the standard SOIC-8 (D) or PDIP-8 (P) packages.

Using a design that inherently minimizes shoot-through current, these drivers deliver 4-A of current where it is needed most at the Miller plateau region during the MOSFET switching transition. A unique BiPolar and MOSFET hybrid output stage in parallel also allows efficient current sourcing and sinking at low supply voltages.

BLOCK DIAGRAM



D, DGN, OR P PACKAGE
(TOP VIEW)



(DUAL INVERTING) (DUAL NONINVERTING) (ONE INVERTING, ONE NONINVERTING)

ORDERING INFORMATION(1)

OUTPUT CONFIGURATION	TEMPERATURE RANGE $T_A = T_J$	PACKAGED DEVICES		
		SOIC-8 (D)	MSOP-8 PowerPAD (DGN)(2)	PDIP-8 (P)
Dual inverting	–40°C to +125°C	UCC27323D	UCC27323DGN	UCC27323P
	0°C to +70°C	UCC37323D	UCC37323DGN	UCC37323P
Dual nonInverting	–40°C to +125°C	UCC27324D	UCC27324DGN	UCC27324P
	0°C to +70°C	UCC37324D	UCC37324DGN	UCC37324P
One inverting, one noninverting	–40°C to +125°C	UCC27325D	UCC27325DGN	UCC27325P
	0°C to +70°C	UCC37325D	UCC37325DGN	UCC37325P

(1) D (SOIC-8) and DGN (PowerPAD-MSOP) packages are available taped and reeled. Add R suffix to device type (for example UCC27323DR, UCC27324DGNR) to order quantities of 2,500 devices per reel for D or 1,000 devices per reel for DGN package.
(2) The PowerPAD is not directly connected to any leads of the package. However, the PowerPAD is electrically and thermally connected to the substrate which is the ground of the device.

POWER DISSIPATION RATINGS

PACKAGE	SUFFIX	θ_{JC} (°C/W)	θ_{JA} (°C/W)	Power Rating (mW) T_A = 70°C(1)	Derating Factor Above 70°C (mW/°C)(1)
SOIC-8	D	42	84 to 160(2)	344 to 655(3)	6.25 to 11.9(3)
PDIP-8	P	49	110	500	9
MSOP PowerPAD-8(2)	DGN	4.7	50 to 59(2)	1370	17.1

(1) 125°C operating junction temperature is used for power rating calculations.
(2) The PowerPAD is not directly connected to any leads of the package. However, it is electrically and thermally connected to the substrate which is the ground of the device.
(3) The range of values indicates the effect of pc-board. These values are intended to give the system designer an indication of the best and worst case conditions. In general, the system designer should attempt to use larger traces on the pc-board where possible in order to spread the heat away form the device more effectively. For information on the PowerPAD package, refer to Technical Brief, *PowerPad Thermally Enhanced Package*, Texas Instrument's Literature Number SLMA002, and Application Brief, *PowerPad Made Easy*, Texas Instruments Literature Number SLMA004.

Table 1. INPUT/OUTPUT TABLE

INPUTS (VIN_L, VIN_H)		UCC37323		UCC37324		UCC37325	
INA	INB	OUTA	OUTB	OUTA	OUTB	OUTA	OUTB
L	L	H	H	L	L	H	L
L	H	H	L	L	H	H	H
H	L	L	H	H	L	L	L
H	H	L	L	H	H	L	H

ABSOLUTE MAXIMUM RATINGS(1)(2)

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
	Analog input voltage (INA, INB)		–0.3 to V_{DD} + 0.3 V	not to exceed 16	V
	Output body diode DC current (OUTA, OUTB)			0.2	A
I_{OUT_DC}	Output current (OUTA, OUTB)	DC		0.2	A
I_{OUT_PULSED}		Pulsed (0.5 µs)		4.5	A
	Power dissipation at T_A = 25°C	D package		1.14	W
		DGN package		2.12	W
		P package		780	mW
	Output voltage (OUTA, OUTB)			16	V
V_{DD}	Supply voltage		–0.3	16	V
T_J	Junction operating temperature		–55	150	°C
T_{stg}	Storage temperature		–65	150	°C
	Lead temperature (soldering, 10 sec.)			300	°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages are with respect to GND. Currents are positive into, negative out of the specified terminal.

ELECTRICAL CHARACTERISTICS

V_{DD} = 4.5 to 15 V, T_A = T_J (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
INPUT (INA, INB)						
V_{IN_H}	Logic 1 input threshold		2			V
V_{IN_L}	Logic 0 input threshold				1	V
	Input current	0 V ← V_{IN} ← V_{DD}	–10		10	µA
OUTPUT (OUTA, OUTB)						
	Output current	V_{DD} = 14 V(1)		4		V
V_{OH}	High-level output voltage	V_{OH} = V_{DD} – V_{OUT}, I_{OUT} = –10 mA		300	450	mV
V_{OL}	Low-level output level	I_{OUT} = 10 mA		22	45	mV
	Output resistance high	T_A = 25°C, I_{OUT} = –10 mA, V_{DD} = 14 V(2)	25	30	35	Ω
		T_A = full range, I_{OUT} = –10 mA, V_{DD} = 14 V(2)	18		42	Ω
	Output resistance low	T_A = 25°C, I_{OUT} = 10 mA, V_{DD} = 14 V(2)	1.9	2.2	2.5	Ω
		T_A = full range, I_{OUT} = 10 mA, V_{DD} = 14 V(2)	1.2		4	Ω
	Latch-up protection		500			mA

(1) The pullup and pulldown circuits of the driver are bipolar and MOSFET transistors in parallel. The pulsed output current rating is the combined current from the bipolar and MOSFET transistors.
(2) The pullup and pulldown circuits of the driver are bipolar and MOSFET transistors in parallel. The output resistance is the $R_{DS(ON)}$ of the MOSFET transistor when the voltage on the driver output is less than the saturation voltage of the bipolar transistor.

ELECTRICAL CHARACTERISTICS (continued)

V_{DD} = 4.5 to 15 V, T_A = T_J (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
OVERALL							
I_{DD}	Static Operating Current	UCCx7323	INA = 0 V, INB = 0 V		300	450	µA
			INA = 0 V, INB = HIGH		300	450	
			INA = HIGH, INB = 0 V		300	450	
			INA = HIGH, INB = HIGH		300	450	
		UCCx7324	INA = 0 V, INB = 0 V		2	50	
			INA = 0 V, INB = HIGH		300	450	
			INA = HIGH, INB = 0 V		300	450	
			INA = HIGH, INB = HIGH		600	750	
		UCCx7325	INA = 0 V, INB = 0 V		150	300	
			INA = 0 V, INB = HIGH		450	600	
			INA = HIGH, INB = 0 V		150	300	
			INA = HIGH, INB = HIGH		450	600	

SWITCHING CHARACTERISTICS

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
T_R	Rise time (OUTA, OUTB)	C_{LOAD} = 1.8 nF, see Figure 1		20	40	ns
T_F	Fall time (OUTA, OUTB)	C_{LOAD} = 1.8 nF, see Figure 1		15	40	
T_{D1}	Delay, IN rising (IN to OUT)	C_{LOAD} = 1.8 nF, see Figure 1		25	40	
T_{D2}	Delay, IN falling (IN to OUT)	C_{LOAD} = 1.8 nF, see Figure 1		35	35	

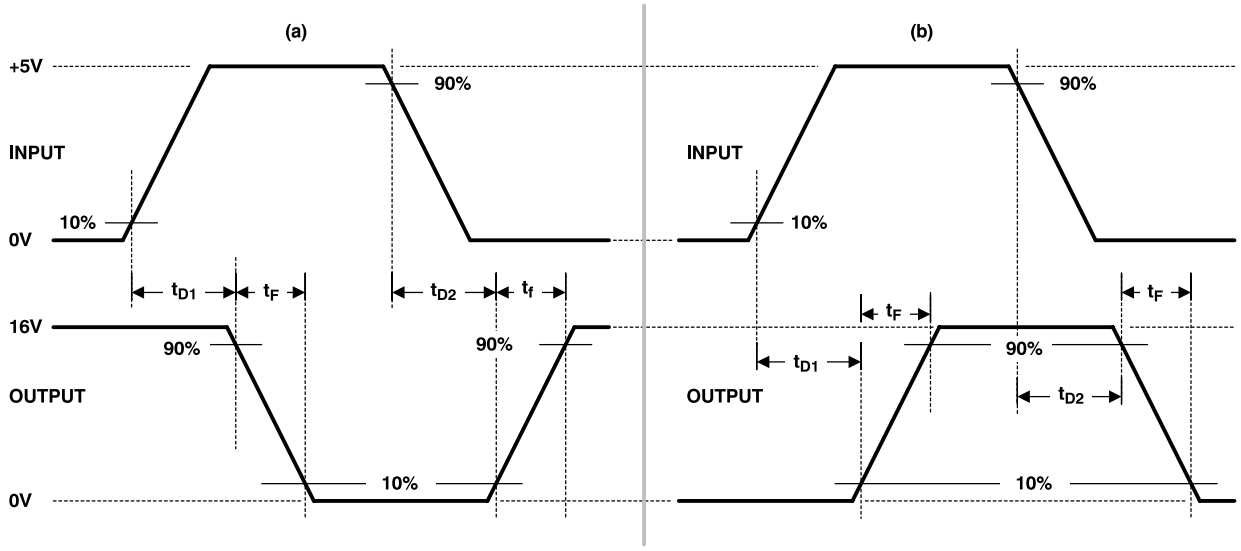


Figure 1. Switching Waveforms for (a) Inverting Driver and (b) Noninverting Driver

TERMINAL FUNCTIONS

TERMINAL			FUNCTION
NAME	NO.	I/O	
GND	3		**Common ground**: This ground should be connected very closely to the source of the power MOSFET which the driver is driving.
INA	2	I	**Input A**: Input signal of the A driver which has logic compatible threshold and hysteresis. If not used, this input must be tied to either VDD or GND; it must not be left floating.
INB	4	I	**Input B**: Input signal of the A driver which has logic compatible threshold and hysteresis. If not used, this input must be tied to either VDD or GND; it must not be left floating.
N/C	1		**No connection**: Must be grounded.
N/C	8		**No connection**: Must be grounded.
OUTA	7	O	**Driver output A**: The output stage is capable of providing 4-A drive current to the gate of a power MOSFET.
OUTB	5	O	**Driver output B**: The output stage is capable of providing 4-A drive current to the gate of a power MOSFET.
VDD	6	I	**Supply**: Supply voltage and the power input connection for this device.

APPLICATION INFORMATION

General Information

High-frequency power supplies often require high-speed, high-current drivers such as the UCC37323/4/5 family. A leading application is the needed to provide a high-power buffer stage between the PWM output of the control IC and the gates of the primary power MOSFET or IGBT switching devices. In other cases, the driver IC is used to drive the power-device gates through a drive transformer. Synchronous rectification supplies are also needed to simultaneously drive multiple devices which presents an extremely large load to the control circuitry.

Driver ICs are used when having the primary PWM regulator IC directly drive the switching devices for one or more reasons is not feasible. The PWMIC does not have the brute drive capability required for the intended switching MOSFET, limiting the switching performance in the application. In other cases there may be a desire to minimize the effect of high-frequency switching noise by placing the high current driver physically close to the load. Also, newer ICs that target the highest operating frequencies do not incorporate onboard gate drivers at all. Their PWM outputs are only intended to drive the high impedance input to a driver such as the UCC37323/4/5. Finally, the control IC is under thermal stress due to power dissipation, and an external driver helps by moving the heat from the controller to an external package.

Input Stage

The input thresholds have a 3.3-V logic sensitivity over the full range of V_{DD} voltage; yet it is equally compatible with 0 V to V_{DD} signals.

The inputs of UCC37323/4/5 family of drivers are designed to withstand 500-mA reverse current without either damage to the IC for logic upset. The input stage of each driver must be driven by a signal with a short rise or fall time. This condition is satisfied in typical power-supply applications, where the input signals are provided by a PWM controller or logic gates with fast transition times (<200 ns). The input stages to the drivers function as a digital gate, and are not intended for applications where a slow-changing input voltage is used to generate a switching output when the logic threshold of the input section is reached. While this may not be harmful to the driver, the output of the driver may switch repeatedly at a high frequency.

Users must not attempt to shape the input signals to the driver in an attempt to slow down (or delay) the signal at the output. If limiting the rise or fall times to the power device is desired, limit the rise or fall times to the power device, then add an external resistance between the output of the driver and the load device, which is generally a power MOSFET gate. The external resistor also helps remove power dissipation from the IC package, as discussed in the section on Thermal Considerations (see THERMAL INFORMATION).

Output Stage

Inverting outputs of the UCC37323 and OUTA of the UCC37325 are intended to drive external P-channel MOSFETs. Noninverting outputs of the UCC37324 and OUTB of the UCC37325 are intended to drive external N-channel MOSFETs.

Each output stage is capable of supplying ±4-A peak current pulses and swings to both VDD and GND. The pullup and pulldown circuits of the driver are constructed of bipolar and MOSFET transistors in parallel. The peak output current rating is the combined current from the bipolar and MOSFET transistors. The output resistance is the $R_{DS(on)}$ of the MOSFET transistor when the voltage on the driver output is less than the saturation voltage of the bipolar transistor. Each output stage also provides a very low impedance to overshoot and undershoot due to the body diode of the internal MOSFET. In many cases, external-schottky-clamp diodes are not required.

The UCC37323 family delivers 4-A of gate drive where it is most needed during the MOSFET switching transition — at the Miller plateau region — providing improved efficiency gains. A unique BiPolar and MOSFET hybrid output stage in parallel also allows efficient current sourcing at low supply voltages.

Source/Sink Capabilities During Miller Plateau

Large power MOSFETs present a large load to the control circuitry. Proper drive is required for efficient, reliable operation. The UCC37323/4/5 drivers have been optimized to provide maximum drive to a power MOSFET during the Miller plateau region of the switching transition. This interval occurs while the drain voltage is swinging between the voltage levels dictated by the power topology, requiring the charging and discharging of the drain-gate capacitance with current supplied or removed by the driver IC. (see References)

Two circuits are used to test the current capabilities of the UCC37323 driver. In each case, external circuitry is added to clamp the output near 5 V while the IC is sinking or sourcing current. An input pulse of 250 ns is applied at a frequency of 1 kHz in the proper polarity for the respective test. In each test there is a transient period where the current peaked up and then settled down to a steady-state value. The noted current measurements are made at a time of 200 ns after the input pulse is applied, after the initial transient.

The first circuit in Figure 2 is used to verify the current sink capability when the output of the driver is clamped around 5 V, a typical value of gate-source voltage during the Miller plateau region. The UCC37323 is found to sink 4.5 A at V_{DD} = 15 V and 4.28 A at V_{DD} = 12 V.

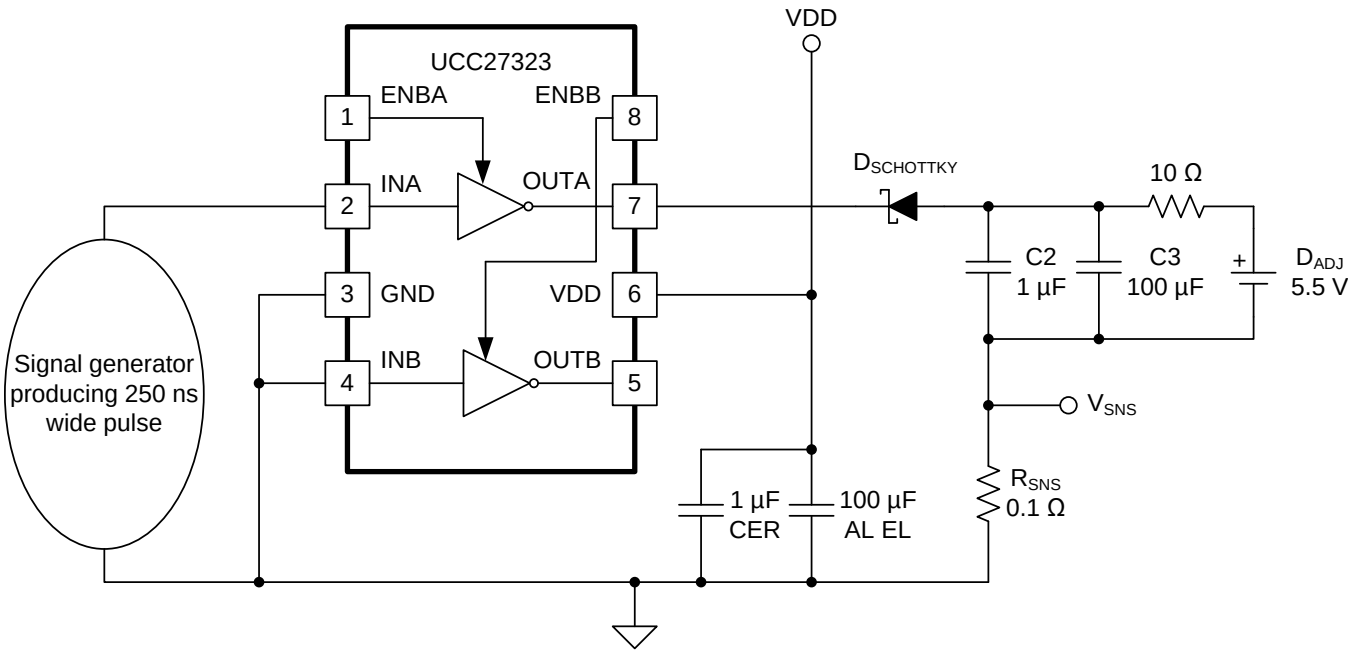


Figure 2.

The circuit shown in Figure 3 is used to test the current source capability with the output clamped to around 5 V with a string of Zener diodes. The UCC37323 is found to source 4.8 A at V_{DD} = 15 V and 3.7 A at V_{DD} = 12 V.

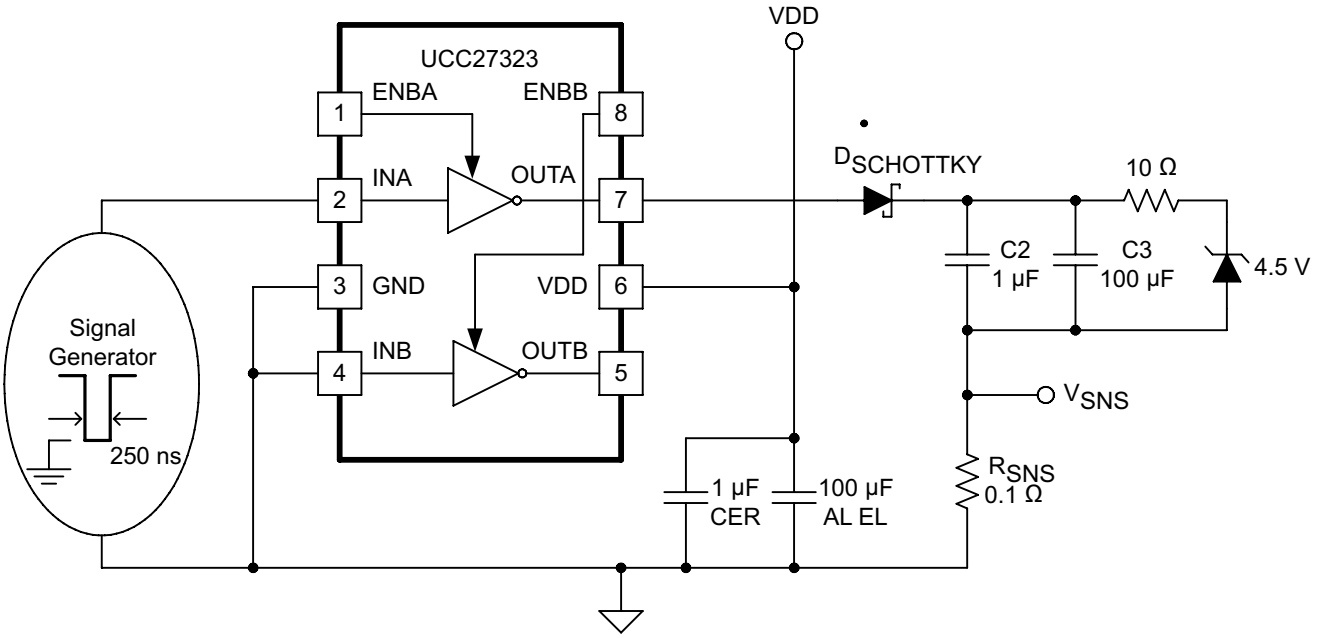


Figure 3.

Note that the current sink capability is slightly stronger than the current source capability at lower VDD. This stronger capability is due to the differences in the structure of the bipolar-MOSFET power output section, where the current source is a P-channel MOSFET and the current sink has an N-channel MOSFET.

In a large majority of applications it is advantageous that the turn-off capability of a driver is stronger than the turn-on capability. This helps to ensure that the MOSFET is held OFF during common power supply transients which may turn the device back ON.

Parallel Outputs

The A and B drivers combine into a single driver by connecting the INA and INB inputs together and the OUTA and OUTB outputs together. Then, a single signal controls the paralleled combination as shown in Figure 4.

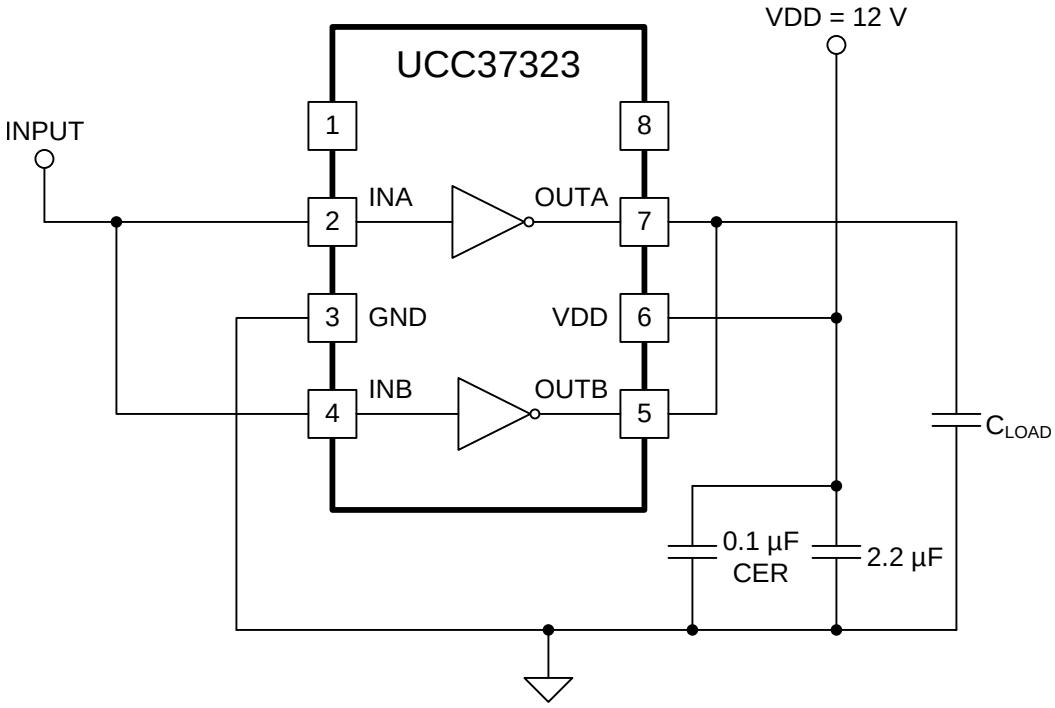


Figure 4.

Operational Waveforms and Circuit Layout

Figure 5 shows the circuit performance achievable with a single driver (half of the 8-pin IC) driving a 10-nF load. The input pulse width (not shown) is set to 300 ns to show both transitions in the output waveform. Note the linear rise and fall edges of the switching waveforms which is due to the constant output current characteristic of the driver as opposed to the resistive output impedance of traditional MOSFET-based gate drivers.

Sink and source currents of the driver are dependent upon the VDD value and the output capacitive load. The larger the VDD value, the higher the current capability; also, the larger the capacitive load, the higher the current sink and source capability.

Trace resistance and inductance, including wires and cables for testing, slows down the rise and fall times of the outputs; thus reducing the current capabilities of the driver.

To achieve higher current results, reduce resistance and inductance on the board as much as possible and increase the capacitive load value in order to swamp out the effect of inductance values.

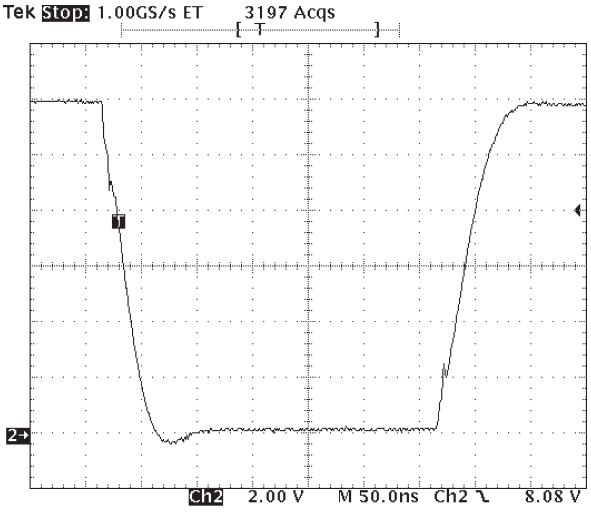


Figure 5.

In a power driver operating at high frequency, a significant challenge is to get clean waveforms without much overshoot or undershoot and ringing. The low output impedance of these drivers produces waveforms with high di/dt, which tends to induce ringing in the parasitic inductances. Utmost care must be used in the circuit layout. Connecting the driver IC as close as possible to the leads is advantageous. The driver IC layout has ground on the opposite side of the output, so the ground is connected to the bypass capacitors and the load with copper trace as wide as possible. These connections are also made with a small enclosed loop area to minimize the inductance.

VDD

Although quiescent VDD current is very low, total supply current will be higher, depending on OUTA and OUTB current and the programmed oscillator frequency. Total VDD current is the sum of quiescent VDD current and the average OUT current. Knowing the operating frequency and the MOSFET gate charge (Qg), average OUT current is calculated from Equation 1.

$$I_{OUT} = Qg \times f \quad (1)$$

where

- f is frequency

For the best high-speed circuit performance, two V_{DD} bypass capacitors are recommended tp prevent noise problems. The use of surface mount components is highly recommended. A 0.1-μF ceramic capacitor must be located closest to the VDD to ground connection. In addition, a larger capacitor (such as 1-μF) with relatively low ESR must be connected in parallel, to help deliver the high current peaks to the load. The parallel combination of capacitors must present a low impedance characteristic for the expected current levels in the driver application.

Drive Current and Power Requirements

The UCC37323/4/5 family of drivers are capable of delivering 4-A of current to a MOSFET gate for a period of several-hundred nanoseconds. High peak current is required to turn the device ON quickly. Then, to turn the device OFF, the driver is required to sink a similar amount of current to ground which repeats at the operating frequency of the power device. A MOSFET is used in this discussion because it is the most common type of switching device used in high frequency power conversion equipment.

References 1 and 2 discuss the current required to drive a power MOSFET and other capacitive-input switching devices. Reference 2 includes information on the previous generation of bipolar IC gate drivers (see References).

When a driver IC is tested with a discrete, capacitive load calculating the power that is required from the bias supply is fairly simple. The energy that must be transferred from the bias supply to charge the capacitor is given by Equation 2.

$$E = \tfrac{1}{2}CV^2 \quad (2)$$

where

- C is the load capacitor
- V is the bias voltage feeding the driver

There is an equal amount of energy transferred to ground when the capacitor is discharged. This leads to a power loss given by Equation 3.

$$P = 2 \times \tfrac{1}{2}CV^2f \quad (3)$$

where

- f is the switching frequency

This power is dissipated in the resistive elements of the circuit. Thus, with no external resistor between the driver and gate, this power is dissipated inside the driver. Half of the total power is dissipated when the capacitor is charged, and the other half is dissipated when the capacitor is discharged. An actual example using the conditions of the previous gate drive waveform helps to clarify this.

With V_{DD} = 12 V, C_{LOAD} = 10 nF, and f = 300 kHz, the power loss is calculated with Equation 4.

$$P = 10\ nF \times (12)^2 \times (300\ kHz) = 0.432\ W \quad (4)$$

With a 12-V supply, this equates to a current of (see Equation 5):

$$I = \frac{P}{V} = \frac{0.432\ W}{12\ V} = 0.036\ A \quad (5)$$

The actual current measured from the supply is 0.037 A, and is very close to the predicted value. But, the I_{DD} current that is due to the IC internal consumption must be considered. With no load the IC current draw is 0.0027 A. Under this condition the output rise and fall times are faster than with a load, which could lead to an almost insignificant, yet measurable current due to cross-conduction in the output stages of the driver. However, these small current differences are buried in the high frequency switching spikes, and are beyond the measurement capabilities of a basic lab setup. The measured current with 10-nF load is reasonably close to that expected.

The switching load presented by a power MOSFET converts to an equivalent capacitance by examining the gate charge required to switch the device. This gate charge includes the effects of the input capacitance plus the added charge needed to swing the drain of the device between the ON and OFF states. Most manufacturers provide specifications that provide the typical and maximum gate charge, in nC, to switch the device under specified conditions. Using the gate charge Qg, determine the power that must be dissipated when charging a capacitor which is done by using the equivalence Qg = CeffV to provide Equation 6 for power:

$$P = C \times V^2 \times f = Qg \times f \quad (6)$$

Equation 6 allows a power designer to calculate the bias power required to drive a specific MOSFET gate at a specific bias voltage.

THERMAL INFORMATION

The useful range of a driver is greatly affected by the drive power requirements of the load and the thermal characteristics of the IC package. In order for a power driver to be useful over a particular temperature range, the package must allow for the efficient removal of the heat produced while keeping the junction temperature within rated limits. The UCC37323/4/5 family of drivers is available in three different packages to cover a range of application requirements.

As shown in the POWER DISSIPATION RATINGS table, the SOIC-8 (D) and PDIP-8 (P) packages each have a power rating of around 0.5 W with T_A = 70°C. This limit is imposed in conjunction with the power derating factor also given in the table. Note that the power dissipation in our earlier example is 0.432 W with a 10-nF load, 12 VDD, switched at 300 kHz. Thus, only one load of this size can be driven using the D or P package, even if the two onboard drivers are paralleled. The difficulties with heat removal limit the drive available in the older packages.

The MSOP PowerPAD-8 (DGN) package significantly relieves this concern by offering an effective means of removing the heat from the semiconductor junction. As illustrated in Reference 3 (see References), the PowerPAD packages offer a lead-frame die pad that is exposed at the base of the package. This pad is soldered to the copper on the PC board directly underneath the IC package, reducing the θ_{JC} down to 4.7°C/W. Data is presented in Reference 3 to show that the power dissipation can be quadrupled in the PowerPAD configuration when compared to the standard packages. The PC board must be designed with thermal lands and thermal vias to complete the heat removal subsystem, as summarized in Reference 4. This design allows a significant improvement in heat sinking over that which is available in the D or P packages, and is shown to more than double the power capability of the D and P packages.

NOTE

The PowerPAD is not directly connected to any leads of the package. However, the PowerPad is electrically and thermally connected to the substrate which is the ground of the device.

References

1. Power Supply Seminar SEM-1400 Topic 2, *Design And Application Guide For High Speed MOSFET Gate Drive Circuits*, by Laszlo Balogh, TI Literature Number SLUP133
2. Application Note, *Practical Considerations in High Performance MOSFET, IGBT and MCT Gate Drive Circuits*, by Bill Andreycak, TI Literature Number SLUA105
3. Technical Brief, *PowerPad Thermally Enhanced Package*, TI Literature Number SLMA002
4. Application Brief, *PowerPAD Made Easy*, TI Literature Number SLMA004

REVISION HISTORY

Changes from Revision G (March 2010) to Revision H **Page**

- Changed $D_{SCHOTTKY}$ diode direction and voltage of zener diode from 5.5 to 4.5 V in Figure 3 8
- Added three paragraphs after first paragraph of *Operational Waveforms and Circuit Layout* section before Figure 5 10

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
UCC27323D	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	27323	Samples
UCC27323DG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	27323	Samples
UCC27323DGN	ACTIVE	MSOP-PowerPAD	DGN	8	80	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	27323	Samples
UCC27323DGNG4	ACTIVE	MSOP-PowerPAD	DGN	8	80	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	27323	Samples
UCC27323DGNR	ACTIVE	MSOP-PowerPAD	DGN	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	27323	Samples
UCC27323DGNRG4	ACTIVE	MSOP-PowerPAD	DGN	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	27323	Samples
UCC27323DR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	27323	Samples
UCC27323DRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	27323	Samples
UCC27323P	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-40 to 125	UCC27323P	Samples
UCC27323PE4	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-40 to 125	UCC27323P	Samples
UCC27324D	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	27324	Samples
UCC27324DG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	27324	Samples
UCC27324DGN	ACTIVE	MSOP-PowerPAD	DGN	8	80	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	27324	Samples
UCC27324DGNG4	ACTIVE	MSOP-PowerPAD	DGN	8	80	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	27324	Samples
UCC27324DGNR	ACTIVE	MSOP-PowerPAD	DGN	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	27324	Samples
UCC27324DGNRG4	ACTIVE	MSOP-PowerPAD	DGN	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	27324	Samples
UCC27324DR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	27324	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
UCC27324DRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	27324	Samples
UCC27324P	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-40 to 125	UCC27324P	Samples
UCC27324PE4	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-40 to 125	UCC27324P	Samples
UCC27325D	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	27325	Samples
UCC27325DG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	27325	Samples
UCC27325DGN	ACTIVE	MSOP-PowerPAD	DGN	8	80	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	27325	Samples
UCC27325DGNG4	ACTIVE	MSOP-PowerPAD	DGN	8	80	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	27325	Samples
UCC27325DGNR	ACTIVE	MSOP-PowerPAD	DGN	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	27325	Samples
UCC27325DR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	27325	Samples
UCC27325P	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-40 to 125	UCC27325P	Samples
UCC27325PE4	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-40 to 125	UCC27325P	Samples
UCC37323D	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	37323	Samples
UCC37323DG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	37323	Samples
UCC37323DGN	ACTIVE	MSOP-PowerPAD	DGN	8	80	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-1-260C-UNLIM	0 to 70	37323	Samples
UCC37323DGNG4	ACTIVE	MSOP-PowerPAD	DGN	8	80	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-1-260C-UNLIM	0 to 70	37323	Samples
UCC37323DGNR	ACTIVE	MSOP-PowerPAD	DGN	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-1-260C-UNLIM	0 to 70	37323	Samples
UCC37323DGNRG4	ACTIVE	MSOP-PowerPAD	DGN	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-1-260C-UNLIM	0 to 70	37323	Samples
UCC37323DR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	37323	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
UCC37323DRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	37323	Samples
UCC37323P	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	UCC37323P	Samples
UCC37323PE4	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	UCC37323P	Samples
UCC37324D	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	37324	Samples
UCC37324DG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	37324	Samples
UCC37324DGN	ACTIVE	MSOP-PowerPAD	DGN	8	80	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-1-260C-UNLIM	0 to 70	37324	Samples
UCC37324DGNR	ACTIVE	MSOP-PowerPAD	DGN	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-1-260C-UNLIM	0 to 70	37324	Samples
UCC37324DR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	37324	Samples
UCC37324DRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	37324	Samples
UCC37324P	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	UCC37324P	Samples
UCC37324PE4	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	UCC37324P	Samples
UCC37325D	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	37325	Samples
UCC37325DG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	37325	Samples
UCC37325DGN	ACTIVE	MSOP-PowerPAD	DGN	8	80	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-1-260C-UNLIM	0 to 70	37325	Samples
UCC37325DGNR	ACTIVE	MSOP-PowerPAD	DGN	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-1-260C-UNLIM	0 to 70	37325	Samples
UCC37325DGNRG4	ACTIVE	MSOP-PowerPAD	DGN	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-1-260C-UNLIM	0 to 70	37325	Samples
UCC37325DR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	37325	Samples
UCC37325P	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	UCC37325P	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
UCC37325PE4	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	UCC37325P	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

OTHER QUALIFIED VERSIONS OF UCC27324 :

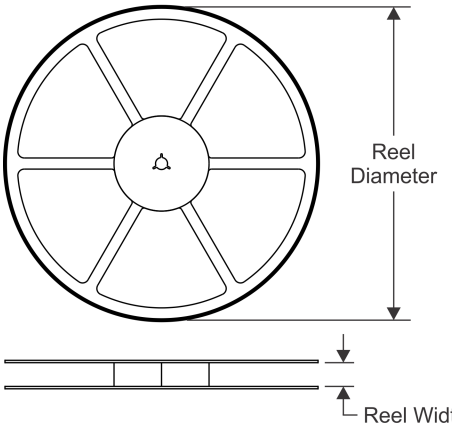
- Automotive: UCC27324-Q1

NOTE: Qualified Version Definitions:

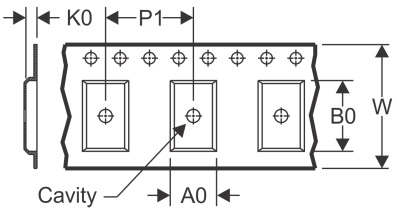
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

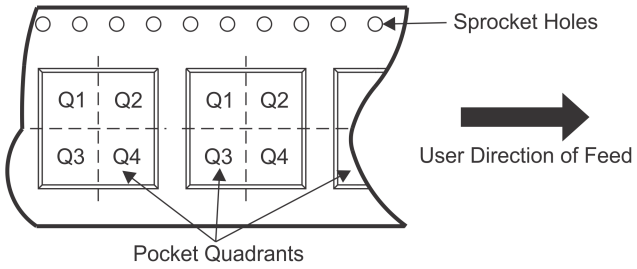


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

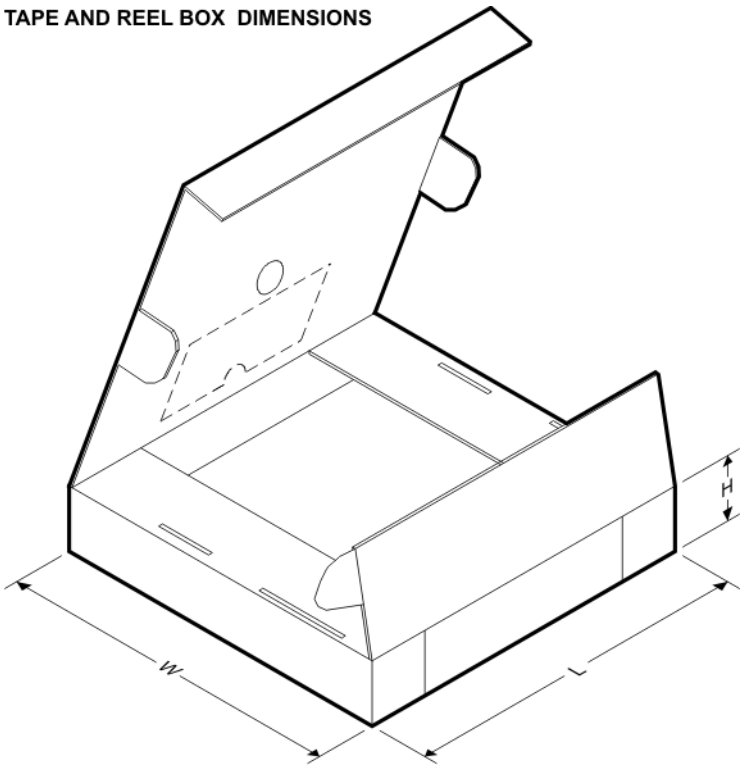


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
UCC27323DGNR	MSOP-Power PAD	DGN	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
UCC27323DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
UCC27324DGNR	MSOP-Power PAD	DGN	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
UCC27324DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
UCC27325DGNR	MSOP-Power PAD	DGN	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
UCC27325DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
UCC37323DGNR	MSOP-Power PAD	DGN	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
UCC37323DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
UCC37324DGNR	MSOP-Power PAD	DGN	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
UCC37324DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
UCC37325DGNR	MSOP-	DGN	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
	Power PAD											
UCC37325DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

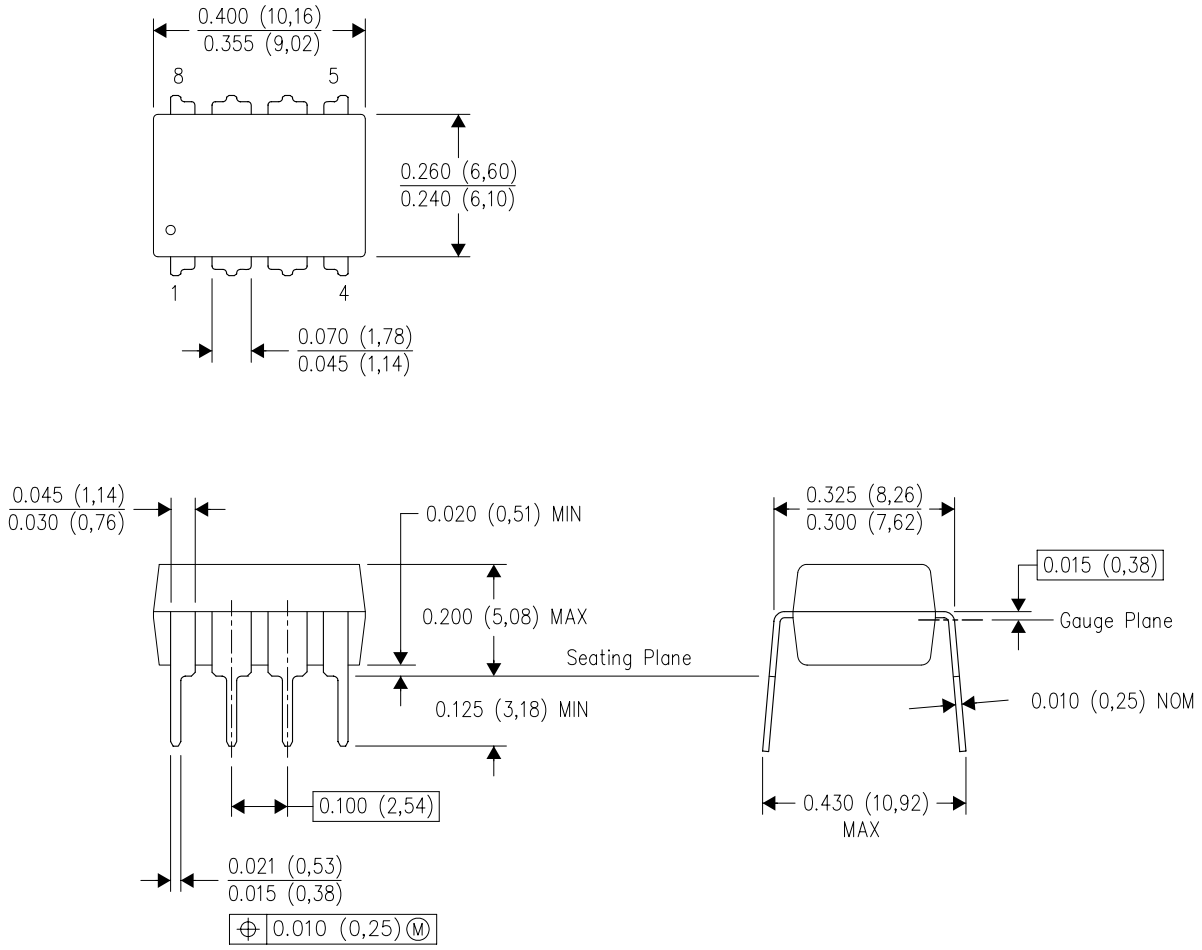
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

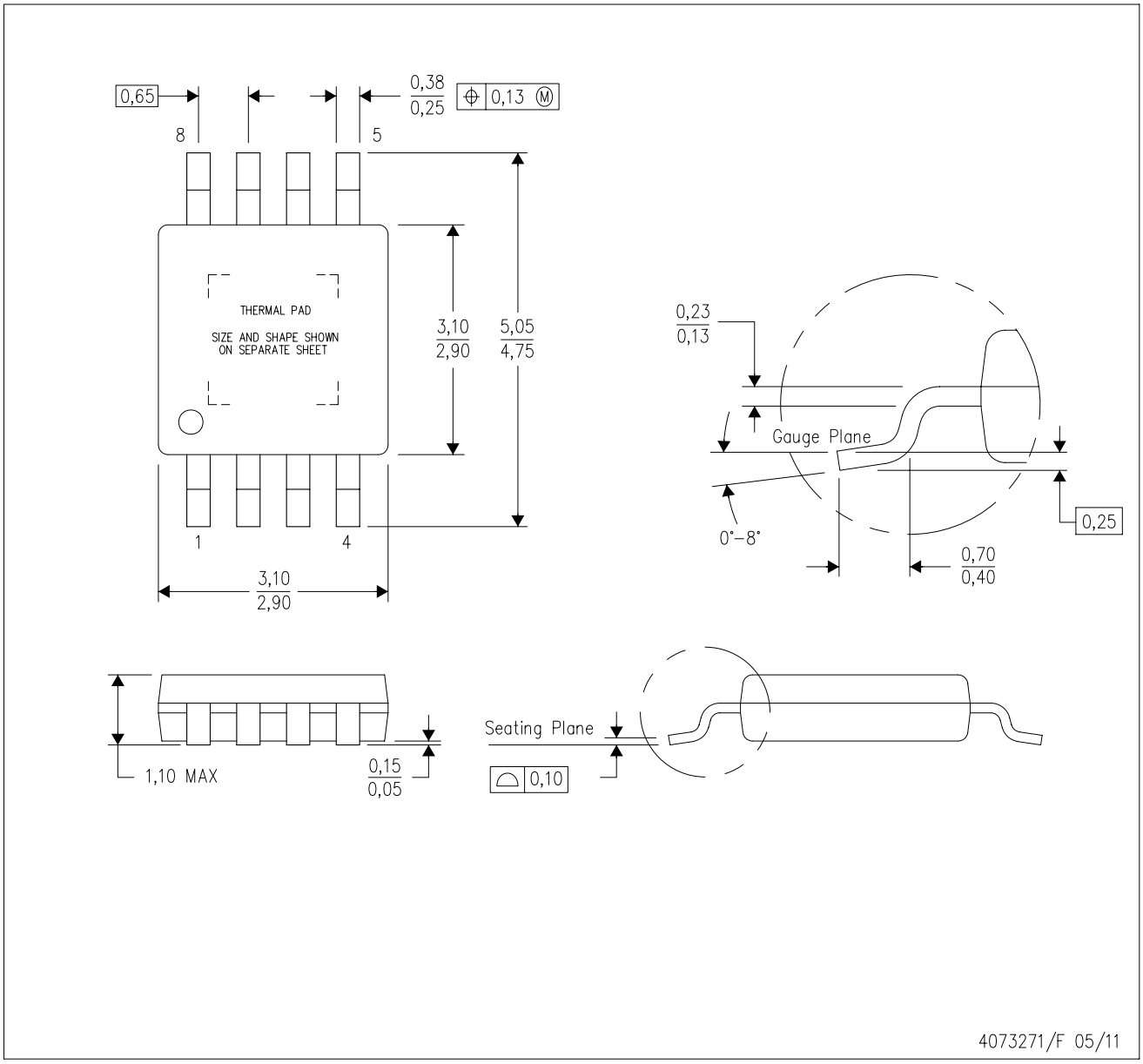
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
UCC27323DGNR	MSOP-PowerPAD	DGN	8	2500	364.0	364.0	27.0
UCC27323DR	SOIC	D	8	2500	340.5	338.1	20.6
UCC27324DGNR	MSOP-PowerPAD	DGN	8	2500	364.0	364.0	27.0
UCC27324DR	SOIC	D	8	2500	340.5	338.1	20.6
UCC27325DGNR	MSOP-PowerPAD	DGN	8	2500	364.0	364.0	27.0
UCC27325DR	SOIC	D	8	2500	340.5	338.1	20.6
UCC37323DGNR	MSOP-PowerPAD	DGN	8	2500	364.0	364.0	27.0
UCC37323DR	SOIC	D	8	2500	340.5	338.1	20.6
UCC37324DGNR	MSOP-PowerPAD	DGN	8	2500	364.0	364.0	27.0
UCC37324DR	SOIC	D	8	2500	340.5	338.1	20.6
UCC37325DGNR	MSOP-PowerPAD	DGN	8	2500	364.0	364.0	27.0
UCC37325DR	SOIC	D	8	2500	340.5	338.1	20.6

P (R–PDIP–T8) PLASTIC DUAL–IN–LINE PACKAGE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001 variation BA.

DGN (S–PDSO–G8) PowerPAD™ PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http://www.ti.com>.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Falls within JEDEC MO–187 variation AA–T

PowerPAD is a trademark of Texas Instruments.

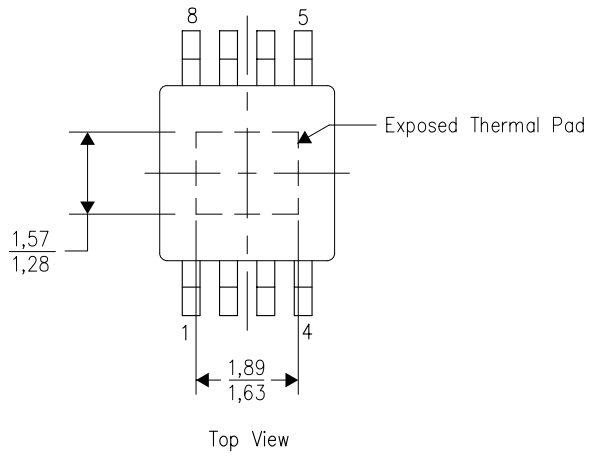
DGN (S–PDSO–G8) PowerPAD™ PLASTIC SMALL OUTLINE

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Top View

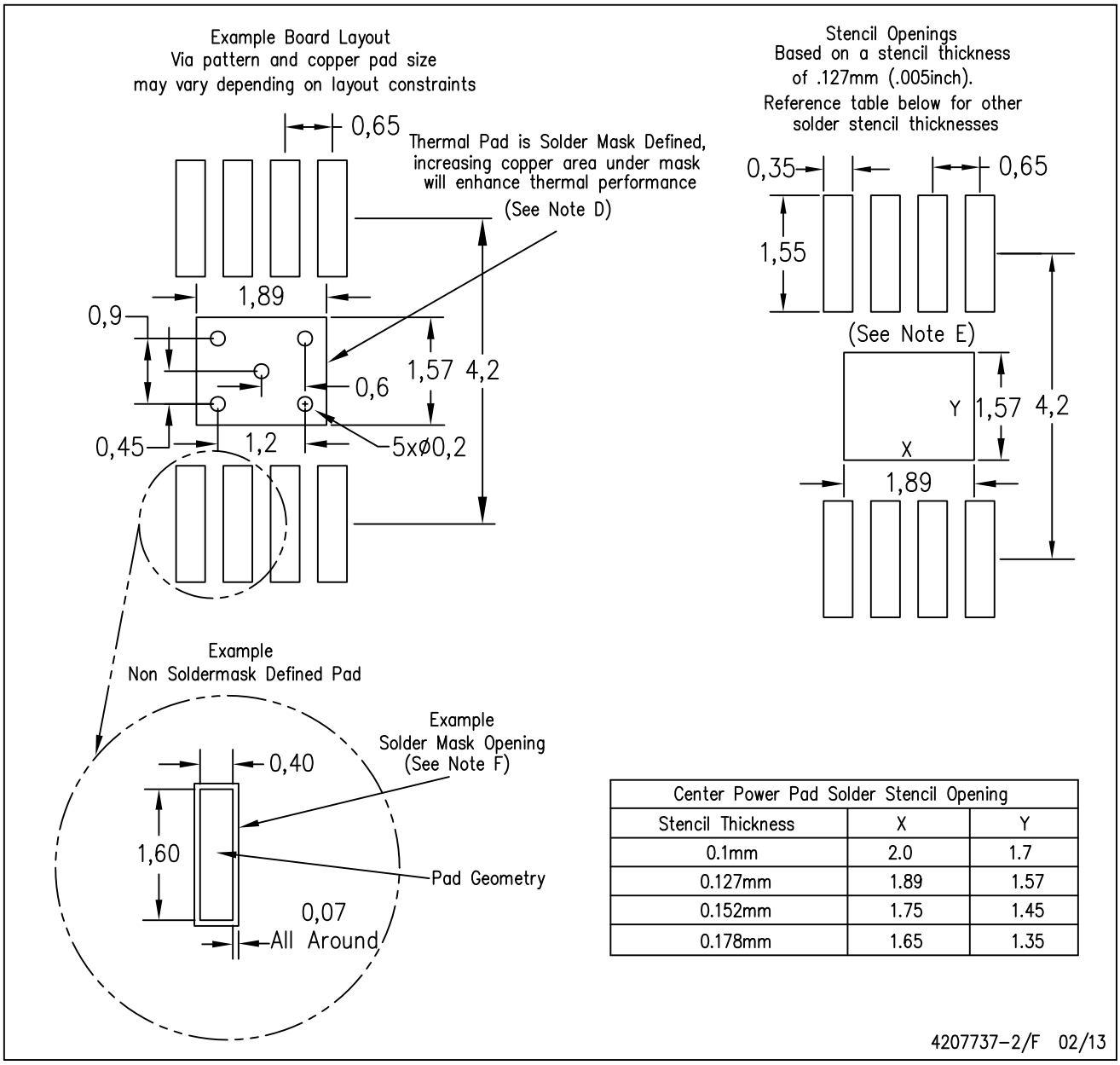
Exposed Thermal Pad Dimensions

4206323–2/I 12/11

NOTE: All linear dimensions are in millimeters

PowerPAD is a trademark of Texas Instruments

DGN (R–PDSO–G8) PowerPAD™ PLASTIC SMALL OUTLINE

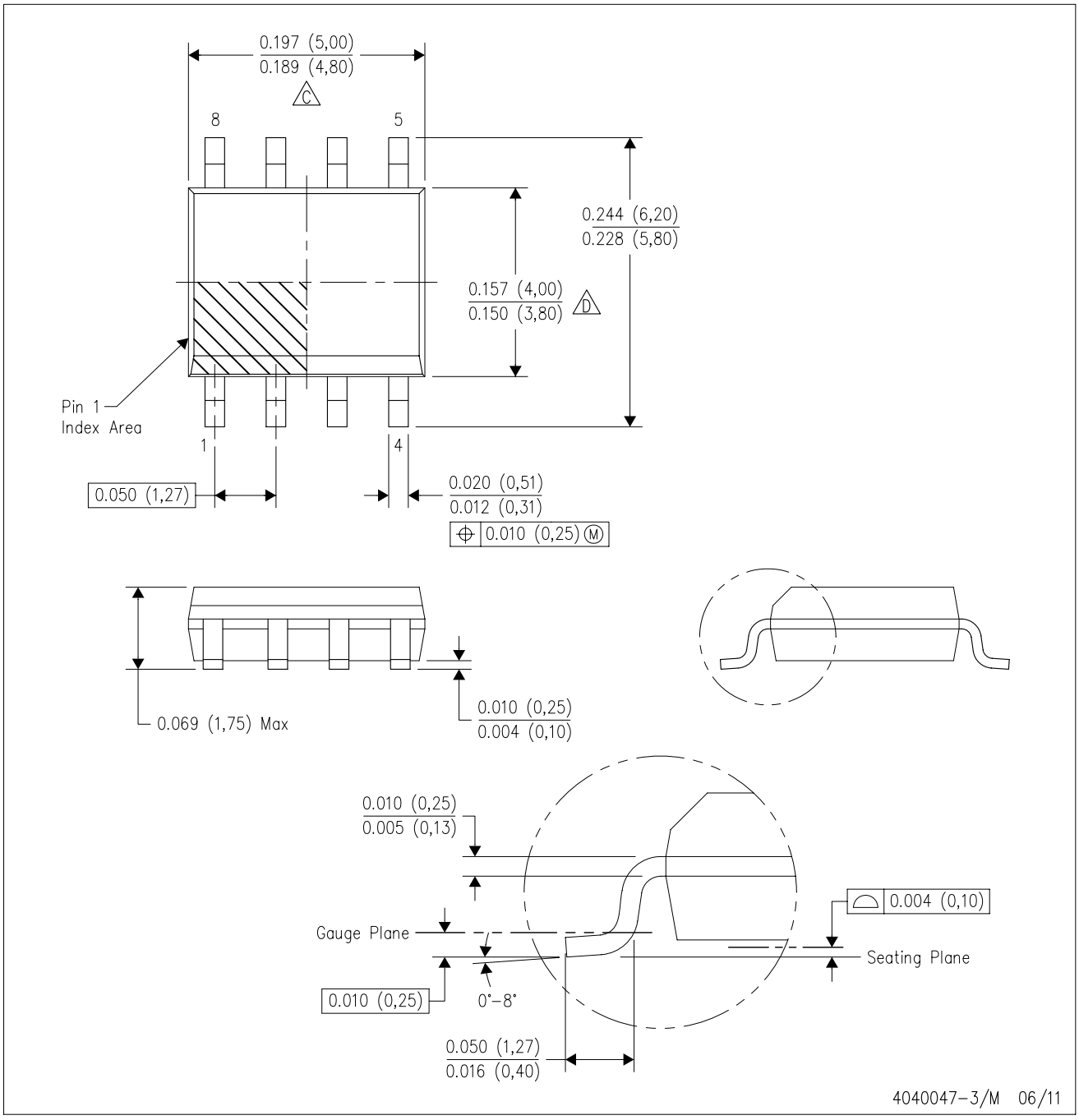


Center Power Pad Solder Stencil Opening		
Stencil Thickness	X	Y
0.1mm	2.0	1.7
0.127mm	1.89	1.57
0.152mm	1.75	1.45
0.178mm	1.65	1.35

4207737–2/F 02/13

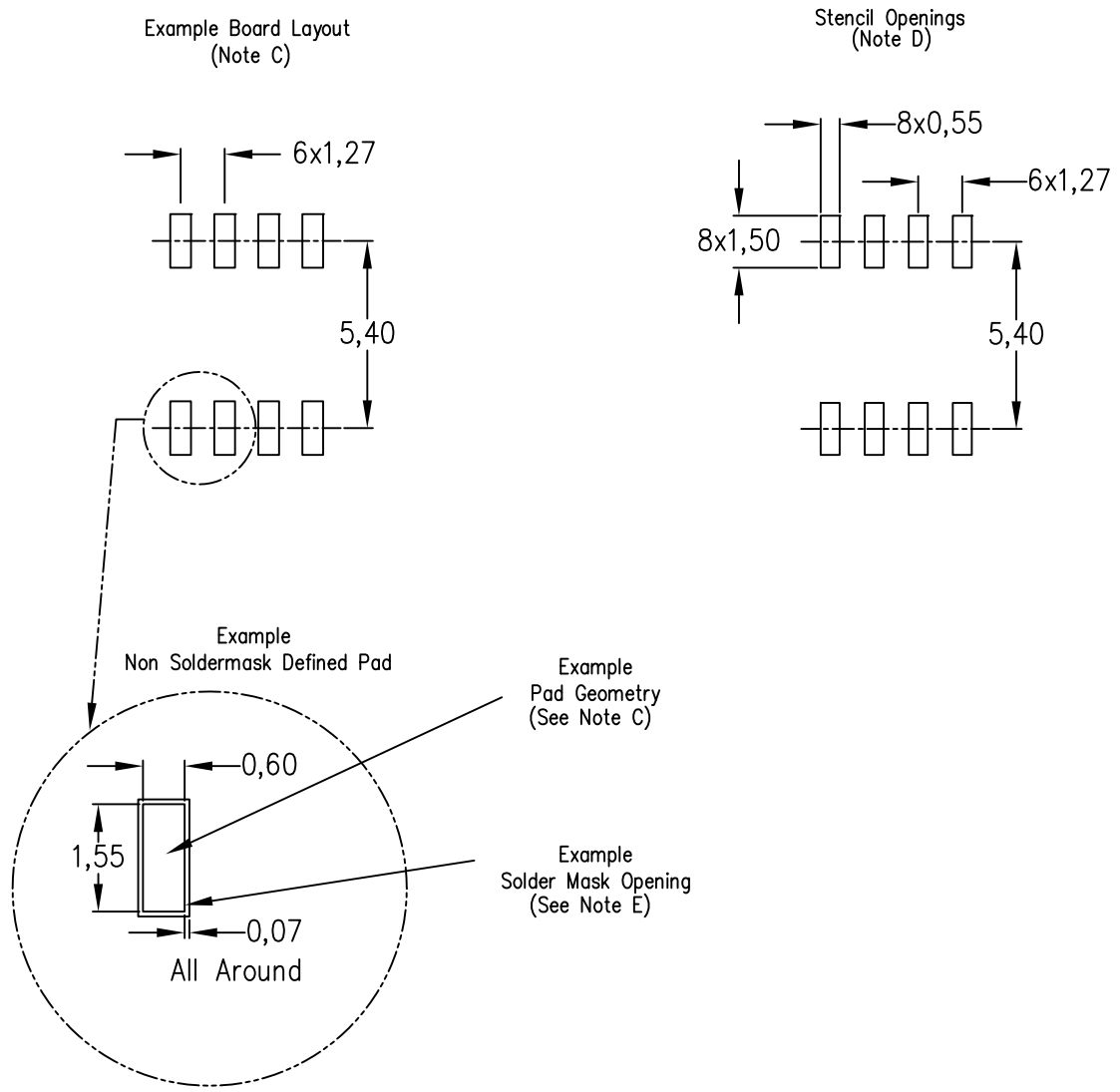
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.
F. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

D (R–PDSO–G8) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AA.

D (R–PDSO–G8) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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Only those TI components which TI has specifically designated as military grade or “enhanced plastic” are designed and intended for use in military/aerospace applications or environments. Buyer acknowledges and agrees that any military or aerospace use of TI components which have ***not*** been so designated is solely at the Buyer's risk, and that Buyer is solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI has specifically designated certain components as meeting ISO/TS16949 requirements, mainly for automotive use. In any case of use of non-designated products, TI will not be responsible for any failure to meet ISO/TS16949.

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