

# TLVx314

## 3-MHz, Low-Power, Internal EMI Filter, RRIO, Operational Amplifier

### 1 Features

- Low Offset Voltage: 0.75 mV (typ)
- Low Input Bias Current: 1 pA (typ)
- Wide Supply Range: 1.8 V to 5.5 V
- Rail-to-Rail Input and Output
- Gain Bandwidth: 3 MHz
- Low  $I_Q$ : 250  $\mu$ A/Ch (max)
- Low Noise: 16 nV/ $\sqrt{\text{Hz}}$  at 1 kHz
- Internal RF/EMI Filter
- Extended Temperature Range:  $-40^\circ\text{C}$  to  $+125^\circ\text{C}$

### 2 Applications

- White Goods
- Handheld Test Equipment
- Portable Blood Glucose Systems
- Remote Sensing
- Active Filters
- Industrial Automation
- Battery-Powered Electronics

### 3 Description

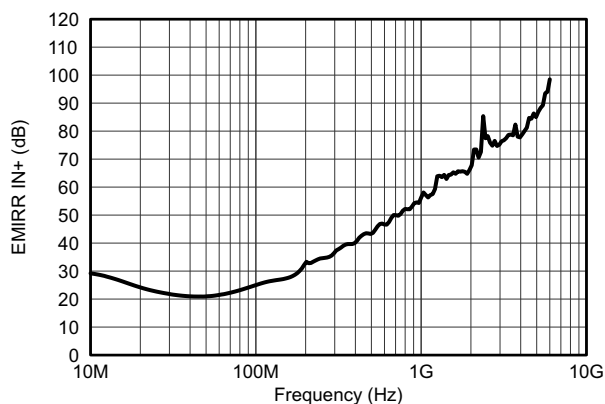
The TLV314 family of single-, dual-, and quad-channel operational amplifiers represents a new generation of low-power, general-purpose operational amplifiers. Rail-to-rail input and output swings (RRIO), low quiescent current (150  $\mu$ A typically at 5 V) combine with a wide bandwidth of 3 MHz to make this family very attractive for a variety of battery-powered applications that require a good balance between cost and performance. Additionally, the TLV314 family architecture achieves a low input bias current of 1 pA, allowing for applications with M $\Omega$  source impedances.

The robust design of the TLV314 devices provides ease-of-use to the circuit designer: unity-gain stability, RRIO, capacitive loads of up to 300 pF, an integrated RF/EMI rejection filter, no phase reversal in overdrive conditions, and high electrostatic discharge (ESD) protection (4-kV HBM).

These devices are optimized for low-voltage operation as low as 1.8 V ( $\pm 0.9$  V) and up to 5.5 V ( $\pm 2.75$  V), and are specified over the extended industrial temperature range of  $-40^\circ\text{C}$  to  $+125^\circ\text{C}$ .

The TLV314 (single) is available in both 5-pin SC70 and SOT-23 packages. The TLV2314 (dual) is offered in 8-pin SOIC and VSSOP packages. The quad-channel TLV4314 is offered in a 14-pin TSSOP package.

EMIRR vs Frequency



Device Information<sup>(1)</sup>

| PART NUMBER | PACKAGE    | BODY SIZE (NOM)   |
|-------------|------------|-------------------|
| TLV314      | SOT-23 (5) | 2.90 mm x 1.60 mm |
|             | SC70 (5)   | 2.00 mm x 1.25 mm |
| TLV2314     | VSSOP (8)  | 3.00 mm x 3.00 mm |
|             | SOIC (8)   | 4.90 mm x 3.91 mm |
| TLV4314     | TSSOP (14) | 5.00 mm x 4.40 mm |

(1) For all available packages, see the orderable addendum at the end of the data sheet.



## Table of Contents

|  |           |  |           |
|--|-----------|--|-----------|
| <b>1 Features</b> .....                        | <b>1</b>  | 8.4 Device Functional Modes.....                 | <b>15</b> |
| <b>2 Applications</b> .....                    | <b>1</b>  | <b>9 Application and Implementation</b> .....    | <b>16</b> |
| <b>3 Description</b> .....                     | <b>1</b>  | 9.1 Application Information.....                 | <b>16</b> |
| <b>4 Revision History</b> .....                | <b>2</b>  | 9.2 Typical Application .....                    | <b>16</b> |
| <b>5 Device Comparison Table</b> .....         | <b>3</b>  | 9.3 System Examples .....                        | <b>17</b> |
| <b>6 Pin Configuration and Functions</b> ..... | <b>3</b>  | <b>10 Power Supply Recommendations</b> .....     | <b>18</b> |
| <b>7 Specifications</b> .....                  | <b>6</b>  | 10.1 Input and ESD Protection .....              | <b>18</b> |
| 7.1 Absolute Maximum Ratings .....             | <b>6</b>  | <b>11 Layout</b> .....                           | <b>19</b> |
| 7.2 ESD Ratings.....                           | <b>6</b>  | 11.1 Layout Guidelines .....                     | <b>19</b> |
| 7.3 Recommended Operating Conditions.....      | <b>6</b>  | 11.2 Layout Example .....                        | <b>19</b> |
| 7.4 Thermal Information: TLV314 .....          | <b>7</b>  | <b>12 Device and Documentation Support</b> ..... | <b>20</b> |
| 7.5 Thermal Information: TLV2314 .....         | <b>7</b>  | 12.1 Device Support.....                         | <b>20</b> |
| 7.6 Thermal Information: TLV4314 .....         | <b>7</b>  | 12.2 Documentation Support .....                 | <b>20</b> |
| 7.7 Electrical Characteristics.....            | <b>8</b>  | 12.3 Related Links .....                         | <b>20</b> |
| 7.8 Typical Characteristics.....               | <b>9</b>  | 12.4 Community Resources.....                    | <b>20</b> |
| 7.9 Typical Characteristics.....               | <b>10</b> | 12.5 Trademarks .....                            | <b>20</b> |
| <b>8 Detailed Description</b> .....            | <b>13</b> | 12.6 Electrostatic Discharge Caution.....        | <b>20</b> |
| 8.1 Overview .....                             | <b>13</b> | 12.7 Glossary .....                              | <b>20</b> |
| 8.2 Functional Block Diagram .....             | <b>13</b> | <b>13 Mechanical, Packaging, and Orderable</b>   | <b>20</b> |
| 8.3 Feature Description.....                   | <b>14</b> | <b>Information</b> .....                         | <b>20</b> |

## 4 Revision History

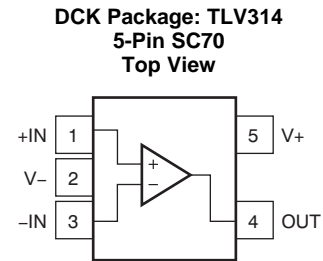
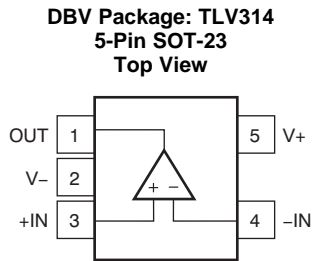
NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

| <b>Changes from Original (March 2016) to Revision A</b> | <b>Page</b> |
|---|-------------|
| • Released to production .....                          | <b>1</b>    |

## 5 Device Comparison Table

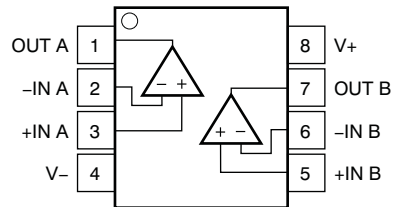
| DEVICE  | NO. OF CHANNELS | PACKAGE-LEADS |      |      |       |       |
|---------|-----------------|---------------|------|------|-------|-------|
|         |                 | SOT-23        | SC70 | SOIC | VSSOP | TSSOP |
| TLV314  | 1               | 5             | 5    | —    | —     | —     |
| TLV2314 | 2               | —             | —    | 8    | 8     | —     |
| TLV4314 | 4               | —             | —    | —    | —     | 14    |

## 6 Pin Configuration and Functions



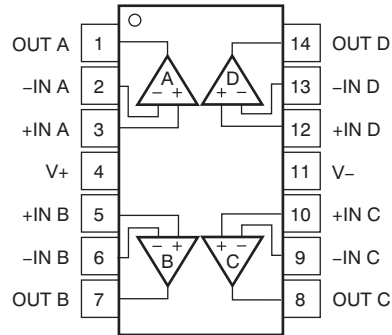
### Pin Functions: TLV314

| NAME | PIN |     | I/O | DESCRIPTION               |
|------|-----|-----|-----|---------------------------|
|      | NO. |     |     |                           |
|      | DBV | DCK |     |                           |
| -IN  | 4   | 3   | I   | Inverting input           |
| +IN  | 3   | 1   | I   | Noninverting input        |
| OUT  | 1   | 4   | O   | Output                    |
| V-   | 2   | 2   | —   | Negative (lowest) supply  |
| V+   | 5   | 5   | —   | Positive (highest) supply |

**D, DGK Package: TLV2314  
8-Pin SOIC or VSSOP  
Top View**

**Pin Functions: TLV2314**

| PIN   |     | I/O | DESCRIPTION                   |
|-------|-----|-----|-------------------------------|
| NAME  | NO. |     |                               |
| -IN A | 2   | I   | Inverting input, channel A    |
| +IN A | 3   | I   | Noninverting input, channel A |
| -IN B | 6   | I   | Inverting input, channel B    |
| +IN B | 5   | I   | Noninverting input, channel B |
| OUT A | 1   | O   | Output, channel A             |
| OUT B | 7   | O   | Output, channel B             |
| V-    | 4   | —   | Negative (lowest) supply      |
| V+    | 8   | —   | Positive (highest) supply     |

**PW Package: TLV4314  
14-Pin TSSOP  
Top View**



**Pin Functions: TLV4314**

| PIN   |     | I/O | DESCRIPTION                   |
|-------|-----|-----|-------------------------------|
| NAME  | NO. |     |                               |
| -IN A | 2   | I   | Inverting input, channel A    |
| +IN A | 3   | I   | Noninverting input, channel A |
| -IN B | 6   | I   | Inverting input, channel B    |
| +IN B | 5   | I   | Noninverting input, channel B |
| -IN C | 9   | I   | Inverting input, channel C    |
| +IN C | 10  | I   | Noninverting input, channel C |
| -IN D | 13  | I   | Inverting input, channel D    |
| +IN D | 12  | I   | Noninverting input, channel D |
| OUT A | 1   | O   | Output, channel A             |
| OUT B | 7   | O   | Output, channel B             |
| OUT C | 8   | O   | Output, channel C             |
| OUT D | 14  | O   | Output, channel D             |
| V-    | 11  | —   | Negative (lowest) supply      |
| V+    | 4   | —   | Positive (highest) supply     |

## 7 Specifications

### 7.1 Absolute Maximum Ratings

 over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

|                                     |                           | MIN                     | MAX                     | UNIT |
|-------------------------------------|---------------------------|-------------------------|-------------------------|------|
| Supply voltage                      |                           | 7                       |                         | V    |
| Signal input pins                   | Voltage <sup>(2)</sup>    | (V <sub>-</sub> ) – 0.5 | (V <sub>+</sub> ) + 0.5 | V    |
|                                     | Current <sup>(2)</sup>    | –10                     | 10                      | mA   |
| Output short-circuit <sup>(3)</sup> |                           | Continuous              |                         | mA   |
| Temperature                         | Specified, T <sub>A</sub> | –40                     | 125                     | °C   |
|                                     | Junction, T <sub>J</sub>  |                         | 150                     |      |
|                                     | Storage, T <sub>stg</sub> | –65                     | 150                     |      |

- (1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not supported.
- (2) Input pins are diode-clamped to the power-supply rails. Input signals that can swing more than 0.5 V beyond the supply rails must be current limited to 10 mA or less.
- (3) Short-circuit to ground, one amplifier per package.

### 7.2 ESD Ratings

|                    |                         | VALUE  | UNIT  |
|--------------------|-------------------------|--|-------|
| V <sub>(ESD)</sub> | Electrostatic discharge | Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 <sup>(1)</sup>              | ±4000 |
|                    |                         | Charged-device model (CDM), per JEDEC specification JESD22-C101 <sup>(2)</sup> | ±1000 |

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

### 7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

|                             |                | MIN           | NOM  | MAX   | UNIT |
|-----------------------------|----------------|---------------|------|-------|------|
| V <sub>S</sub>              | Supply voltage | Single supply | 1.8  | 5.5   | V    |
|                             |                | Dual supply   | ±0.9 | ±2.75 |      |
| Specified temperature range |                | –40           |      | 125   | °C   |

## 7.4 Thermal Information: TLV314

| THERMAL METRIC <sup>(1)</sup> |  | TLV314       |            | UNIT |
|-------------------------------|--|--------------|------------|------|
|                               |  | DBV (SOT-23) | DCK (SC70) |      |
|                               |  | 5 PINS       | 5 PINS     |      |
| R <sub>θJA</sub>              | Junction-to-ambient thermal resistance       | 228.5        | 281.4      | °C/W |
| R <sub>θJC(top)</sub>         | Junction-to-case(top) thermal resistance     | 99.1         | 91.6       | °C/W |
| R <sub>θJB</sub>              | Junction-to-board thermal resistance         | 54.6         | 59.6       | °C/W |
| Ψ <sub>JT</sub>               | Junction-to-top characterization parameter   | 7.7          | 1.5        | °C/W |
| Ψ <sub>JB</sub>               | Junction-to-board characterization parameter | 53.8         | 58.8       | °C/W |

- (1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, [SPRA953](#).

## 7.5 Thermal Information: TLV2314

| THERMAL METRIC <sup>(1)</sup> |  | TLV2314  |             | UNIT |
|-------------------------------|--|----------|-------------|------|
|                               |  | D (SOIC) | DGK (VSSOP) |      |
|                               |  | 8 PINS   | 8 PINS      |      |
| R <sub>θJA</sub>              | Junction-to-ambient thermal resistance       | 138.4    | 191.2       | °C/W |
| R <sub>θJC(top)</sub>         | Junction-to-case(top) thermal resistance     | 89.5     | 61.9        | °C/W |
| R <sub>θJB</sub>              | Junction-to-board thermal resistance         | 78.6     | 111.9       | °C/W |
| Ψ <sub>JT</sub>               | Junction-to-top characterization parameter   | 29.9     | 5.1         | °C/W |
| Ψ <sub>JB</sub>               | Junction-to-board characterization parameter | 78.1     | 110.2       | °C/W |

- (1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, [SPRA953](#).

## 7.6 Thermal Information: TLV4314

| THERMAL METRIC <sup>(1)</sup> |  | TLV4314  |            | UNIT |
|-------------------------------|--|----------|------------|------|
|                               |  | D (SOIC) | PW (TSSOP) |      |
|                               |  | 14 PINS  | 14 PINS    |      |
| R <sub>θJA</sub>              | Junction-to-ambient thermal resistance       | 93.2     | 121        | °C/W |
| R <sub>θJC(top)</sub>         | Junction-to-case(top) thermal resistance     | 51.8     | 49.4       | °C/W |
| R <sub>θJB</sub>              | Junction-to-board thermal resistance         | 49.4     | 62.8       | °C/W |
| Ψ <sub>JT</sub>               | Junction-to-top characterization parameter   | 13.5     | 5.9        | °C/W |
| Ψ <sub>JB</sub>               | Junction-to-board characterization parameter | 42.2     | 62.2       | °C/W |

- (1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, [SPRA953](#).

## 7.7 Electrical Characteristics

 $V_S = 1.8\text{ V to }5.5\text{ V}$ ; at  $T_A = 25^\circ\text{C}$ ,  $R_L = 10\text{ k}\Omega$  connected to  $V_S / 2$ ,  $V_{CM} = V_S / 2$ , and  $V_{OUT} = V_S / 2$  (unless otherwise noted)<sup>(1)</sup>

| PARAMETER                  |   | TEST CONDITIONS   | MIN   | TYP        | MAX           | UNIT                         |
|----------------------------|---|---|---|------------|---------------|------------------------------|
| <b>OFFSET VOLTAGE</b>      |   |   |   |            |               |                              |
| $V_{OS}$                   | Input offset voltage                              | $V_{CM} = (V_{S+}) - 1.3\text{ V}$ , $T_A = 25^\circ\text{C}$   |   | $\pm 0.75$ | $\pm 3$       | mV                           |
| $dV_{OS}/dT$               | $V_{OS}$ vs temperature                           | $T_A = -40^\circ\text{C to }+125^\circ\text{C}$   |   | 2          |               | $\mu\text{V}/^\circ\text{C}$ |
| PSRR                       | Power-supply rejection ratio                      | $V_{CM} = (V_{S+}) - 1.3\text{ V}$ , $T_A = 25^\circ\text{C}$   |   | $\pm 30$   | $\pm 135$     | $\mu\text{V}/\text{V}$       |
|                            | Channel separation, dc                            | At dc, $T_A = 25^\circ\text{C}$   |   | 100        |               | dB                           |
| <b>INPUT VOLTAGE RANGE</b> |   |   |   |            |               |                              |
| $V_{CM}$                   | Common-mode voltage range                         | $T_A = 25^\circ\text{C}$  | $(V_-) - 0.2$                                 |            | $(V_+) + 0.2$ | V                            |
| CMRR                       | Common-mode rejection ratio                       | $V_S = 5.5\text{ V}$ , $(V_{S-}) - 0.2\text{ V} < V_{CM} < (V_{S+}) - 1.3\text{ V}$ ,<br>$T_A = 25^\circ\text{C}$                                 | 72  | 96         |               | dB                           |
|                            |   | $V_S = 5.5\text{ V}$ , $V_{CM} = -0.2\text{ V to }5.7\text{ V}^{(2)}$ , $T_A = 25^\circ\text{C}$  |   | 75         |               |                              |
| <b>INPUT BIAS CURRENT</b>  |   |   |   |            |               |                              |
| $I_B$                      | Input bias current                                | $T_A = 25^\circ\text{C}$  |   | $\pm 1.0$  |               | pA                           |
| $I_{OS}$                   | Input offset current                              | $T_A = 25^\circ\text{C}$  |   | $\pm 1.0$  |               | pA                           |
| <b>NOISE</b>               |   |   |   |            |               |                              |
|                            | Input voltage noise (peak-to-peak)                | $f = 0.1\text{ Hz to }10\text{ Hz}$ , $T_A = 25^\circ\text{C}$  |   | 5          |               | $\mu\text{V}_{PP}$           |
| $e_n$                      | Input voltage noise density                       | $f = 10\text{ kHz}$ , $T_A = 25^\circ\text{C}$  |   | 15         |               | $\text{nV}/\sqrt{\text{Hz}}$ |
|                            |   | $f = 1\text{ kHz}$ , $T_A = 25^\circ\text{C}$   |   | 16         |               |                              |
| $i_n$                      | Input current noise density                       | $f = 1\text{ kHz}$ , $T_A = 25^\circ\text{C}$   |   | 6          |               | $\text{fA}/\sqrt{\text{Hz}}$ |
| <b>INPUT CAPACITANCE</b>   |   |   |   |            |               |                              |
| $C_{IN}$                   | Input capacitance                                 | Differential  | $V_S = 5\text{ V}$ , $T_A = 25^\circ\text{C}$ | 1          |               | pF                           |
|                            |   | Common-mode   | $V_S = 5\text{ V}$ , $T_A = 25^\circ\text{C}$ | 5          |               |                              |
| <b>OPEN-LOOP GAIN</b>      |   |   |   |            |               |                              |
| $A_{OL}$                   | Open-loop voltage gain                            | $V_S = 1.8\text{ V to }5.5\text{ V}$ , $0.2\text{ V} < V_O < (V_+) - 0.2\text{ V}$ ,<br>$R_L = 10\text{ k}\Omega$ , $T_A = 25^\circ\text{C}$      | 85  | 115        |               | dB                           |
|                            |   | $V_S = 1.8\text{ V to }5.5\text{ V}$ , $0.5\text{ V} < V_O < (V_+) - 0.5\text{ V}$ ,<br>$R_L = 2\text{ k}\Omega^{(2)}$ , $T_A = 25^\circ\text{C}$ | 85  | 100        |               |                              |
|                            | Phase margin                                      | $V_S = 5\text{ V}$ , $G = 1$ , $R_L = 10\text{ k}\Omega$ , $T_A = 25^\circ\text{C}$   |   | 65         |               | $^\circ$                     |
| <b>FREQUENCY RESPONSE</b>  |   |   |   |            |               |                              |
| GBW                        | Gain-bandwidth product                            | $V_S = 1.8\text{ V}$ , $R_L = 10\text{ k}\Omega$ , $C_L = 10\text{ pF}$ , $T_A = 25^\circ\text{C}$  |   | 2.7        |               | MHz                          |
|                            |   | $V_S = 5\text{ V}$ , $R_L = 10\text{ k}\Omega$ , $C_L = 10\text{ pF}$ , $T_A = 25^\circ\text{C}$  |   | 3          |               |                              |
| SR                         | Slew rate <sup>(3)</sup>                          | $V_S = 5\text{ V}$ , $G = 1$ , $T_A = 25^\circ\text{C}$   |   | 1.5        |               | $\text{V}/\mu\text{s}$       |
| $t_s$                      | Settling time                                     | To 0.1%, $V_S = 5\text{ V}$ , 2-V step, $G = 1$ , $T_A = 25^\circ\text{C}$  |   | 3          |               | $\mu\text{s}$                |
|                            | Overload recovery time                            | $V_S = 5\text{ V}$ , $V_{IN} \times \text{gain} > V_S$ , $T_A = 25^\circ\text{C}$   |   | 8          |               | $\mu\text{s}$                |
| THD+N                      | Total harmonic distortion + noise <sup>(4)</sup>  | $V_S = 5\text{ V}$ , $V_O = 1\text{ V}_{RMS}$ , $G = 1$ , $f = 1\text{ kHz}$ ,<br>$R_L = 10\text{ k}\Omega$ , $T_A = 25^\circ\text{C}$            |   | 0.005%     |               |                              |
| <b>OUTPUT</b>              |   |   |   |            |               |                              |
| $V_O$                      | Voltage output swing from supply rails            | $V_S = 1.8\text{ V to }5.5\text{ V}$ , $R_L = 10\text{ k}\Omega$ , $T_A = 25^\circ\text{C}$   |   | 5          | 25            | mV                           |
|                            |   | $V_S = 1.8\text{ V to }5.5\text{ V}$ , $R_L = 2\text{ k}\Omega$ , $T_A = 25^\circ\text{C}$  |   | 22         | 45            |                              |
| $I_{SC}$                   | Short-circuit current                             | $V_S = 5\text{ V}$ , $T_A = 25^\circ\text{C}$   |   | $\pm 20$   |               | mA                           |
| $R_O$                      | Open-loop output impedance                        | $V_S = 5.5\text{ V}$ , $f = 100\text{ Hz}$ , $T_A = 25^\circ\text{C}$   |   | 570        |               | $\Omega$                     |
| <b>POWER SUPPLY</b>        |   |   |   |            |               |                              |
| $V_S$                      | Specified voltage range                           |   | 1.8   |            | 5.5           | V                            |
| $I_Q$                      | Quiescent current per amplifier, over temperature | $V_S = 5\text{ V}$ , $I_O = 0\text{ mA}$ , $T_A = -40^\circ\text{C to }+125^\circ\text{C}$  |   | 150        | 250           | $\mu\text{A}$                |
| <b>TEMPERATURE</b>         |   |   |   |            |               |                              |
|                            | Specified range                                   |   | -40   |            | 125           | $^\circ\text{C}$             |
| $T_{stg}$                  | Storage range                                     |   | -65   |            | 150           | $^\circ\text{C}$             |

- Parameters with minimum or maximum specification limits are 100% production tested at  $25^\circ\text{C}$ , unless otherwise noted. Over-temperature limits are based on characterization and statistical analysis.
- Specified by design and characterization; not production tested.
- Signifies the slower value of the positive or negative slew rate.
- Third-order filter; bandwidth = 80 kHz at -3 dB.



## 7.8 Typical Characteristics

**Table 1. Table of Graphs**

| TITLE  | FIGURE                    |
|--|---------------------------|
| Open-Loop Gain and Phase vs Frequency                            | <a href="#">Figure 1</a>  |
| Quiescent Current vs Supply Voltage                              | <a href="#">Figure 2</a>  |
| Offset Voltage Production Distribution                           | <a href="#">Figure 3</a>  |
| Offset Voltage vs Common-Mode Voltage (Maximum Supply)           | <a href="#">Figure 4</a>  |
| Input Voltage Noise Spectral Density vs Frequency (1.8 V, 5.5 V) | <a href="#">Figure 5</a>  |
| Input Bias and Offset Current vs Temperature                     | <a href="#">Figure 6</a>  |
| Output Voltage Swing vs Output Current (over Temperature)        | <a href="#">Figure 7</a>  |
| Small-Signal Overshoot vs Load Capacitance                       | <a href="#">Figure 8</a>  |
| Small-Signal Step Response, Noninverting (1.8 V)                 | <a href="#">Figure 9</a>  |
| Large-Signal Step Response, Noninverting (1.8 V)                 | <a href="#">Figure 10</a> |
| No Phase Reversal  | <a href="#">Figure 11</a> |
| Channel Separation vs Frequency (Dual)                           | <a href="#">Figure 12</a> |
| EMIRR  | <a href="#">Figure 13</a> |

## 7.9 Typical Characteristics

at  $T_A = 25^\circ\text{C}$ ,  $R_L = 10\text{ k}\Omega$  connected to  $V_S / 2$ ,  $V_{CM} = V_S / 2$ , and  $V_{OUT} = V_S / 2$  (unless otherwise noted)

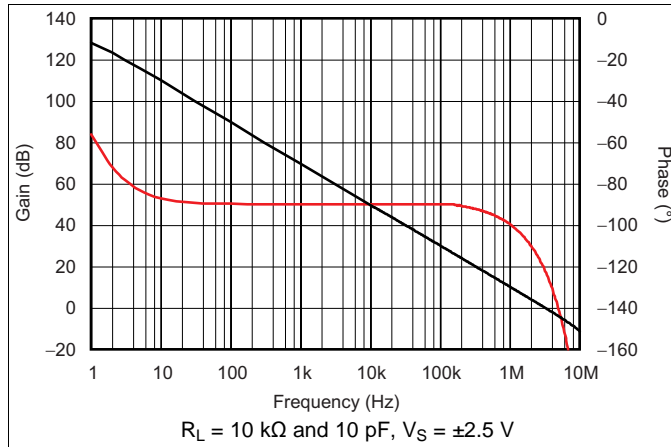


Figure 1. Open-Loop Gain and Phase vs Frequency

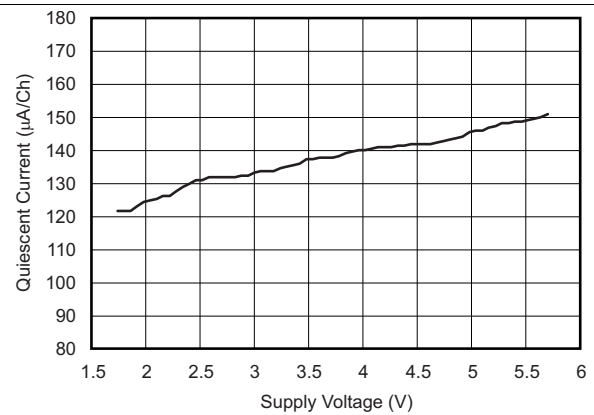


Figure 2. Quiescent Current vs Supply

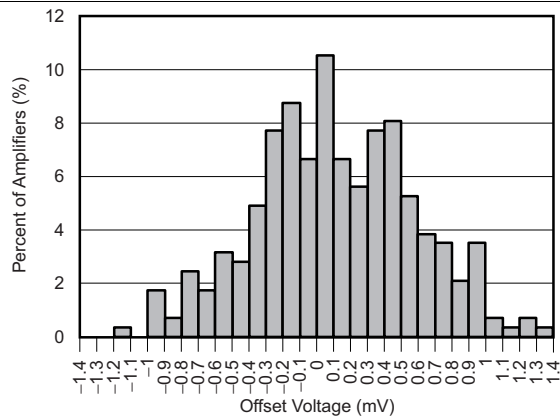


Figure 3. Offset Voltage Production Distribution

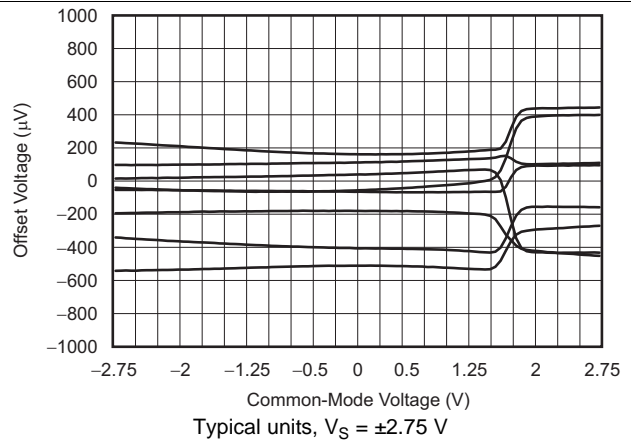


Figure 4. Offset Voltage vs Common-Mode Voltage

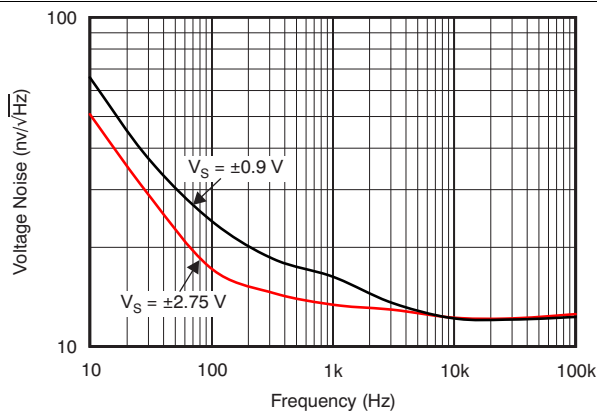


Figure 5. Input Voltage Noise Spectral Density vs Frequency

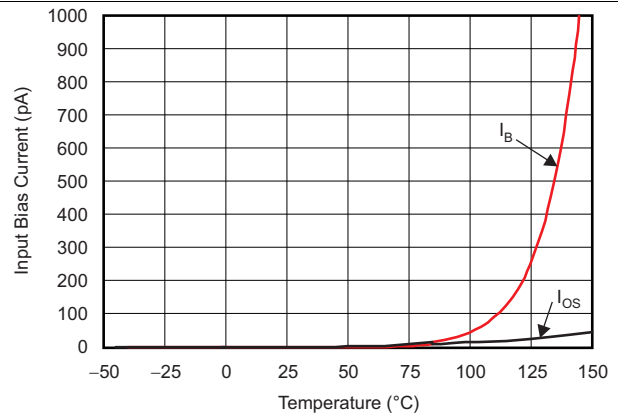


Figure 6. Input Bias and Offset Current vs Temperature

Typical Characteristics (continued)

at  $T_A = 25^\circ\text{C}$ ,  $R_L = 10\text{ k}\Omega$  connected to  $V_S / 2$ ,  $V_{CM} = V_S / 2$ , and  $V_{OUT} = V_S / 2$  (unless otherwise noted)

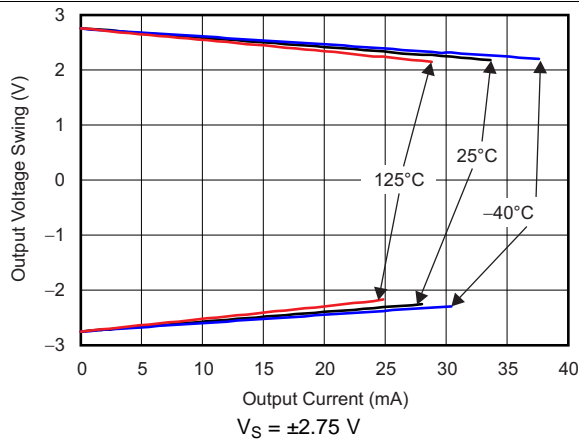


Figure 7. Output Voltage Swing vs Output Current (Over Temperature)

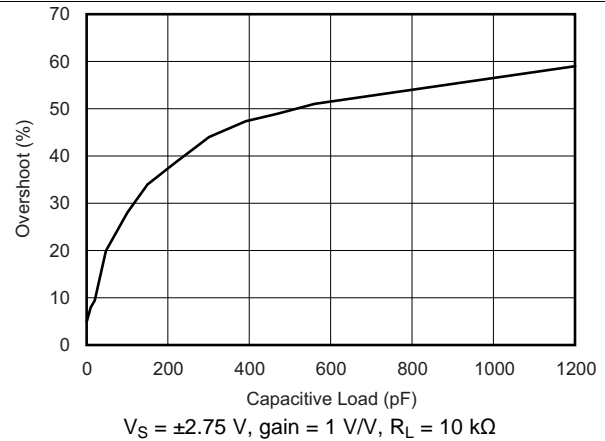


Figure 8. Small-Signal Overshoot vs Load Capacitance

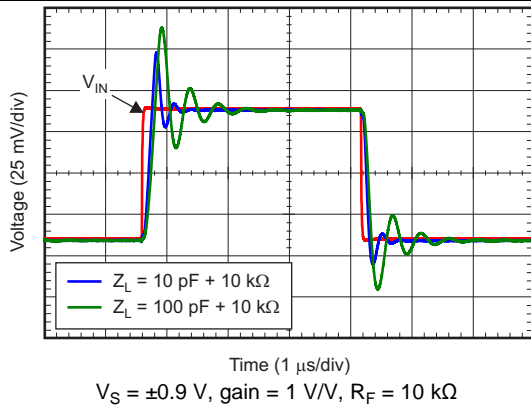


Figure 9. Small-Signal Pulse Response (Noninverting)

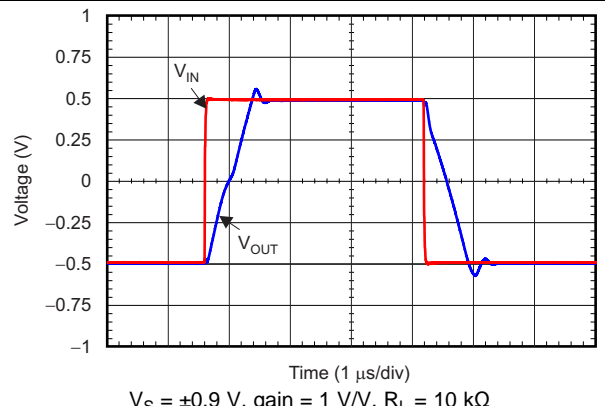


Figure 10. Large-Signal Pulse Response (Noninverting)

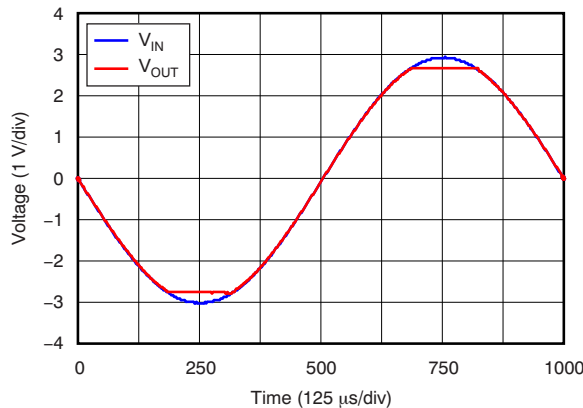


Figure 11. No Phase Reversal

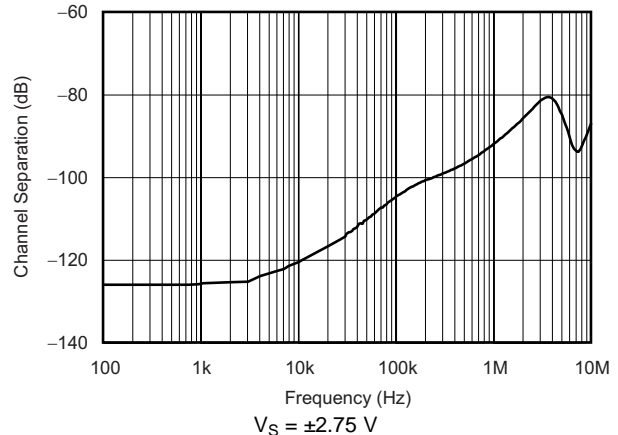
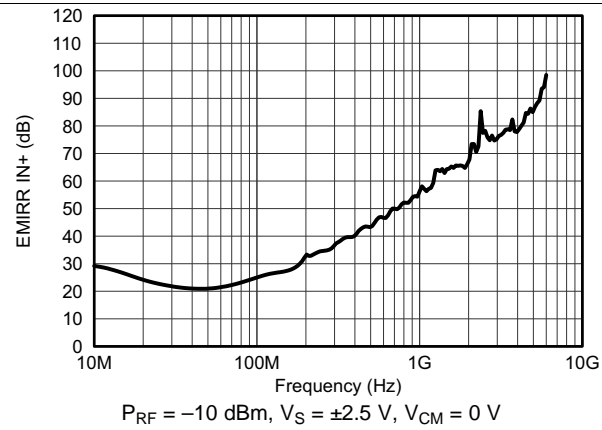


Figure 12. Channel Separation vs Frequency (TLV2314)

### Typical Characteristics (continued)

at  $T_A = 25^\circ\text{C}$ ,  $R_L = 10\text{ k}\Omega$  connected to  $V_S / 2$ ,  $V_{CM} = V_S / 2$ , and  $V_{OUT} = V_S / 2$  (unless otherwise noted)



**Figure 13. Electromagnetic Interference Rejection Ratio Referred to Noninverting Input (EMIRR IN+) vs Frequency**

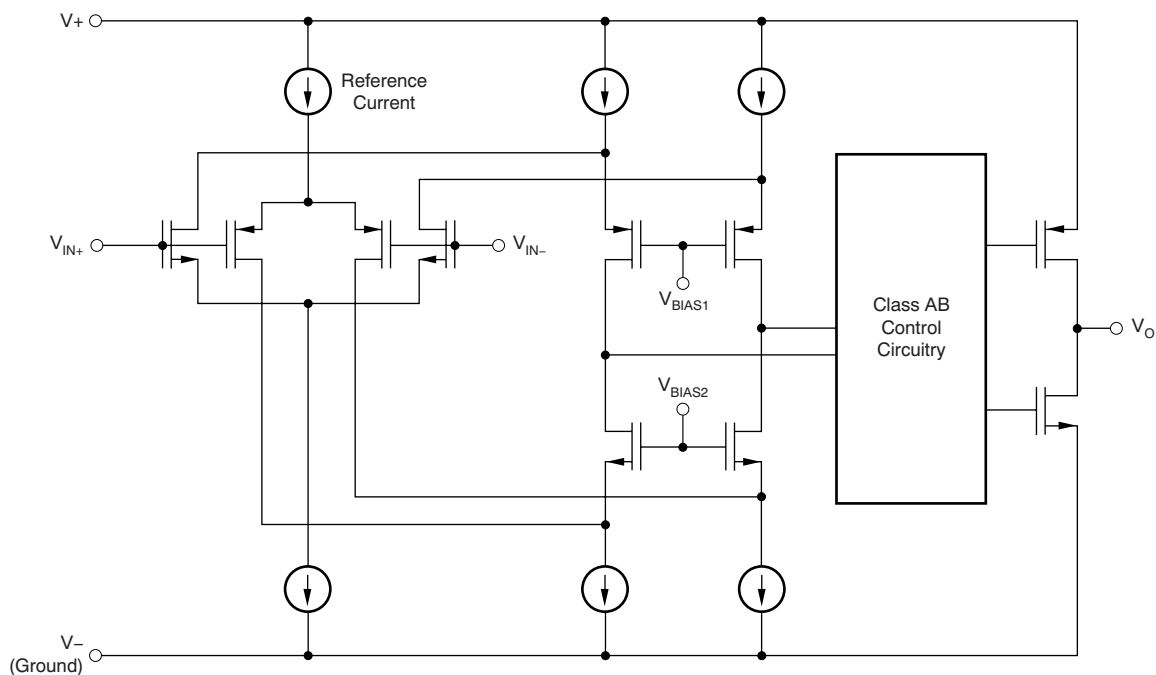
## 8 Detailed Description

### 8.1 Overview

The TLV314 is a family of low-power, rail-to-rail input and output operational amplifiers specifically designed for portable applications. These devices operate from 1.8 V to 5.5 V, are unity-gain stable, and suitable for a wide range of general-purpose applications. The class AB output stage is capable of driving  $\leq 10\text{-k}\Omega$  loads connected to any point between  $V+$  and ground. The input common-mode voltage range includes both rails, and allows the TLV314 series to be used in virtually any single-supply application. Rail-to-rail input and output swing significantly increases dynamic range, especially in low-supply applications, and makes these devices ideal for driving sampling analog-to-digital converters (ADCs).

The TLV314 features 3-MHz bandwidth and  $1.5\text{-V}/\mu\text{s}$  slew rate with only  $150\text{-}\mu\text{A}$  supply current per channel, providing good ac performance at very low power consumption. DC applications are also well served with a very low input noise voltage of  $14\text{ nV}/\sqrt{\text{Hz}}$  at 1 kHz, low input bias current ( $0.2\text{ pA}$ ), and an input offset voltage of  $0.5\text{ mV}$  (typical).

### 8.2 Functional Block Diagram



## 8.3 Feature Description

### 8.3.1 Operating Voltage

The TLV314 series of operational amplifiers is fully specified and ensured for operation from 1.8 V to 5.5 V. In addition, many specifications apply from  $-40^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$ . Parameters that vary significantly with operating voltages or temperature are provided in the [Typical Characteristics](#) section. Bypass power-supply pins with 0.01- $\mu\text{F}$  ceramic capacitors.

### 8.3.2 Rail-to-Rail Input

The input common-mode voltage range of the TLV314 series extends 200 mV beyond the supply rails. This performance is achieved with a complementary input stage: an N-channel input differential pair in parallel with a P-channel differential pair; see the [Functional Block Diagram](#) section. The N-channel pair is active for input voltages close to the positive rail, typically  $(V+) - 1.3\text{ V}$  to 200 mV above the positive supply, and the P-channel pair is on for inputs from 200 mV below the negative supply to approximately  $(V+) - 1.3\text{ V}$ . There is a small transition region, typically  $(V+) - 1.4\text{ V}$  to  $(V+) - 1.2\text{ V}$ , in which both pairs are on. This 200-mV transition region can vary up to 300 mV with process variation. Thus, the transition region (both stages on) can range from  $(V+) - 1.7\text{ V}$  to  $(V+) - 1.5\text{ V}$  on the low end, up to  $(V+) - 1.1\text{ V}$  to  $(V+) - 0.9\text{ V}$  on the high end. Within this transition region, PSRR, CMRR, offset voltage, offset drift, and THD can be degraded compared to device operation outside this region.

### 8.3.3 Rail-to-Rail Output

Designed as a micro-power, low-noise operational amplifier, the TLV314 delivers a robust output drive capability. A class AB output stage with common-source transistors is used to achieve full rail-to-rail output swing capability. For resistive loads up to 10 k $\Omega$ , the output typically swings to within 5 mV of either supply rail regardless of the power-supply voltage applied. Different load conditions change the ability of the amplifier to swing close to the rails; see [Figure 7](#).

### 8.3.4 Common-Mode Rejection Ratio (CMRR)

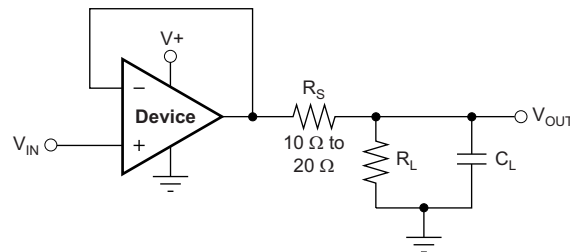
The CMRR for the TLV314 is specified in several ways so the best match for a given application can be used; see the [Electrical Characteristics](#) table. First, the CMRR of the device in the common-mode range below the transition region [ $V_{\text{CM}} < (V+) - 1.3\text{ V}$ ] is given. This specification is the best indicator of the capability of the device when the application requires using one of the differential input pairs. Second, the CMRR over the entire common-mode range is specified at ( $V_{\text{CM}} = -0.2\text{ V}$  to 5.7 V). This last value includes the variations measured through the transition region (see [Figure 4](#)).

## Feature Description (continued)

### 8.3.5 Capacitive Load and Stability

The TLV314 is designed to be used in applications where driving a capacitive load is required. As with all operational amplifiers, there may be specific instances where the TLV314 can become unstable. The particular operational amplifier circuit configuration, layout, gain, and output loading are some of the factors to consider when establishing whether or not an amplifier is stable in operation. An operational amplifier in the unity-gain (1 V/V) buffer configuration that drives a capacitive load exhibits a greater tendency to be unstable than an amplifier operated at a higher noise gain. The capacitive load, in conjunction with the operational amplifier output resistance, creates a pole within the feedback loop that degrades the phase margin. The degradation of the phase margin increases when capacitive loading increases. When operating in the unity-gain configuration, the TLV314 remains stable with a pure capacitive load up to approximately 1 nF. The equivalent series resistance (ESR) of some very large capacitors ( $C_L$  greater than 1  $\mu$ F) is sufficient to alter the phase characteristics in the feedback loop such that the amplifier remains stable. Increasing the amplifier closed-loop gain allows the amplifier to drive increasingly larger capacitance. This increased capability is evident when measuring the overshoot response of the amplifier at higher voltage gains; see [Figure 8](#).

One technique for increasing the capacitive load drive capability of the amplifier operating in a unity-gain configuration is to insert a small resistor (typically 10  $\Omega$  to 20  $\Omega$ ) in series with the output, as shown in [Figure 14](#). This resistor significantly reduces the overshoot and ringing associated with large capacitive loads. One possible problem with this technique, however, is that a voltage divider is created with the added series resistor and any resistor connected in parallel with the capacitive load. The voltage divider introduces a gain error at the output that reduces the output swing.



**Figure 14. Improving Capacitive Load Drive**

### 8.3.6 EMI Susceptibility and Input Filtering

Operational amplifiers vary with regard to the susceptibility of the device to electromagnetic interference (EMI). If conducted EMI enters the operational amplifier, the dc offset observed at the amplifier output can shift from its nominal value when EMI is present. This shift is a result of signal rectification associated with the internal semiconductor junctions. Although all operational amplifier pin functions can be affected by EMI, the signal input pins are likely to be the most susceptible. The TLV314 operational amplifier family incorporates an internal input low-pass filter that reduces the amplifiers response to EMI. Both common-mode and differential mode filtering are provided by this filter. The filter is designed for a cutoff frequency of approximately 80 MHz (–3 dB), with a roll-off of 20 dB per decade.

Texas Instruments has developed the ability to accurately measure and quantify the immunity of an operational amplifier over a broad frequency spectrum extending from 10 MHz to 6 GHz. The EMI rejection ratio (EMIRR) metric allows operational amplifiers to be directly compared by the EMI immunity. [Figure 13](#) illustrates the results of this testing on the TLV314. Detailed information can also be found in application report, *EMI Rejection Ratio of Operational Amplifiers* (SBOA128), available for download from [www.ti.com](http://www.ti.com).

## 8.4 Device Functional Modes

The TLV314 family has a single functional mode. These devices are powered on as long as the power-supply voltage is between 1.8 V ( $\pm 0.9$  V) and 5.5 V ( $\pm 2.75$  V).

## 9 Application and Implementation

### NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

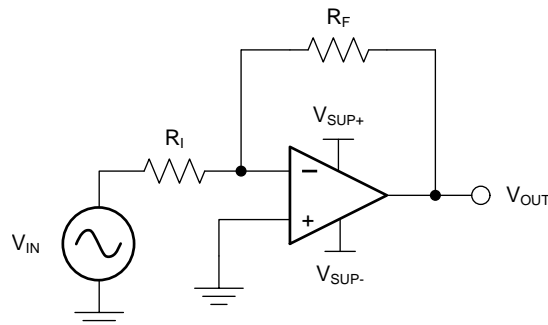
### 9.1 Application Information

The TLV314 device is a low-power, rail-to-rail input and output operational amplifier specifically designed for portable applications. These devices operate from 1.8 V to 5.5 V, are unity-gain stable, and suitable for a wide range of general-purpose applications. The class AB output stage is capable of driving  $\leq 10\text{-k}\Omega$  loads connected to any point between  $V_+$  and ground. The input common-mode voltage range includes both rails, and allows the TLV314 device to be used in virtually any single-supply application. Rail-to-rail input and output swing significantly increases dynamic range, especially in low-supply applications, and makes the device ideal for driving sampling analog-to-digital converters (ADCs).

The TLV314 family of devices features a 3-MHz bandwidth and 1.5-V/ $\mu\text{s}$  slew rate with only 150- $\mu\text{A}$  supply current per channel, providing good ac performance at very low power consumption. DC applications are also well served with a very-low input noise voltage of 14 nV/ $\sqrt{\text{Hz}}$  at 1 kHz, low-input bias current (0.2 pA), and an input offset voltage of 0.5 mV (typical).

### 9.2 Typical Application

A typical application for an operational amplifier is an inverting amplifier, as shown in [Figure 15](#). An inverting amplifier takes a positive voltage on the input and outputs a signal inverted to the input, making a negative voltage of the same magnitude. In the same manner, the amplifier also makes negative input voltages positive on the output. In addition, amplification can be added by selecting the input resistor  $R_I$  and the feedback resistor  $R_F$ .



**Figure 15. Application Schematic**

#### 9.2.1 Design Requirements

The supply voltage must be chosen to be larger than the input voltage range and the desired output range. The limits of the input common-mode range ( $V_{CM}$ ) and the output voltage swing to the rails ( $V_O$ ) must also be considered. For instance, this application scales a signal of  $\pm 0.5\text{ V}$  (1 V) to  $\pm 1.8\text{ V}$  (3.6 V). Setting the supply at  $\pm 2.5\text{ V}$  is sufficient to accommodate this application.

#### 9.2.2 Detailed Design Procedure

Determine the gain required by the inverting amplifier using [Equation 1](#) and [Equation 2](#):

$$A_V = \frac{V_{OUT}}{V_{IN}} \quad (1)$$

$$A_V = \frac{1.8}{-0.5} = -3.6 \quad (2)$$



### Typical Application (continued)

When the desired gain is determined, choose a value for  $R_1$  or  $R_F$ . Choosing a value in the kilo ohm range is desirable for general-purpose applications because the amplifier circuit uses currents in the milliamp range. This milliamp current range ensures the device does not draw too much current. The trade-off is that very large resistors (100s of kilo ohms) draw the smallest current but generate the highest noise. Very small resistors (100s of ohms) generate low noise but draw high current. This example uses 10 k $\Omega$  for  $R_1$ , meaning 36 k $\Omega$  is used for  $R_F$ . These values are determined by [Equation 3](#):

$$A_V = -\frac{R_F}{R_1} \quad (3)$$

### 9.2.3 Application Curve

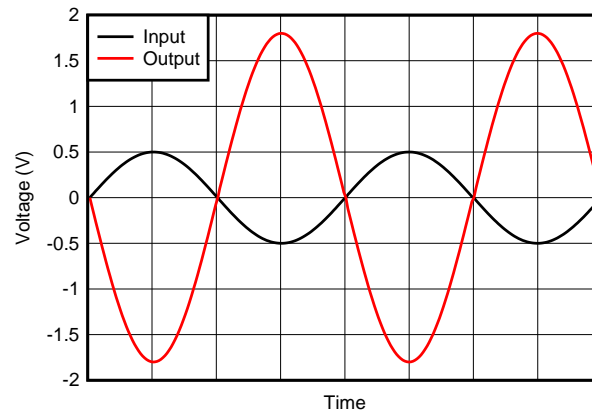
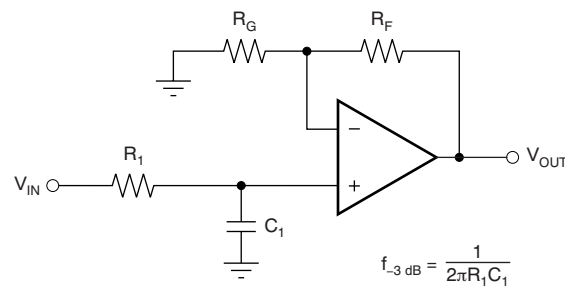


Figure 16. Inverting Amplifier Input and Output

### 9.3 System Examples

When receiving low-level signals, limiting the bandwidth of the incoming signals into the system is often required. The simplest way to establish this limited bandwidth is to place an RC filter at the noninverting terminal of the amplifier, as [Figure 17](#) shows.

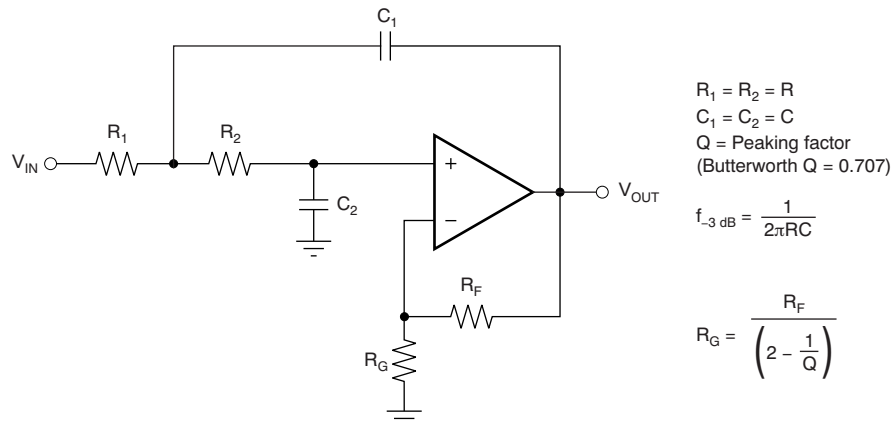


$$\frac{V_{OUT}}{V_{IN}} = \left(1 + \frac{R_F}{R_G}\right) \left(\frac{1}{1 + sR_1C_1}\right)$$

Figure 17. Single-Pole, Low-Pass Filter

### System Examples (continued)

If even more attenuation is needed, a multiple pole filter is required. The Sallen-Key filter can be used for this task, as [Figure 18](#) shows. For best results, the amplifier must have a bandwidth that is eight to ten times the filter frequency bandwidth. Failure to follow this guideline can result in phase shift of the amplifier.



**Figure 18. Two-Pole, Low-Pass, Sallen-Key Filter**

## 10 Power Supply Recommendations

The TLV314 family is specified for operation from 1.8 V to 5.5 V ( $\pm 0.9$  V to  $\pm 2.75$  V); many specifications apply from  $-40^\circ\text{C}$  to  $+125^\circ\text{C}$ . The [Typical Characteristics](#) section presents parameters that can exhibit significant variance with regard to operating voltage or temperature.

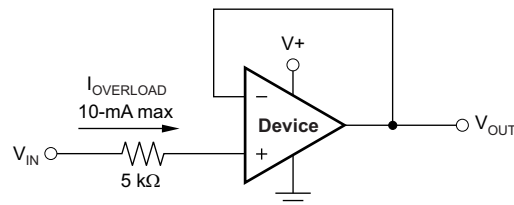
### CAUTION

Supply voltages larger than 7 V can permanently damage the device (see the [Absolute Maximum Ratings](#) table).

Place 0.1- $\mu\text{F}$  bypass capacitors close to the power-supply pins to reduce errors coupling in from noisy or high-impedance power supplies. For more detailed information on bypass capacitor placement; see the [Layout Guidelines](#) section.

### 10.1 Input and ESD Protection

The TLV314 family incorporates internal electrostatic discharge (ESD) protection circuits on all pins. In the case of input and output pins, this protection primarily consists of current-steering diodes connected between the input and power-supply pins. These ESD protection diodes also provide in-circuit, input overdrive protection, as long as the current is limited to 10 mA as stated in the [Absolute Maximum Ratings](#) table. [Figure 19](#) shows how a series input resistor can be added to the driven input to limit the input current. The added resistor contributes thermal noise at the amplifier input, which must be kept to a minimum in noise-sensitive applications.



**Figure 19. Input Current Protection**

## 11 Layout

### 11.1 Layout Guidelines

For best operational performance of the device, use good printed circuit board (PCB) layout practices, including:

- Noise can propagate into analog circuitry through the power pins of the circuit as a whole and the operational amplifier. Use bypass capacitors to reduce the coupled noise by providing low-impedance power sources local to the analog circuitry.
  - Connect low-ESR, 0.1- $\mu$ F ceramic bypass capacitors between each supply pin and ground, placed as close to the device as possible. A single bypass capacitor from V+ to ground is applicable for single-supply applications.
- Separate grounding for analog and digital portions of the circuitry is one of the simplest and most effective methods of noise suppression. One or more layers on multilayer PCBs are usually devoted to ground planes. A ground plane helps distribute heat and reduces EMI noise pickup. Make sure to physically separate digital and analog grounds, paying attention to the flow of the ground current. For more detailed information, see *Circuit Board Layout Techniques*, [SLOA089](#).
- To reduce parasitic coupling, run the input traces as far away from the supply or output traces as possible. If these traces cannot be kept separate, crossing the sensitive trace perpendicularly is much better than crossing in parallel with the noisy trace.
- Place the external components as close to the device as possible. Keep  $R_F$  and  $R_G$  close to the inverting input in order to minimize parasitic capacitance, as shown in [Figure 20](#).
- Keep the length of input traces as short as possible. Always remember that the input traces are the most sensitive part of the circuit.
- Consider a driven, low-impedance guard ring around the critical traces. A guard ring can significantly reduce leakage currents from nearby traces that are at different potentials.

### 11.2 Layout Example

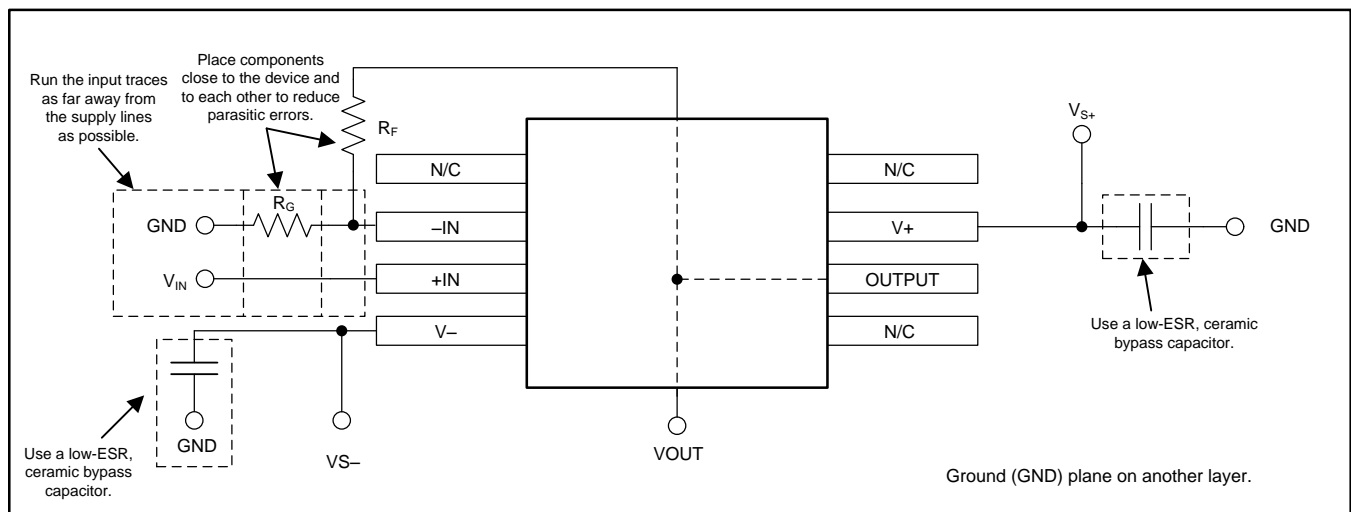
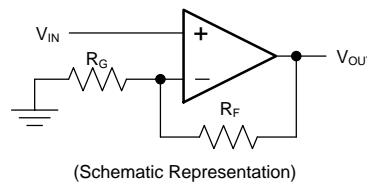


Figure 20. Operational Amplifier Board Layout for Noninverting Configuration

## 12 Device and Documentation Support

### 12.1 Device Support

### 12.2 Documentation Support

#### 12.2.1 Related Documentation

For related documentation, see the following:

- *EMI Rejection Ratio of Operational Amplifiers*, [SBOA128](#)
- *Circuit Board Layout Techniques*, [SLOA089](#)
- *QFN/SON PCB Attachment*, [SLUA271](#)
- *Quad Flatpack No-Lead Logic Packages*, [SCBA017](#)

### 12.3 Related Links

[Table 2](#) lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

**Table 2. Related Links**

| PARTS   | PRODUCT FOLDER             | SAMPLE & BUY               | TECHNICAL DOCUMENTS        | TOOLS & SOFTWARE           | SUPPORT & COMMUNITY        |
|---------|----------------------------|----------------------------|----------------------------|----------------------------|----------------------------|
| TLV314  | <a href="#">Click here</a> | <a href="#">Click here</a> | <a href="#">Click here</a> | <a href="#">Click here</a> | <a href="#">Click here</a> |
| TLV2314 | <a href="#">Click here</a> | <a href="#">Click here</a> | <a href="#">Click here</a> | <a href="#">Click here</a> | <a href="#">Click here</a> |
| TLV4314 | <a href="#">Click here</a> | <a href="#">Click here</a> | <a href="#">Click here</a> | <a href="#">Click here</a> | <a href="#">Click here</a> |

### 12.4 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

**TI E2E™ Online Community** *TI's Engineer-to-Engineer (E2E) Community*. Created to foster collaboration among engineers. At [e2e.ti.com](http://e2e.ti.com), you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

**Design Support** *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

### 12.5 Trademarks

E2E is a trademark of Texas Instruments.  
All other trademarks are the property of their respective owners.

### 12.6 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

### 12.7 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

## 13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

**PACKAGING INFORMATION**

| Orderable Device | Status<br>(1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan<br>(2)         | Lead/Ball Finish<br>(6) | MSL Peak Temp<br>(3) | Op Temp (°C) | Device Marking<br>(4/5) | Samples                 |
|------------------|---------------|--------------|-----------------|------|-------------|-------------------------|-------------------------|----------------------|--------------|-------------------------|-------------------------|
| TLV2314IDGKR     | ACTIVE        | VSSOP        | DGK             | 8    | 2500        | Green (RoHS & no Sb/Br) | CU NIPDAUAG             | Level-2-260C-1 YEAR  | -40 to 125   | 13E7                    | <a href="#">Samples</a> |
| TLV2314IDGKT     | ACTIVE        | VSSOP        | DGK             | 8    | 250         | Green (RoHS & no Sb/Br) | CU NIPDAUAG             | Level-2-260C-1 YEAR  | -40 to 125   | 13E7                    | <a href="#">Samples</a> |
| TLV2314IDR       | ACTIVE        | SOIC         | D               | 8    | 2500        | Green (RoHS & no Sb/Br) | CU NIPDAU               | Level-2-260C-1 YEAR  | -40 to 125   | V2314                   | <a href="#">Samples</a> |
| TLV314IDBVR      | ACTIVE        | SOT-23       | DBV             | 5    | 3000        | Green (RoHS & no Sb/Br) | CU NIPDAU               | Level-2-260C-1 YEAR  | -40 to 125   | 12H                     | <a href="#">Samples</a> |
| TLV314IDBVT      | ACTIVE        | SOT-23       | DBV             | 5    | 250         | Green (RoHS & no Sb/Br) | CU NIPDAU               | Level-2-260C-1 YEAR  | -40 to 125   | 12H                     | <a href="#">Samples</a> |
| TLV314IDCKR      | ACTIVE        | SC70         | DCK             | 5    | 3000        | Green (RoHS & no Sb/Br) | CU NIPDAU               | Level-1-260C-UNLIM   | -40 to 125   | 12I                     | <a href="#">Samples</a> |
| TLV314IDCKT      | ACTIVE        | SC70         | DCK             | 5    | 250         | Green (RoHS & no Sb/Br) | CU NIPDAU               | Level-1-260C-UNLIM   | -40 to 125   | 12I                     | <a href="#">Samples</a> |
| TLV4314IPWR      | ACTIVE        | TSSOP        | PW              | 14   | 2000        | Green (RoHS & no Sb/Br) | CU NIPDAU               | Level-2-260C-1 YEAR  | -40 to 125   | V4314                   | <a href="#">Samples</a> |

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

**Important Information and Disclaimer:**The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

| Device       | Package Type | Package Drawing | Pins | SPQ  | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|--------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| TLV2314IDGKR | VSSOP        | DGK             | 8    | 2500 | 330.0              | 12.4               | 5.3     | 3.4     | 1.4     | 8.0     | 12.0   | Q1            |
| TLV2314IDGKT | VSSOP        | DGK             | 8    | 250  | 330.0              | 12.4               | 5.3     | 3.4     | 1.4     | 8.0     | 12.0   | Q1            |
| TLV2314IDR   | SOIC         | D               | 8    | 2500 | 330.0              | 12.4               | 6.4     | 5.2     | 2.1     | 8.0     | 12.0   | Q1            |
| TLV314IDBVR  | SOT-23       | DBV             | 5    | 3000 | 178.0              | 9.0                | 3.23    | 3.17    | 1.37    | 4.0     | 8.0    | Q3            |
| TLV314IDBVT  | SOT-23       | DBV             | 5    | 250  | 178.0              | 9.0                | 3.23    | 3.17    | 1.37    | 4.0     | 8.0    | Q3            |
| TLV314IDCKR  | SC70         | DCK             | 5    | 3000 | 178.0              | 9.0                | 2.4     | 2.5     | 1.2     | 4.0     | 8.0    | Q3            |
| TLV314IDCKT  | SC70         | DCK             | 5    | 250  | 178.0              | 9.0                | 2.4     | 2.5     | 1.2     | 4.0     | 8.0    | Q3            |
| TLV4314IPWR  | TSSOP        | PW              | 14   | 2000 | 330.0              | 12.4               | 6.9     | 5.6     | 1.6     | 8.0     | 12.0   | Q1            |

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

| Device       | Package Type | Package Drawing | Pins | SPQ  | Length (mm) | Width (mm) | Height (mm) |
|--------------|--------------|-----------------|------|------|-------------|------------|-------------|
| TLV2314IDGKR | VSSOP        | DGK             | 8    | 2500 | 366.0       | 364.0      | 50.0        |
| TLV2314IDGKT | VSSOP        | DGK             | 8    | 250  | 366.0       | 364.0      | 50.0        |
| TLV2314IDR   | SOIC         | D               | 8    | 2500 | 367.0       | 367.0      | 35.0        |
| TLV314IDBVR  | SOT-23       | DBV             | 5    | 3000 | 180.0       | 180.0      | 18.0        |
| TLV314IDBVT  | SOT-23       | DBV             | 5    | 250  | 180.0       | 180.0      | 18.0        |
| TLV314IDCKR  | SC70         | DCK             | 5    | 3000 | 180.0       | 180.0      | 18.0        |
| TLV314IDCKT  | SC70         | DCK             | 5    | 250  | 180.0       | 180.0      | 18.0        |
| TLV4314IPWR  | TSSOP        | PW              | 14   | 2000 | 367.0       | 367.0      | 35.0        |



## GENERIC PACKAGE VIEW

DBV 5

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



Images above are just a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.

4073253/P

DBV0005A



# PACKAGE OUTLINE

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



4214839/C 04/2017

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC MO-178.

# EXAMPLE BOARD LAYOUT

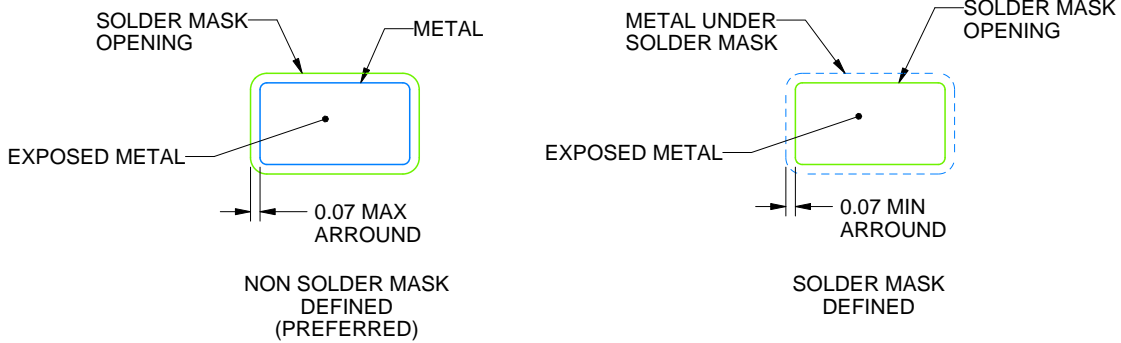
DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE:15X



SOLDER MASK DETAILS

4214839/C 04/2017

NOTES: (continued)

- Publication IPC-7351 may have alternate designs.
- Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:15X

4214839/C 04/2017

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
7. Board assembly site may have different recommendations for stencil design.



PW (R-PDSO-G14)

PLASTIC SMALL OUTLINE



- NOTES:
- All linear dimensions are in millimeters.
  - This drawing is subject to change without notice.
  - Publication IPC-7351 is recommended for alternate designs.
  - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.



D (R-PDSO-G8)

PLASTIC SMALL OUTLINE



4211283-2/E 08/12

- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Publication IPC-7351 is recommended for alternate designs.
  - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.



DGK (S-PDSO-G8)

PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.
  - D. Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
  - E. Falls within JEDEC MO-187 variation AA, except interlead flash.



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Publication IPC-7351 is recommended for alternate designs.
  - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

DCK (R-PDSO-G5)

PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
  - D. Falls within JEDEC MO-203 variation AA.

DCK (R-PDSO-G5)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
  - D. Publication IPC-7351 is recommended for alternate designs.
  - E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.

## IMPORTANT NOTICE

Texas Instruments Incorporated (TI) reserves the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete.

TI's published terms of sale for semiconductor products (<http://www.ti.com/sc/docs/stdterms.htm>) apply to the sale of packaged integrated circuit products that TI has qualified and released to market. Additional terms may apply to the use or sale of other types of TI products and services.

Reproduction of significant portions of TI information in TI data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such reproduced documentation. Information of third parties may be subject to additional restrictions. Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyers and others who are developing systems that incorporate TI products (collectively, "Designers") understand and agree that Designers remain responsible for using their independent analysis, evaluation and judgment in designing their applications and that Designers have full and exclusive responsibility to assure the safety of Designers' applications and compliance of their applications (and of all TI products used in or for Designers' applications) with all applicable regulations, laws and other applicable requirements. Designer represents that, with respect to their applications, Designer has all the necessary expertise to create and implement safeguards that (1) anticipate dangerous consequences of failures, (2) monitor failures and their consequences, and (3) lessen the likelihood of failures that might cause harm and take appropriate actions. Designer agrees that prior to using or distributing any applications that include TI products, Designer will thoroughly test such applications and the functionality of such TI products as used in such applications.

TI's provision of technical, application or other design advice, quality characterization, reliability data or other services or information, including, but not limited to, reference designs and materials relating to evaluation modules, (collectively, "TI Resources") are intended to assist designers who are developing applications that incorporate TI products; by downloading, accessing or using TI Resources in any way, Designer (individually or, if Designer is acting on behalf of a company, Designer's company) agrees to use any particular TI Resource solely for this purpose and subject to the terms of this Notice.

TI's provision of TI Resources does not expand or otherwise alter TI's applicable published warranties or warranty disclaimers for TI products, and no additional obligations or liabilities arise from TI providing such TI Resources. TI reserves the right to make corrections, enhancements, improvements and other changes to its TI Resources. TI has not conducted any testing other than that specifically described in the published documentation for a particular TI Resource.

Designer is authorized to use, copy and modify any individual TI Resource only in connection with the development of applications that include the TI product(s) identified in such TI Resource. NO OTHER LICENSE, EXPRESS OR IMPLIED, BY ESTOPPEL OR OTHERWISE TO ANY OTHER TI INTELLECTUAL PROPERTY RIGHT, AND NO LICENSE TO ANY TECHNOLOGY OR INTELLECTUAL PROPERTY RIGHT OF TI OR ANY THIRD PARTY IS GRANTED HEREIN, including but not limited to any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information regarding or referencing third-party products or services does not constitute a license to use such products or services, or a warranty or endorsement thereof. Use of TI Resources may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

TI RESOURCES ARE PROVIDED "AS IS" AND WITH ALL FAULTS. TI DISCLAIMS ALL OTHER WARRANTIES OR REPRESENTATIONS, EXPRESS OR IMPLIED, REGARDING RESOURCES OR USE THEREOF, INCLUDING BUT NOT LIMITED TO ACCURACY OR COMPLETENESS, TITLE, ANY EPIDEMIC FAILURE WARRANTY AND ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, AND NON-INFRINGEMENT OF ANY THIRD PARTY INTELLECTUAL PROPERTY RIGHTS. TI SHALL NOT BE LIABLE FOR AND SHALL NOT DEFEND OR INDEMNIFY DESIGNER AGAINST ANY CLAIM, INCLUDING BUT NOT LIMITED TO ANY INFRINGEMENT CLAIM THAT RELATES TO OR IS BASED ON ANY COMBINATION OF PRODUCTS EVEN IF DESCRIBED IN TI RESOURCES OR OTHERWISE. IN NO EVENT SHALL TI BE LIABLE FOR ANY ACTUAL, DIRECT, SPECIAL, COLLATERAL, INDIRECT, PUNITIVE, INCIDENTAL, CONSEQUENTIAL OR EXEMPLARY DAMAGES IN CONNECTION WITH OR ARISING OUT OF TI RESOURCES OR USE THEREOF, AND REGARDLESS OF WHETHER TI HAS BEEN ADVISED OF THE POSSIBILITY OF SUCH DAMAGES.

Unless TI has explicitly designated an individual product as meeting the requirements of a particular industry standard (e.g., ISO/TS 16949 and ISO 26262), TI is not responsible for any failure to meet such industry standard requirements.

Where TI specifically promotes products as facilitating functional safety or as compliant with industry functional safety standards, such products are intended to help enable customers to design and create their own applications that meet applicable functional safety standards and requirements. Using products in an application does not by itself establish any safety features in the application. Designers must ensure compliance with safety-related requirements and standards applicable to their applications. Designer may not use any TI products in life-critical medical equipment unless authorized officers of the parties have executed a special contract specifically governing such use. Life-critical medical equipment is medical equipment where failure of such equipment would cause serious bodily injury or death (e.g., life support, pacemakers, defibrillators, heart pumps, neurostimulators, and implantables). Such equipment includes, without limitation, all medical devices identified by the U.S. Food and Drug Administration as Class III devices and equivalent classifications outside the U.S.

TI may expressly designate certain products as completing a particular qualification (e.g., Q100, Military Grade, or Enhanced Product). Designers agree that it has the necessary expertise to select the product with the appropriate qualification designation for their applications and that proper product selection is at Designers' own risk. Designers are solely responsible for compliance with all legal and regulatory requirements in connection with such selection.

Designer will fully indemnify TI and its representatives against any damages, costs, losses, and/or liabilities arising out of Designer's non-compliance with the terms and provisions of this Notice.