FAIRCHILD

SEMICONDUCTOR®

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74VHC74
Dual D-Type Flip-Flop with Preset and Clear

General Description

The VHC74 is an advanced high speed CMOS Dual D-Type Flip-Flop fabricated with silicon gate CMOS technology. It achieves the high speed operation similar to equivalent Bipolar Schottky TTL while maintaining the CMOS low power dissipation. The signal level applied to the D input is transferred to the Q output during the positive going transition of the CK pulse. $\overline{CLR}$ and $\overline{PR}$ are independent of the CK and are accomplished by setting the appropriate input LOW.

An input protection circuit ensures that 0V to 7V can be applied to the input pins without regard to the supply voltage. This device can be used to interface 5V to 3V systems and two supply systems such as battery backup. This circuit prevents device destruction due to mismatched supply and input voltages.

Features

■ High Speed: f_{MAX} = 170 MHz (typ) at T_A = 25°C
■ High noise immunity: V_{NIH} = V_{NIL} = 28% V_{CC} (min)
■ Power down protection is provided on all inputs
■ Low power dissipation: I_{CC} = 2 μA (max) at T_A = 25°C
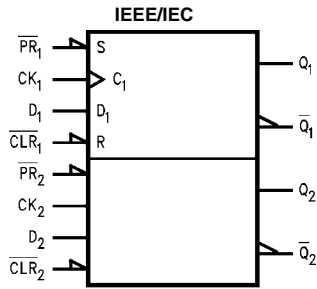■ Pin and function compatible with 74HC74

Ordering Code:

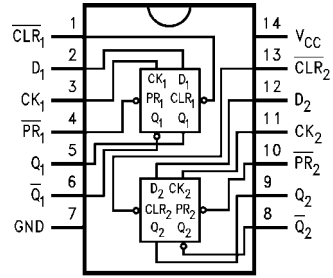| Order Number	Package Number	Package Description
74VHC74M	M14A	14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow
74VHC74MX_NL	M14A	Pb-Free 14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow
74VHC74SJ	M14D	Pb-Free 14-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
74VHC74MTC	MTC14	14-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
74VHC74MTCX_NL (Note 1)	MTC14	Pb-Free 14-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
74VHC74N	N14A	14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide

Surface mount packages are also available on Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.
Pb-Free package per JEDED J-STD-020B.

Note 1: "_NL" indicates Pb-Free package (per JEDEC J-STD-020B). Device available in Tape and Reel only.

74VHC74

Logic Symbol

IEEE/IEC

$\overline{PR}_1$ — S

CK_1 — $\triangleright$ C_1

D_1 — D_1

$\overline{CLR}_1$ — R

— Q_1

— $\overline{Q}_1$

$\overline{PR}_2$ —

CK_2 —

D_2 —

$\overline{CLR}_2$ —

— Q_2

— $\overline{Q}_2$

Connection Diagram

$\overline{CLR}_1$	1	14	V_{CC}
D_1	2	13	$\overline{CLR}_2$
CK_1	3	12	D_2
$\overline{PR}_1$	4	11	CK_2
Q_1	5	10	$\overline{PR}_2$
$\overline{Q}_1$	6	9	Q_2
GND	7	8	$\overline{Q}_2$

Internal: CK_1 D_1 / PR_1 CLR_1 / Q_1 $\overline{Q}_1$; D_2 CK_2 / CLR_2 PR_2 / Q_2 $\overline{Q}_2$

Pin Descriptions

Pin Names	Description
D_1, D_2	Data Inputs
CK_1, CK_2	Clock Pulse Inputs
$\overline{CLR}_1$, $\overline{CLR}_2$	Direct Clear Inputs
$\overline{PR}_1$, $\overline{PR}_2$	Direct Preset Inputs
Q_1, $\overline{Q}_1$, Q_2, $\overline{Q}_2$	Output

Truth Table

Inputs				Outputs		Function
CLR	$\overline{\textbf{PR}}$	**D**	**CK**	**Q**	$\overline{\textbf{Q}}$	
L	H	X	X	L	H	Clear
H	L	X	X	H	L	Preset
L	L	X	X	H (Note 2)	H (Note 2)	
H	H	L	$\diagup$	L	H	
H	H	H	$\diagup$	H	L	
H	H	X	$\diagdown$	Q_n	Q_n	No Change

Note 2: This configuration is nonstable; that is, it will not persist when preset and clear inputs return to their inactive (HIGH) state.

Absolute Maximum Ratings(Note 3)

Supply Voltage (V_{CC})	−0.5V to +7.0V
DC Input Voltage (V_{IN})	−0.5V to +7.0V
DC Output Voltage (V_{OUT})	−0.5V to V_{CC} + 0.5V
Input Diode Current (I_{IK})	−20 mA
Output Diode Current (I_{OK})	±20 mA
DC Output Current (I_{OUT})	±25 mA
DC V_{CC}/GND Current (I_{CC})	±50 mA
Storage Temperature (T_{STG})	−65°C to +150°C
Lead Temperature (T_L)	
Soldering (10 seconds)	260°C

Recommended Operating Conditions (Note 4)

Supply Voltage (V_{CC})	2.0V to 5.5V
Input Voltage (V_{IN})	0V to +5.5V
Output Voltage (V_{OUT})	0V to V_{CC}
Operating Temperature (T_{OPR})	−40°C to +85°C
Input Rise and Fall Time (t_r, t_f)	
V_{CC} = 3.3V ± 0.3V	0 ~ 100 ns/V
V_{CC} = 5.0V ± 0.5V	0 ~ 20 ns/V

Note 3: Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading varaibles. Fairchild does not recommend operation outside databook specifications.

Note 4: Unused inputs must be held HIGH or LOW. They may not float.

DC Electrical Characteristics

Symbol	Parameter	V_{CC} (V)	T_A = 25°C			T_A = −40°C to +85°C		Units	Conditions	
			Min	Typ	Max	Min	Max			
V_{IH}	HIGH Level Input	2.0	1.50			1.50		V		
	Voltage	3.0 – 5.5	0.7 V_{CC}			0.7 V_{CC}				
V_{IL}	LOW Level Input	2.0			0.50		0.50	V		
	Voltage	3.0 – 5.5			0.3 V_{CC}		0.3 V_{CC}			
V_{OH}	HIGH Level Output	2.0	1.9	2.0		1.9		V	V_{IN} = V_{IH} or V_{IL}	I_{OH} = −50 μA
	Voltage	3.0	2.9	3.0		2.9				
		4.5	4.4	4.5		4.4				
		3.0	2.58			2.48		V		I_{OH} = −4 mA
		4.5	3.94			3.80				I_{OH} = −8 mA
V_{OL}	LOW Level Output	2.0		0.0	0.1		0.1	V	V_{IN} = V_{IH} or V_{IL}	I_{OL} = 50 μA
	Voltage	3.0		0.0	0.1		0.1			
		4.5		0.0	0.1		0.1			
		3.0			0.36		0.44	V		I_{OL} = 4 mA
		4.5			0.36		0.44			I_{OL} = 8 mA
I_{IN}	Input Leakage Current	0 – 5.5			±0.1		±1.0	μA	V_{IN} = 5.5V or GND	
I_{CC}	Quiescent Supply Current	5.5			2.0		20.0	μA	V_{IN} = V_{CC} or GND	

AC Electrical Characteristics

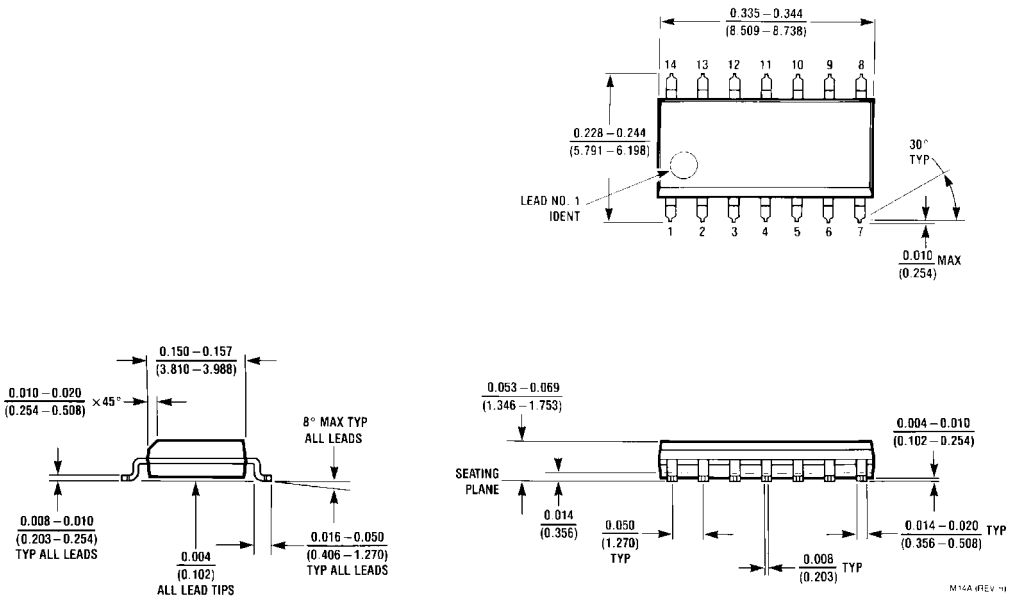| Symbol	Parameter	V_{CC} (V)	$T_A = 25°C$			$T_A = -40°C$ to $+85°C$		Units	Conditions
			Min	Typ	Max	Min	Max		
f_{MAX}	Maximum Clock Frequency	3.3 ± 0.3	80	125		70		MHz	$C_L = 15$ pF
			50	75		45			$C_L = 50$ pF
		5.0 ± 0.5	130	170		110		MHz	$C_L = 15$ pF
			90	115		75			$C_L = 50$ pF
t_{PLH}	Propagation Delay	3.3 ± 0.3		6.7	11.9	1.0	14.0	ns	$C_L = 15$ pF
t_{PHL}	Time (CK-Q, $\overline{Q}$)			9.2	15.4	1.0	17.5		$C_L = 50$ pF
		5.0 ± 0.5		4.6	7.3	1.0	8.5	ns	$C_L = 15$ pF
				6.1	9.3	1.0	10.5		$C_L = 50$ pF
t_{PLH}	Propagation Delay Time	3.3 ± 0.3		7.6	12.3	1.0	14.5	ns	$C_L = 15$ pF
t_{PHL}	($\overline{CLR}$, $\overline{PR}$ -Q, $\overline{Q}$)			10.1	15.8	1.0	18.0		$C_L = 50$ pF
		5.0 ± 0.5		4.8	7.7	1.0	9.0	ns	$C_L = 15$ pF
				6.3	9.7	1.0	11.0		$C_L = 50$ pF
C_{IN}	Input Capacitance			4	10		10	pF	V_{CC} = Open
C_{PD}	Power Dissipation Capacitance			25				pF	(Note 5)

Note 5: C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained from the equation: I_{CC} (opr.) = $C_{PD} * V_{CC} * f_{IN} + I_{CC}/2$ (per F/F).

AC Operating Requirements

Symbol	Parameter	V_{CC} (V) (Note 6)	$T_A = 25°C$	$T_A = -40°C$ to $+85°C$	Units
			Typ	Guaranteed Minimum	
$t_{W}(L)$	Minimum Pulse Width (CK)	3.3		6.0	7.0	ns
$t_{W}(H)$		5.0		5.0	5.0	
$t_{W}(L)$	Minimum Pulse Width ($\overline{CLR}$, $\overline{PR}$)	3.3		6.0	7.0	ns
		5.0		5.0	5.0	
t_S	Minimum Setup Time	3.3		6.0	7.0	ns
		5.0		5.0	5.0	
t_H	Minimum Hold Time	3.3		0.5	0.5	ns
		5.0		0.5	0.5	
t_{REC}	Minimum Recovery Time ($\overline{CLR}$, $\overline{PR}$)	3.3		5.0	5.0	ns
		5.0		3.0	3.0	

Note 6: V_{CC} is $3.3 \pm 0.3V$ or $5.0 \pm 0.5V$

Physical Dimensions inches (millimeters) unless otherwise noted

0.335 − 0.344
(8.509 − 8.738)

14 13 12 11 10 9 8

0.228 − 0.244
(5.791 − 6.198)

LEAD NO. 1
IDENT

30°
TYP

1 2 3 4 5 6 7

0.010 MAX
(0.254)

0.150 − 0.157
(3.810 − 3.988)

0.010 − 0.020
(0.254 − 0.508) ×45°

8° MAX TYP
ALL LEADS

0.008 − 0.010
(0.203 − 0.254)
TYP ALL LEADS

0.004
(0.102)
ALL LEAD TIPS

0.016 − 0.050
(0.406 − 1.270)
TYP ALL LEADS

0.053 − 0.069
(1.346 − 1.753)

0.004 − 0.010
(0.102 − 0.254)

SEATING
PLANE

0.014
(0.356)

0.050
(1.270)
TYP

0.008
(0.203) TYP

0.014 − 0.020 TYP
(0.356 − 0.508)

M14A (REV H)

14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow
Package Number M14A

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)

10.2±0.1

-A-

1.1 TYP

14   8

7.8

5.3±0.1

-B-

3.9

□ 0.2 C B A
ALL LEAD TIPS

PIN #1 IDENT.

1   7

LAND PATTERN RECOMMENDATION

14   13   9   8

5.01 TYP

9.27 TYP

(2.13 TYP)

1   2   6   7

1.27 TYP   0.6 TYP

ALL LEAD TIPS

2.1 MAX.

□ 0.1 C

1.8±0.1

-C-

0.15±0.05

1.27 TYP   0.35-0.51

⊕ 0.12 Ⓜ C A

DIMENSIONS ARE IN MILLIMETERS

SEE DETAIL A

0.15-0.25

7° TYP

GAGE PLANE

0°-8° TYP

0.25

0.60±0.15

1.25

SEATING PLANE

DETAIL A
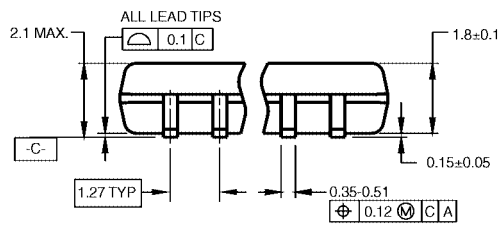
NOTES:
A. CONFORMS TO EIAJ EDR-7320 REGISTRATION, ESTABLISHED IN DECEMBER, 1998.
B. DIMENSIONS ARE IN MILLIMETERS.
C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.

M14DRevB1

Pb-Free 14-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
Package Number M14D

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)

LAND PATTERN RECOMMENDATION

DETAIL A
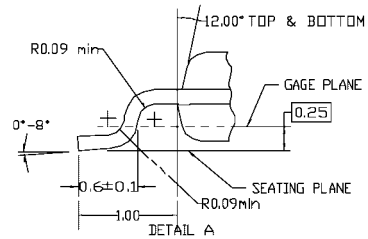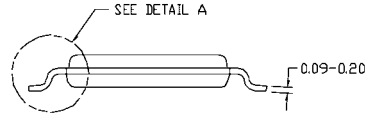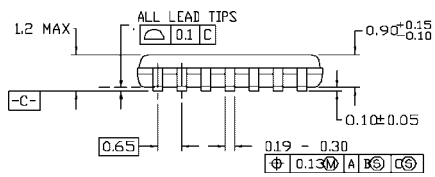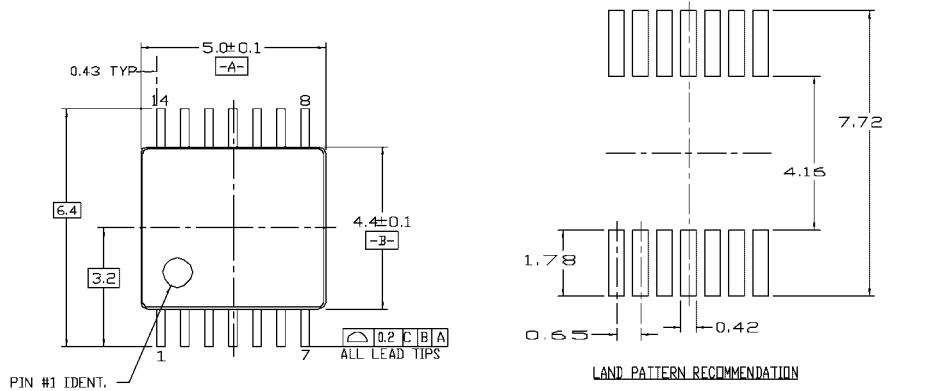
NOTES:

A. CONFORMS TO JEDEC REGISTRATION MO-153, VARIATION AB, REF NOTE 6, DATED 7/93

B. DIMENSIONS ARE IN MILLIMETERS

C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS

D. DIMENSIONING AND TOLERANCES PER ANSI Y14.5M, 1982

MTC14 rev D

14-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
Package Number MTC14

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)

OPTION 1

OPTION 02

14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide
Package Number N14A

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