

ULN200x, ULQ200x High-Voltage, High-Current Darlington Transistor Arrays

1 Features

- 500-mA-Rated Collector Current (Single Output)
- High-Voltage Outputs: 50 V
- Output Clamp Diodes
- Inputs Compatible With Various Types of Logic
- Relay-Driver Applications

2 Applications

- Relay Drivers
- Stepper and DC Brushed Motor Drivers
- Lamp Drivers
- Display Drivers (LED and Gas Discharge)
- Line Drivers
- Logic Buffers

3 Description

The ULx200xA devices are high-voltage, high-current Darlington transistor arrays. Each consists of seven NPN Darlington pairs that feature high-voltage outputs with common-cathode clamp diodes for switching inductive loads.

The collector-current rating of a single Darlington pair is 500 mA. The Darlington pairs can be paralleled for higher current capability. Applications include relay drivers, hammer drivers, lamp drivers, display drivers (LED and gas discharge), line drivers, and logic buffers. For 100-V (otherwise interchangeable) versions of the ULx2003A devices, see the [SLRS023](#) data sheet for the SN75468 and SN75469 devices.

The ULN2002A device is designed specifically for use with 14-V to 25-V PMOS devices. Each input of this device has a Zener diode and resistor in series to control the input current to a safe limit. The ULx2003A devices have a 2.7-k Ω series base resistor for each Darlington pair for operation directly with TTL or 5-V CMOS devices.

The ULx2004A devices have a 10.5-k Ω series base resistor to allow operation directly from CMOS devices that use supply voltages of 6 V to 15 V. The required input current of the ULx2004A device is below that of the ULx2003A devices, and the required voltage is less than that required by the ULN2002A device.

Device Information⁽¹⁾

| PART NUMBER | PACKAGE | BODY SIZE (NOM) |
|-------------|------------|--------------------|
| ULx200xD | SOIC (16) | 9.90 mm x 3.91 mm |
| ULx200xN | PDIP (16) | 19.30 mm x 6.35 mm |
| ULN200xNS | SOP (16) | 10.30 mm x 5.30 mm |
| ULN200xPW | TSSOP (16) | 5.00 mm x 4.40 mm |

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Simplified Block Diagram

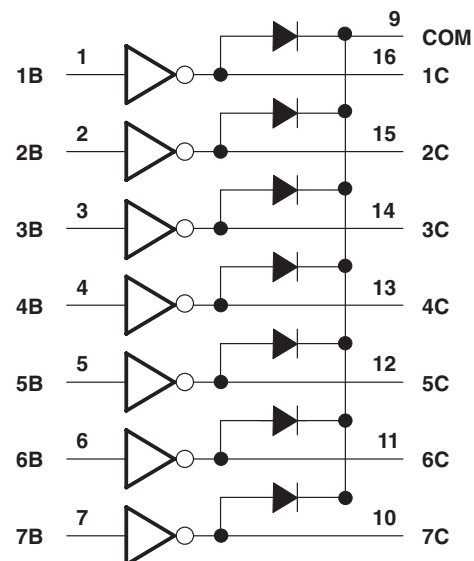


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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

| Changes from Revision N (June 2015) to Revision O | Page |
|--|-------------|
| • Changed Pin Functions table to correct typographical error. | 3 |

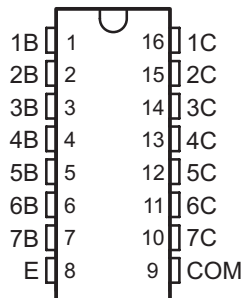
| Changes from Revision M (February 2013) to Revision N | Page |
|--|-------------|
| • Added <i>Pin Configuration and Functions</i> section, <i>ESD Ratings</i> table, <i>Feature Description</i> section, <i>Device Functional Modes</i> , <i>Application and Implementation</i> section, <i>Power Supply Recommendations</i> section, <i>Layout</i> section, <i>Device and Documentation Support</i> section, and <i>Mechanical, Packaging, and Orderable Information</i> section | 1 |
| • Deleted <i>Ordering Information</i> table. No specification changes. | 1 |
| • Moved <i>Typical Characteristics</i> into <i>Specifications</i> section. | 8 |

| Changes from Revision L (April 2012) to Revision M | Page |
|--|-------------|
| • Updated temperature rating for ULN2003AI in the ORDERING INFORMATION table | 1 |

| Changes from Revision K (August 2011) to Revision L | Page |
|--|-------------|
| • Removed reference to obsolete ULN2001 device | 1 |

5 Pin Configuration and Functions

**D, N, NS, and PW Package
16-Pin SOIC, PDIP, SO, and TSSOP
Top View**



Pin Functions

| PIN | | I/O ⁽¹⁾ | DESCRIPTION |
|------|-----|--------------------|---|
| NAME | NO. | | |
| 1B | 1 | I | Channel 1 through 7 Darlington base input |
| 2B | 2 | | |
| 3B | 3 | | |
| 4B | 4 | | |
| 5B | 5 | | |
| 6B | 6 | | |
| 7B | 7 | | |
| 1C | 16 | O | Channel 1 through 7 Darlington collector output |
| 2C | 15 | | |
| 3C | 14 | | |
| 4C | 13 | | |
| 5C | 12 | | |
| 6C | 11 | | |
| 7C | 10 | | |
| COM | 9 | — | Common cathode node for flyback diodes (required for inductive loads) |
| E | 8 | — | Common emitter shared by all channels (typically tied to ground) |

(1) I = Input, O = Output

6 Specifications

6.1 Absolute Maximum Ratings

at 25°C free-air temperature (unless otherwise noted)⁽¹⁾

| | | MIN | MAX | UNIT | |
|------------------|---|-----------|------|------|----|
| V _{CC} | Collector-emitter voltage | | 50 | V | |
| | Clamp diode reverse voltage ⁽²⁾ | | 50 | V | |
| V _I | Input voltage ⁽²⁾ | | 30 | V | |
| | Peak collector current, See Figure 4 and Figure 5 | | 500 | mA | |
| I _{OK} | Output clamp current | | 500 | mA | |
| | Total emitter-terminal current | | -2.5 | A | |
| T _A | Operating free-air temperature range | ULN200xA | -20 | 70 | °C |
| | | ULN200xAI | -40 | 105 | |
| | | ULQ200xA | -40 | 85 | |
| | | ULQ200xAT | -40 | 105 | |
| T _J | Operating virtual junction temperature | | 150 | °C | |
| | Lead temperature for 1.6 mm (1/16 inch) from case for 10 seconds | | 260 | °C | |
| T _{stg} | Storage temperature | -65 | 150 | °C | |

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltage values are with respect to the emitter/substrate terminal E, unless otherwise noted.

6.2 ESD Ratings

| | | | VALUE | UNIT |
|--------------------|-------------------------|--|-------|------|
| V _(ESD) | Electrostatic discharge | Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾ | ±2000 | V |
| | | Charged device model (CDM), per JEDEC specification JESD22-C101 ⁽²⁾ | ±500 | |

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

| | | MIN | MAX | UNIT |
|-----------------|---|-----|-----|------|
| V _{CC} | Collector-emitter voltage (non-V devices) | 0 | 50 | V |
| T _J | Junction temperature | -40 | 125 | °C |

6.4 Thermal Information

| THERMAL METRIC ⁽¹⁾ | ULx200x | | | | UNIT | |
|-------------------------------|--|----------|---------|------------|------|------|
| | D (SOIC) | N (PDIP) | NS (SO) | PW (TSSOP) | | |
| | 16 PINS | 16 PINS | 16 PINS | 16 PINS | | |
| R _{θJA} | Junction-to-ambient thermal resistance | 73 | 67 | 64 | 108 | °C/W |
| R _{θJC(top)} | Junction-to-case (top) thermal resistance | 36 | 54 | n/a | 33.6 | °C/W |
| R _{θJB} | Junction-to-board thermal resistance | n/a | n/a | n/a | 51.9 | °C/W |
| ψ _{JT} | Junction-to-top characterization parameter | n/a | n/a | n/a | 2.1 | °C/W |
| ψ _{JB} | Junction-to-board characterization parameter | n/a | n/a | n/a | 51.4 | °C/W |

- (1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, [SPRA953](#).

6.5 Electrical Characteristics: ULN2002A

 $T_A = 25^\circ\text{C}$

| PARAMETER | TEST FIGURE | TEST CONDITIONS | ULN2002A | | | UNIT |
|--|-------------|--|------------|------|------------|---------------|
| | | | MIN | TYP | MAX | |
| $V_{I(on)}$ ON-state input voltage | Figure 14 | $V_{CE} = 2\text{ V}$, $I_C = 300\text{ mA}$ | | | 13 | V |
| V_{OH} High-level output voltage after switching | Figure 18 | $V_S = 50\text{ V}$, $I_O = 300\text{ mA}$ | $V_S - 20$ | | | mV |
| $V_{CE(sat)}$ Collector-emitter saturation voltage | Figure 12 | $I_I = 250\ \mu\text{A}$, $I_C = 100\text{ mA}$ | | 0.9 | 1.1 | V |
| | | $I_I = 350\ \mu\text{A}$, $I_C = 200\text{ mA}$ | | 1 | 1.3 | |
| | | $I_I = 500\ \mu\text{A}$, $I_C = 350\text{ mA}$ | | 1.2 | 1.6 | |
| V_F Clamp forward voltage | Figure 15 | $I_F = 350\text{ mA}$ | | 1.7 | 2 | V |
| I_{CEX} Collector cutoff current | Figure 9 | $V_{CE} = 50\text{ V}$, $I_I = 0$ | | | 50 | μA |
| | Figure 10 | $V_{CE} = 50\text{ V}$, $T_A = 70^\circ\text{C}$, $V_I = 6\text{ V}$ | | | 100 500 | |
| $I_{I(off)}$ OFF-state input current | Figure 10 | $V_{CE} = 50\text{ V}$, $I_C = 500\ \mu\text{A}$ | 50 | 65 | | μA |
| I_I Input current | Figure 11 | $V_I = 17\text{ V}$ | | 0.82 | 1.25 | mA |
| I_R Clamp reverse current | Figure 14 | $V_R = 50\text{ V}$, $T_A = 70^\circ\text{C}$ | | | 100 | μA |
| | | $V_R = 50\text{ V}$ | | | 50 | |
| C_i Input capacitance | | $V_I = 0$, $f = 1\text{ MHz}$ | | | 25 | pF |

6.6 Electrical Characteristics: ULN2003A and ULN2004A

 $T_A = 25^\circ\text{C}$

| PARAMETER | TEST FIGURE | TEST CONDITIONS | ULN2003A | | | ULN2004A | | | UNIT |
|--|-------------|--|-----------------------|------|------|------------|------------|---------------|------|
| | | | MIN | TYP | MAX | MIN | TYP | MAX | |
| $V_{I(on)}$ ON-state input voltage | Figure 14 | $V_{CE} = 2\text{ V}$ | $I_C = 125\text{ mA}$ | | | | | 5 | V |
| | | | $I_C = 200\text{ mA}$ | | | 2.4 | | 6 | |
| | | | $I_C = 250\text{ mA}$ | | | 2.7 | | | |
| | | | $I_C = 275\text{ mA}$ | | | | | 7 | |
| | | | $I_C = 300\text{ mA}$ | | | 3 | | | |
| | | | $I_C = 350\text{ mA}$ | | | | | 8 | |
| V_{OH} High-level output voltage after switching | Figure 18 | $V_S = 50\text{ V}$, $I_O = 300\text{ mA}$ | $V_S - 20$ | | | $V_S - 20$ | | | mV |
| $V_{CE(sat)}$ Collector-emitter saturation voltage | Figure 13 | $I_I = 250\ \mu\text{A}$, $I_C = 100\text{ mA}$ | | 0.9 | 1.1 | 0.9 | 1.1 | V | |
| | | $I_I = 350\ \mu\text{A}$, $I_C = 200\text{ mA}$ | | 1 | 1.3 | 1 | 1.3 | | |
| | | $I_I = 500\ \mu\text{A}$, $I_C = 350\text{ mA}$ | | 1.2 | 1.6 | 1.2 | 1.6 | | |
| I_{CEX} Collector cutoff current | Figure 9 | $V_{CE} = 50\text{ V}$, $I_I = 0$ | | | 50 | | 50 | μA | |
| | Figure 10 | $V_{CE} = 50\text{ V}$, $T_A = 70^\circ\text{C}$, $V_I = 6\text{ V}$ | | | 100 | | 100 500 | | |
| V_F Clamp forward voltage | Figure 16 | $I_F = 350\text{ mA}$ | | 1.7 | 2 | | 1.7 | 2 | V |
| $I_{I(off)}$ Off-state input current | Figure 11 | $V_{CE} = 50\text{ V}$, $T_A = 70^\circ\text{C}$, $I_C = 500\ \mu\text{A}$ | 50 | 65 | | 50 | 65 | μA | |
| I_I Input current | Figure 12 | $V_I = 3.85\text{ V}$ | | 0.93 | 1.35 | | | mA | |
| | | $V_I = 5\text{ V}$ | | | | 0.35 | 0.5 | | |
| | | $V_I = 12\text{ V}$ | | | | 1 | 1.45 | | |
| I_R Clamp reverse current | Figure 15 | $V_R = 50\text{ V}$ | | | 50 | | 50 | μA | |
| | | $V_R = 50\text{ V}$, $T_A = 70^\circ\text{C}$ | | | 100 | | 100 | | |
| C_i Input capacitance | | $V_I = 0$, $f = 1\text{ MHz}$ | | 15 | 25 | | 15 | 25 | pF |

6.7 Electrical Characteristics: ULN2003AI

T_A = 25°C

| PARAMETER | TEST FIGURE | TEST CONDITIONS | ULN2003AI | | | UNIT |
|---|-------------|--|-------------------------|------|-----|------|
| | | | MIN | TYP | MAX | |
| V _{I(on)} ON-state input voltage | Figure 14 | V _{CE} = 2 V | I _C = 200 mA | | 2.4 | V |
| | | | I _C = 250 mA | | 2.7 | |
| | | | I _C = 300 mA | | 3 | |
| V _{OH} High-level output voltage after switching | Figure 18 | V _S = 50 V, I _O = 300 mA | V _S – 50 | | | mV |
| V _{CE(sat)} Collector-emitter saturation voltage | Figure 13 | I _I = 250 μA, I _C = 100 mA | 0.9 | 1.1 | V | |
| | | I _I = 350 μA, I _C = 200 mA | 1 | 1.3 | | |
| | | I _I = 500 μA, I _C = 350 mA | 1.2 | 1.6 | | |
| I _{CEX} Collector cutoff current | Figure 9 | V _{CE} = 50 V, I _I = 0 | | 50 | μA | |
| V _F Clamp forward voltage | Figure 16 | I _F = 350 mA | 1.7 | 2 | V | |
| I _{I(off)} OFF-state input current | Figure 11 | V _{CE} = 50 V, I _C = 500 μA | 50 | 65 | μA | |
| I _I Input current | Figure 12 | V _I = 3.85 V | 0.93 | 1.35 | mA | |
| I _R Clamp reverse current | Figure 15 | V _R = 50 V | | 50 | μA | |
| C _i Input capacitance | | V _I = 0, f = 1 MHz | 15 | 25 | pF | |

6.8 Electrical Characteristics: ULN2003AI

T_A = –40°C to 105°C

| PARAMETER | TEST FIGURE | TEST CONDITIONS | ULN2003AI | | | UNIT |
|---|-------------|--|-------------------------|------|-----|------|
| | | | MIN | TYP | MAX | |
| V _{I(on)} ON-state input voltage | Figure 14 | V _{CE} = 2 V | I _C = 200 mA | | 2.7 | V |
| | | | I _C = 250 mA | | 2.9 | |
| | | | I _C = 300 mA | | 3 | |
| V _{OH} High-level output voltage after switching | Figure 18 | V _S = 50 V, I _O = 300 mA | V _S – 50 | | | mV |
| V _{CE(sat)} Collector-emitter saturation voltage | Figure 13 | I _I = 250 μA, I _C = 100 mA | 0.9 | 1.2 | V | |
| | | I _I = 350 μA, I _C = 200 mA | 1 | 1.4 | | |
| | | I _I = 500 μA, I _C = 350 mA | 1.2 | 1.7 | | |
| I _{CEX} Collector cutoff current | Figure 9 | V _{CE} = 50 V, I _I = 0 | | 100 | μA | |
| V _F Clamp forward voltage | Figure 16 | I _F = 350 mA | 1.7 | 2.2 | V | |
| I _{I(off)} OFF-state input current | Figure 11 | V _{CE} = 50 V, I _C = 500 μA | 30 | 65 | μA | |
| I _I Input current | Figure 12 | V _I = 3.85 V | 0.93 | 1.35 | mA | |
| I _R Clamp reverse current | Figure 15 | V _R = 50 V | | 100 | μA | |
| C _i Input capacitance | | V _I = 0, f = 1 MHz | 15 | 25 | pF | |

6.9 Electrical Characteristics: ULQ2003A and ULQ2004A

over recommended operating conditions (unless otherwise noted)

| PARAMETER | TEST FIGURE | TEST CONDITIONS | | ULQ2003A | | | ULQ2004A | | | UNIT | |
|--|-------------|--|-----------------------|------------|------|-----|------------|------|---------------|---------------|---|
| | | | | MIN | TYP | MAX | MIN | TYP | MAX | | |
| $V_{I(on)}$ ON-state input voltage | Figure 14 | $V_{CE} = 2\text{ V}$ | $I_C = 125\text{ mA}$ | | | | | | 5 | V | |
| | | | $I_C = 200\text{ mA}$ | | | 2.7 | | | 6 | | |
| | | | $I_C = 250\text{ mA}$ | | | 2.9 | | | | | |
| | | | $I_C = 275\text{ mA}$ | | | | | | 7 | | |
| | | | $I_C = 300\text{ mA}$ | | | | | 3 | | | |
| | | | $I_C = 350\text{ mA}$ | | | | | | | | 8 |
| V_{OH} High-level output voltage after switching | Figure 18 | $V_S = 50\text{ V}, I_O = 300\text{ mA}$ | | $V_S - 50$ | | | $V_S - 50$ | | | mV | |
| $V_{CE(sat)}$ Collector-emitter saturation voltage | Figure 13 | $I_I = 250\text{ }\mu\text{A}, I_C = 100\text{ mA}$ | | 0.9 | 1.2 | | 0.9 | 1.1 | V | | |
| | | $I_I = 350\text{ }\mu\text{A}, I_C = 200\text{ mA}$ | | 1 | 1.4 | | 1 | 1.3 | | | |
| | | $I_I = 500\text{ }\mu\text{A}, I_C = 350\text{ mA}$ | | 1.2 | 1.7 | | 1.2 | 1.6 | | | |
| I_{CEX} Collector cutoff current | Figure 9 | $V_{CE} = 50\text{ V}, I_I = 0$ | | 100 | | | 50 | | | μA | |
| | Figure 10 | $V_{CE} = 50\text{ V}, T_A = 70^\circ\text{C}$ | | | | | 100 | | | | |
| | | $V_I = 6\text{ V}$ | | | | | 500 | | | | |
| V_F Clamp forward voltage | Figure 16 | $I_F = 350\text{ mA}$ | | 1.7 | 2.3 | | 1.7 | 2 | V | | |
| $I_{I(off)}$ OFF-state input current | Figure 11 | $V_{CE} = 50\text{ V}, T_A = 70^\circ\text{C}, I_C = 500\text{ }\mu\text{A}$ | | 65 | | | 50 | 65 | μA | | |
| I_I Input current | Figure 12 | $V_I = 3.85\text{ V}$ | | 0.93 | 1.35 | | | | mA | | |
| | | $V_I = 5\text{ V}$ | | | | | 0.35 | 0.5 | | | |
| | | $V_I = 12\text{ V}$ | | | | | 1 | 1.45 | | | |
| I_R Clamp reverse current | Figure 15 | $V_R = 50\text{ V}, T_A = 25^\circ\text{C}$ | | 100 | | | 50 | | | μA | |
| | | $V_R = 50\text{ V}$ | | 100 | | | 100 | | | | |
| C_i Input capacitance | | $V_I = 0, f = 1\text{ MHz}$ | | 15 | 25 | | 15 | 25 | pF | | |

6.10 Switching Characteristics: ULN2002A, ULN2003A, ULN2004A

 $T_A = 25^\circ\text{C}$

| PARAMETER | TEST CONDITIONS | ULN2002A, ULN2003A, ULN2004A | | | UNIT |
|---|-----------------|------------------------------|------|-----|---------------|
| | | MIN | TYP | MAX | |
| t_{PLH} Propagation delay time, low- to high-level output | See Figure 17 | | 0.25 | 1 | μs |
| t_{PHL} Propagation delay time, high- to low-level output | See Figure 17 | | 0.25 | 1 | μs |

6.11 Switching Characteristics: ULN2003AI

 $T_A = 25^\circ\text{C}$

| PARAMETER | TEST CONDITIONS | ULN2003AI | | | UNIT |
|---|-----------------|-----------|------|-----|---------------|
| | | MIN | TYP | MAX | |
| t_{PLH} Propagation delay time, low- to high-level output | See Figure 17 | | 0.25 | 1 | μs |
| t_{PHL} Propagation delay time, high- to low-level output | See Figure 17 | | 0.25 | 1 | μs |

6.12 Switching Characteristics: ULN2003AI

$T_A = -40^{\circ}\text{C}$ to 105°C

| PARAMETER | TEST CONDITIONS | ULN2003AI | | | UNIT |
|-----------|---|-----------|-----|-----|---------------|
| | | MIN | TYP | MAX | |
| t_{PLH} | Propagation delay time, low- to high-level output | | 1 | 10 | μs |
| t_{PHL} | Propagation delay time, high- to low-level output | | 1 | 10 | μs |

6.13 Switching Characteristics: ULQ2003A, ULQ2004A

over recommended operating conditions (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | ULQ2003A, ULQ2004A | | | UNIT |
|-----------|---|--------------------|-----|-----|---------------|
| | | MIN | TYP | MAX | |
| t_{PLH} | Propagation delay time, low- to high-level output | | 1 | 10 | μs |
| t_{PHL} | Propagation delay time, high- to low-level output | | 1 | 10 | μs |

6.14 Typical Characteristics

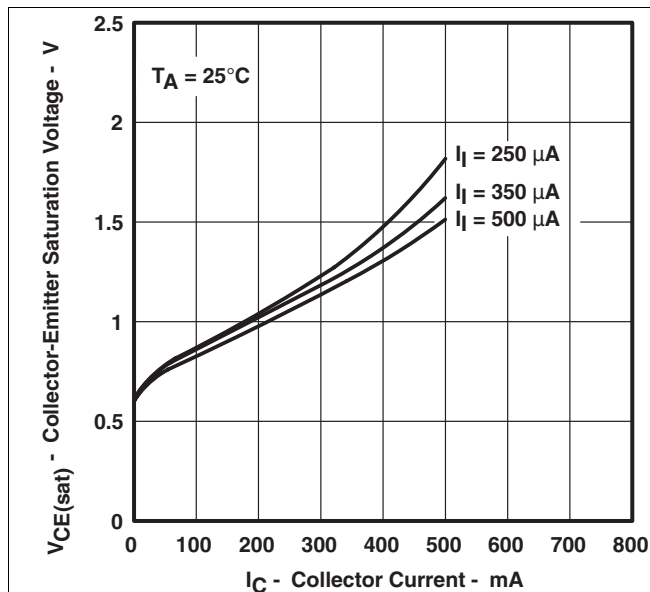


Figure 1. Collector-Emitter Saturation Voltage vs Collector Current (One Darlington)

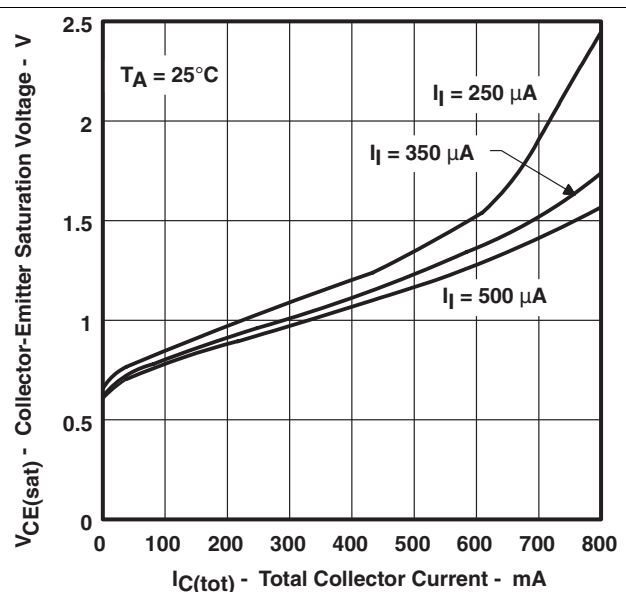


Figure 2. Collector-Emitter Saturation Voltage vs Total Collector Current (Two Darlings in Parallel)

Typical Characteristics (continued)



Figure 3. Collector Current vs Input Current

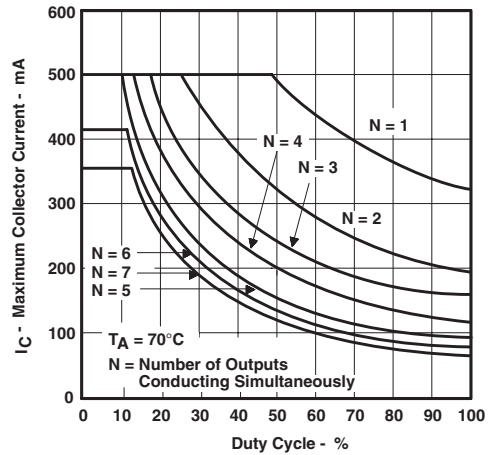


Figure 4. D Package Maximum Collector Current vs Duty Cycle

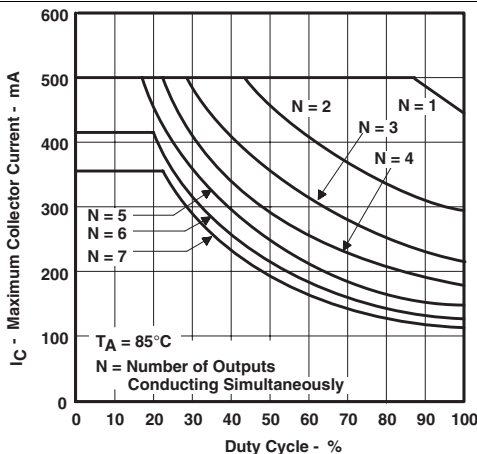


Figure 5. N Package Maximum Collector Current vs Duty Cycle

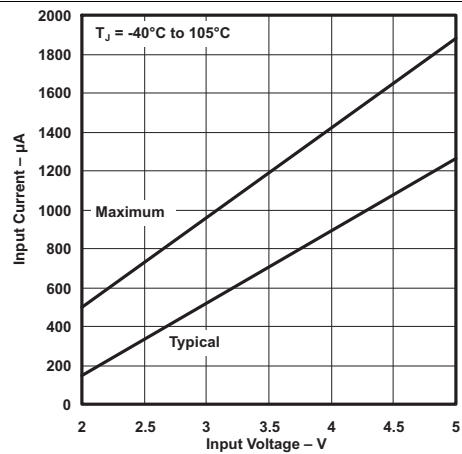


Figure 6. Maximum and Typical Input Current vs Input Voltage

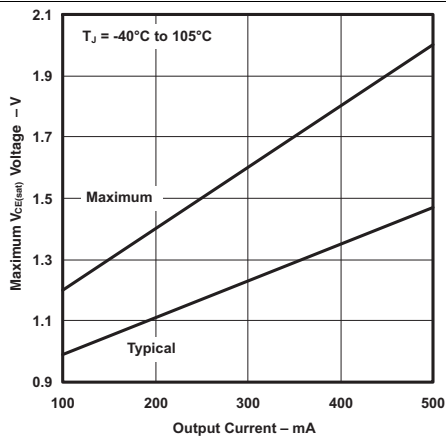


Figure 7. Maximum and Typical Saturated V_{CE} vs Output Current

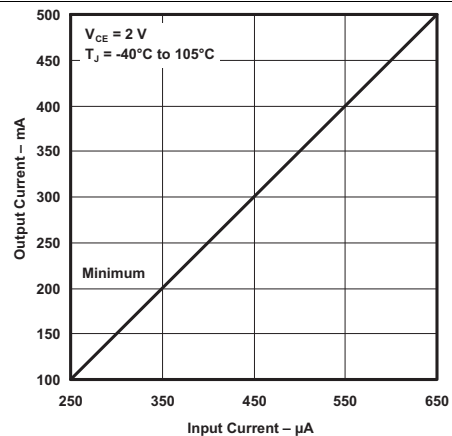


Figure 8. Minimum Output Current vs Input Current

7 Parameter Measurement Information

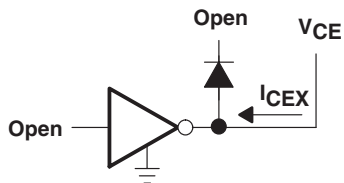


Figure 9. I_{CEX} Test Circuit

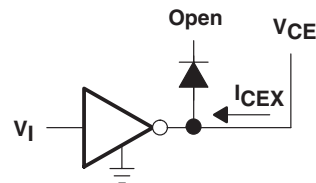


Figure 10. I_{CEX} Test Circuit

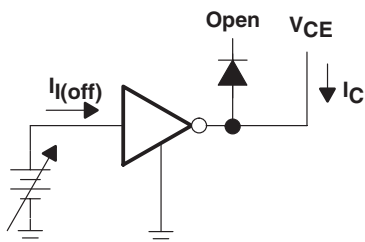


Figure 11. $I_{I(off)}$ Test Circuit

I_I is fixed for measuring $V_{CE(sat)}$, variable for measuring h_{FE} .

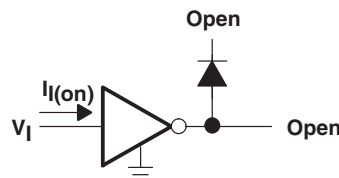


Figure 12. I_I Test Circuit

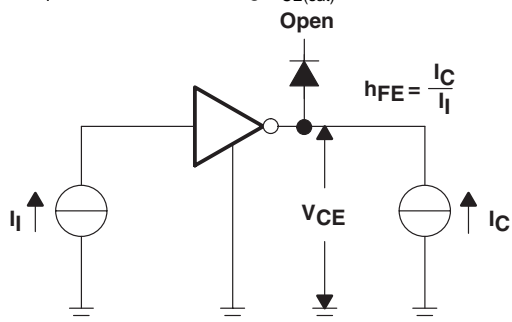


Figure 13. h_{FE} , $V_{CE(sat)}$ Test Circuit

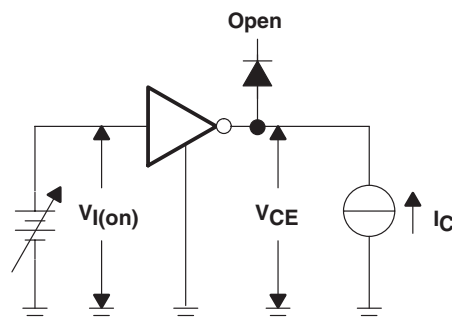


Figure 14. $V_{I(on)}$ Test Circuit

Parameter Measurement Information (continued)

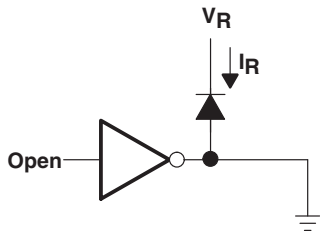


Figure 15. I_R Test Circuit

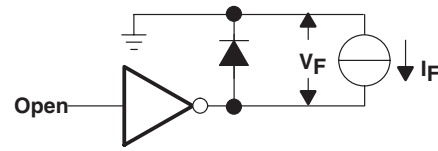


Figure 16. V_F Test Circuit

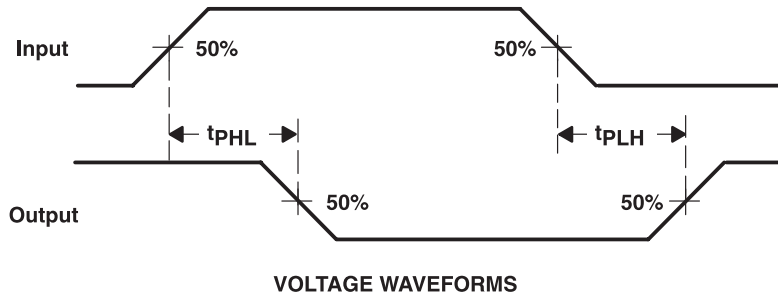
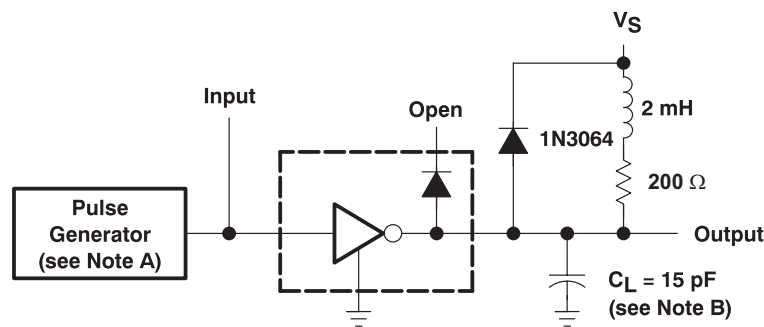
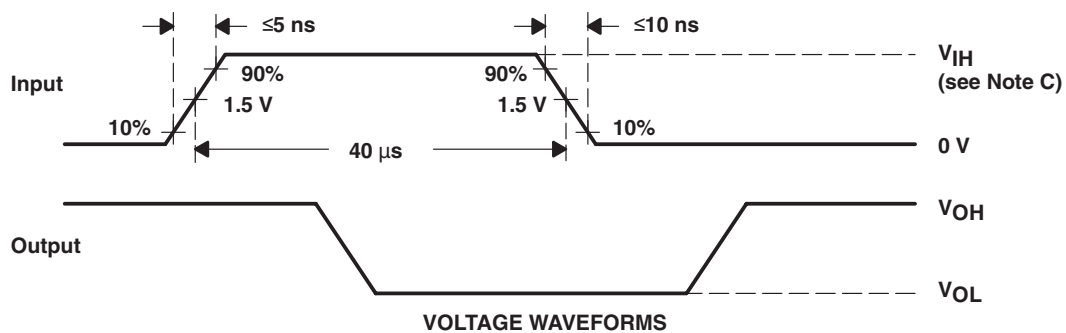


Figure 17. Propagation Delay-Time Waveforms



TEST CIRCUIT



VOLTAGE WAVEFORMS

The pulse generator has the following characteristics: PRR = 12.5 kHz, $Z_O = 50 \Omega$.

C_L includes probe and jig capacitance.

For testing the ULN2003A device, ULN2003AI device, and ULQ2003A devices, $V_{IH} = 3 \text{ V}$; for the ULN2002A device, $V_{IH} = 13 \text{ V}$; for the ULN2004A and the ULQ2004A devices, $V_{IH} = 8 \text{ V}$.

Figure 18. Latch-Up Test Circuit and Voltage Waveforms

8 Detailed Description

8.1 Overview

This standard device has proven ubiquity and versatility across a wide range of applications. This is due to integration of 7 Darlington transistors of the device that are capable of sinking up to 500 mA and wide GPIO range capability.

The ULN2003A device comprises seven high-voltage, high-current NPN Darlington transistor pairs. All units feature a common emitter and open collector outputs. To maximize their effectiveness, these units contain suppression diodes for inductive loads. The ULN2003A device has a series base resistor to each Darlington pair, thus allowing operation directly with TTL or CMOS operating at supply voltages of 5 V or 3.3 V. The ULN2003A device offers solutions to a great many interface needs, including solenoids, relays, lamps, small motors, and LEDs. Applications requiring sink currents beyond the capability of a single output may be accommodated by paralleling the outputs.

This device can operate over a wide temperature range (–40°C to 105°C).

8.2 Functional Block Diagrams

All resistor values shown are nominal. The collector-emitter diode is a parasitic structure and should not be used to conduct current. If the collectors go below GND, an external Schottky diode should be added to clamp negative undershoots.

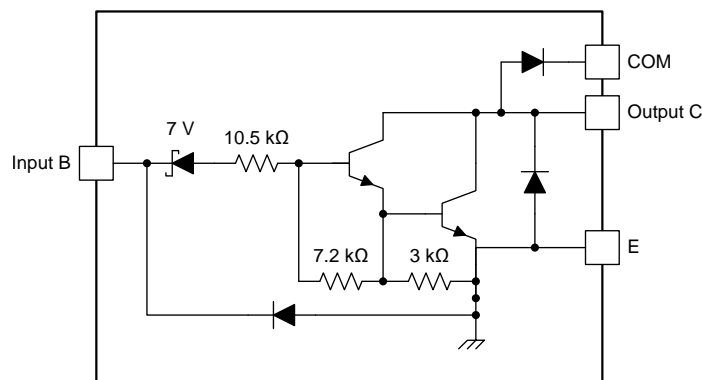


Figure 19. ULN2002A Block Diagram

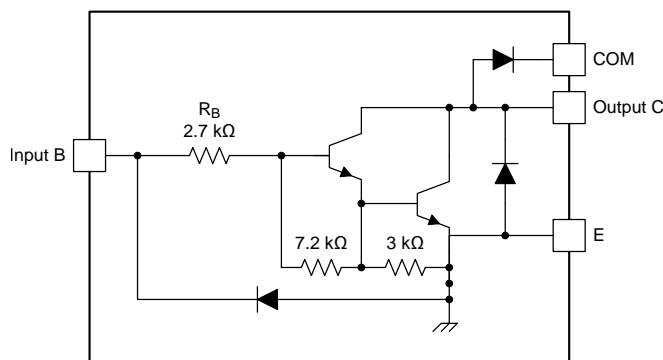


Figure 20. ULN2003A, ULQ2003A and ULN2003AI Block Diagram

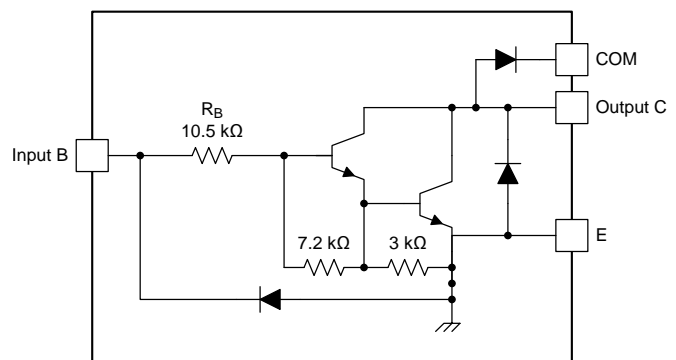


Figure 21. ULN2004A and LQ2004A Block Diagram

8.3 Feature Description

Each channel of the ULN2003A device consists of Darlington connected NPN transistors. This connection creates the effect of a single transistor with a very high-current gain (β^2). This can be as high as 10,000 A/A at certain currents. The very high β allows for high-output current drive with a very low input current, essentially equating to operation with low GPIO voltages.

The GPIO voltage is converted to base current through the 2.7-k Ω resistor connected between the input and base of the predriver Darlington NPN. The 7.2-k Ω and 3-k Ω resistors connected between the base and emitter of each respective NPN act as pulldowns and suppress the amount of leakage that may occur from the input.

The diodes connected between the output and COM pin is used to suppress the kick-back voltage from an inductive load that is excited when the NPN drivers are turned off (stop sinking) and the stored energy in the coils causes a reverse current to flow into the coil supply through the kick-back diode.

In normal operation the diodes on base and collector pins to emitter will be reversed biased. If these diodes are forward biased, internal parasitic NPN transistors will draw (a nearly equal) current from other (nearby) device pins.

8.4 Device Functional Modes

8.4.1 Inductive Load Drive

When the COM pin is tied to the coil supply voltage, ULN2003A device is able to drive inductive loads and suppress the kick-back voltage through the internal free-wheeling diodes.

8.4.2 Resistive Load Drive

When driving a resistive load, a pullup resistor is needed in order for ULN2003A device to sink current and for there to be a logic high level. The COM pin can be left floating for these applications.

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

Typically, the ULN2003A device drives a high-voltage or high-current (or both) peripheral from an MCU or logic device that cannot tolerate these conditions. This design is a common application of ULN2003A device, driving inductive loads. This includes motors, solenoids and relays. [Figure 22](#) shows a model for each load type.

9.2 Typical Application



Figure 22. ULN2003A Device as Inductive Load Driver

9.2.1 Design Requirements

For this design example, use the parameters listed in [Table 1](#) as the input parameters.

Table 1. Design Parameters

| DESIGN PARAMETER | EXAMPLE VALUE |
|-------------------------------|-----------------------------|
| GPIO voltage | 3.3 V or 5 V |
| Coil supply voltage | 12 V to 48 V |
| Number of channels | 7 |
| Output current (R_{COIL}) | 20 mA to 300 mA per channel |
| Duty cycle | 100% |

9.2.2 Detailed Design Procedure

When using ULN2003A device in a coil driving application, determine the following:

- Input voltage range
- Temperature range
- Output and drive current
- Power dissipation

9.2.2.1 Drive Current

The coil voltage (V_{SUP}), coil resistance (R_{COIL}), and low-level output voltage ($V_{CE(SAT)}$ or V_{OL}) determine the coil current.

$$I_{COIL} = (V_{SUP} - V_{CE(SAT)}) / R_{COIL} \quad (1)$$

9.2.2.2 Low-Level Output Voltage

The low-level output voltage (V_{OL}) is the same as $V_{CE(SAT)}$ and can be determined by, [Figure 1](#), [Figure 2](#), or [Figure 7](#).

9.2.2.3 Power Dissipation and Temperature

The number of coils driven is dependent on the coil current and on-chip power dissipation. The number of coils driven can be determined by [Figure 4](#) or [Figure 5](#).

For a more accurate determination of number of coils possible, use the below equation to calculate ULN2003A device on-chip power dissipation P_D :

$$P_D = \sum_{i=1}^N V_{OLi} \times I_{Li}$$

where

- N is the number of channels active together
- V_{OLi} is the OUT_i pin voltage for the load current I_{Li} . This is the same as $V_{CE(SAT)}$ (2)

To ensure reliability of ULN2003A device and the system, the on-chip power dissipation must be lower than or equal to the maximum allowable power dissipation ($PD_{(MAX)}$) dictated by below equation [Equation 3](#).

$$PD_{(MAX)} = \frac{(T_{J(MAX)} - T_A)}{\theta_{JA}}$$

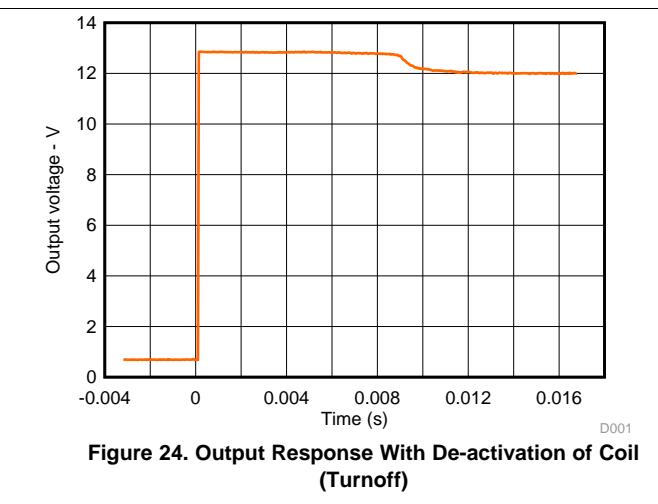
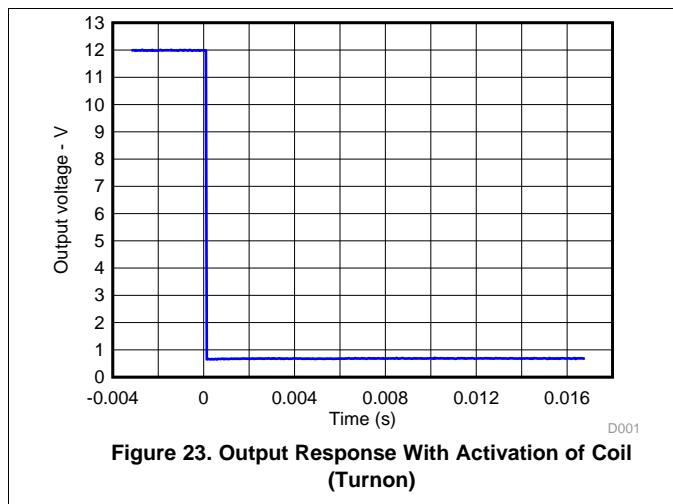
where

- $T_{J(max)}$ is the target maximum junction temperature
- T_A is the operating ambient temperature
- $R_{\theta JA}$ is the package junction to ambient thermal resistance (3)

Limit the die junction temperature of the ULN2003A device to less than 125°C. The IC junction temperature is directly proportional to the on-chip power dissipation.

9.2.3 Application Curves

The characterization data shown in [Figure 23](#) and [Figure 24](#) were generated using the ULN2003A device driving an OMRON G5NB relay and under the following conditions: $V_{IN} = 5\text{ V}$, $V_{SUP} = 12\text{ V}$, and $R_{COIL} = 2.8\text{ k}\Omega$.



9.3 System Examples



Figure 25. P-MOS to Load

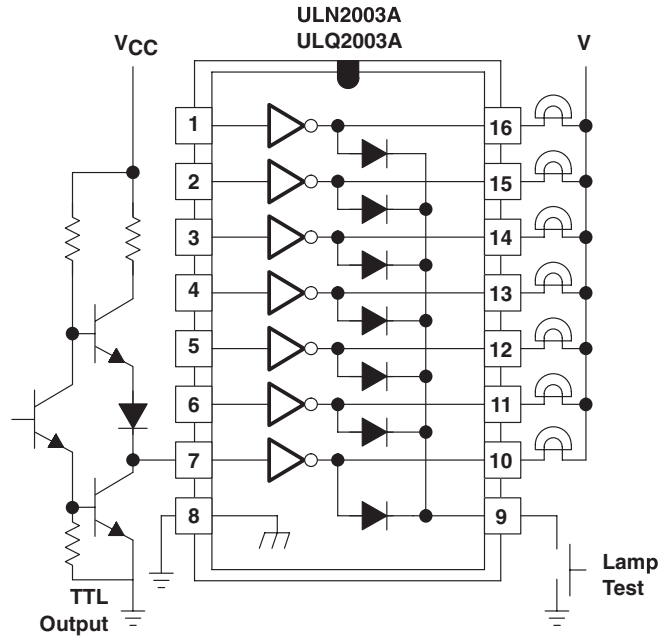


Figure 26. TTL to Load



Figure 27. Buffer for Higher Current Loads

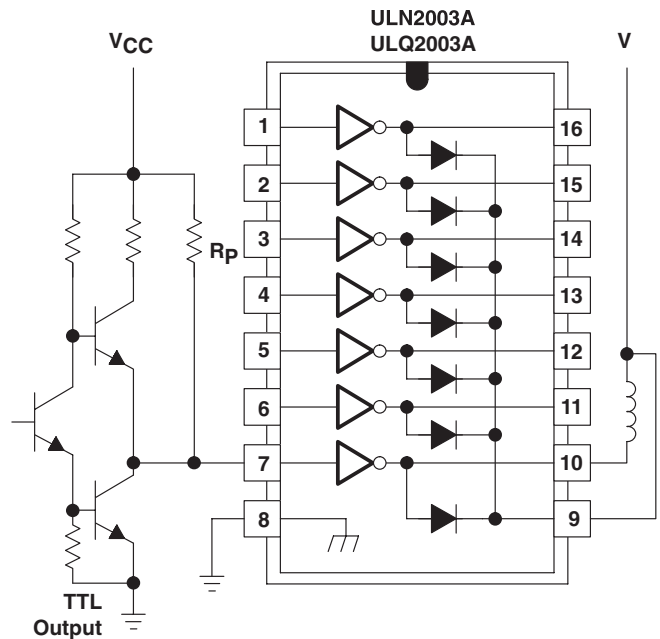


Figure 28. Use of Pullup Resistors to Increase Drive Current

10 Power Supply Recommendations

This device does not need a power supply. However, the COM pin is typically tied to the system power supply. When this is the case, it is very important to ensure that the output voltage does not heavily exceed the COM pin voltage. This discrepancy heavily forward biases the fly-back diodes and causes a large current to flow into COM, potentially damaging the on-chip metal or over-heating the device.

11 Layout

11.1 Layout Guidelines

Thin traces can be used on the input due to the low-current logic that is typically used to drive ULN2003A device. Take care to separate the input channels as much as possible, as to eliminate crosstalk. TI recommends thick traces for the output to drive whatever high currents that may be needed. Wire thickness can be determined by the current density of the trace material and desired drive current.

Because all of the channels currents return to a common emitter, it is best to size that trace width to be very wide. Some applications require up to 2.5 A.

11.2 Layout Example



Figure 29. Package Layout

12 Device and Documentation Support

12.1 Documentation Support

12.1.1 Related Documentation

For related documentation, see the following:

SN7546x Darlington Transistor Arrays, [SLRS023](#)

12.2 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 2. Related Links

| PARTS | PRODUCT FOLDER | SAMPLE & BUY | TECHNICAL DOCUMENTS | TOOLS & SOFTWARE | SUPPORT & COMMUNITY |
|-----------|----------------------------|----------------------------|----------------------------|----------------------------|----------------------------|
| ULN2002A | Click here | Click here | Click here | Click here | Click here |
| ULN2003A | Click here | Click here | Click here | Click here | Click here |
| ULN2003AI | Click here | Click here | Click here | Click here | Click here |
| ULN2004A | Click here | Click here | Click here | Click here | Click here |
| ULQ2003A | Click here | Click here | Click here | Click here | Click here |
| ULQ2004A | Click here | Click here | Click here | Click here | Click here |

12.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

TI E2E™ Online Community *TI's Engineer-to-Engineer (E2E) Community*. Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.4 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

12.5 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.6 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser based versions of this data sheet, refer to the left hand navigation.

PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|------------------|---------------|--------------|-----------------|------|-------------|-------------------------|-------------------------|----------------------|--------------|-------------------------|-------------------------|
| ULN2002AN | ACTIVE | PDIP | N | 16 | 25 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type | -20 to 70 | ULN2002AN | Samples |
| ULN2002ANE4 | ACTIVE | PDIP | N | 16 | 25 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type | -20 to 70 | ULN2002AN | Samples |
| ULN2003AD | ACTIVE | SOIC | D | 16 | 40 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -20 to 70 | ULN2003A | Samples |
| ULN2003ADE4 | ACTIVE | SOIC | D | 16 | 40 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -20 to 70 | ULN2003A | Samples |
| ULN2003ADG4 | ACTIVE | SOIC | D | 16 | 40 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -20 to 70 | ULN2003A | Samples |
| ULN2003ADR | ACTIVE | SOIC | D | 16 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU CU SN | Level-1-260C-UNLIM | -20 to 70 | ULN2003A | Samples |
| ULN2003ADRE4 | ACTIVE | SOIC | D | 16 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -20 to 70 | ULN2003A | Samples |
| ULN2003ADRG3 | ACTIVE | SOIC | D | 16 | 2500 | Green (RoHS & no Sb/Br) | CU SN | Level-1-260C-UNLIM | -20 to 70 | ULN2003A | Samples |
| ULN2003ADRG4 | ACTIVE | SOIC | D | 16 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -20 to 70 | ULN2003A | Samples |
| ULN2003AID | ACTIVE | SOIC | D | 16 | 40 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 105 | ULN2003AI | Samples |
| ULN2003AIDE4 | ACTIVE | SOIC | D | 16 | 40 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 105 | ULN2003AI | Samples |
| ULN2003AIDG4 | ACTIVE | SOIC | D | 16 | 40 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 105 | ULN2003AI | Samples |
| ULN2003AIDR | ACTIVE | SOIC | D | 16 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU CU SN | Level-1-260C-UNLIM | -40 to 105 | ULN2003AI | Samples |
| ULN2003AIDRE4 | ACTIVE | SOIC | D | 16 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 105 | ULN2003AI | Samples |
| ULN2003AIDRG4 | ACTIVE | SOIC | D | 16 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 105 | ULN2003AI | Samples |
| ULN2003AIN | ACTIVE | PDIP | N | 16 | 25 | Pb-Free (RoHS) | CU NIPDAU CU SN | N / A for Pkg Type | -40 to 105 | ULN2003AIN | Samples |
| ULN2003AINE4 | ACTIVE | PDIP | N | 16 | 25 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type | -40 to 105 | ULN2003AIN | Samples |

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|------------------|---------------|--------------|-----------------|------|-------------|-------------------------|-------------------------|----------------------|--------------|-------------------------|-------------------------|
| ULN2003AINSR | ACTIVE | SO | NS | 16 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 105 | ULN2003AI | Samples |
| ULN2003AIPW | ACTIVE | TSSOP | PW | 16 | 90 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 105 | UN2003AI | Samples |
| ULN2003AIPWE4 | ACTIVE | TSSOP | PW | 16 | 90 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 105 | UN2003AI | Samples |
| ULN2003AIPWG4 | ACTIVE | TSSOP | PW | 16 | 90 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 105 | UN2003AI | Samples |
| ULN2003AIPWR | ACTIVE | TSSOP | PW | 16 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU CU SN | Level-1-260C-UNLIM | -40 to 105 | UN2003AI | Samples |
| ULN2003AIPWRG4 | ACTIVE | TSSOP | PW | 16 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 105 | UN2003AI | Samples |
| ULN2003AN | ACTIVE | PDIP | N | 16 | 25 | Pb-Free (RoHS) | CU NIPDAU CU SN | N / A for Pkg Type | -20 to 70 | ULN2003AN | Samples |
| ULN2003ANE4 | ACTIVE | PDIP | N | 16 | 25 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type | -20 to 70 | ULN2003AN | Samples |
| ULN2003ANSR | ACTIVE | SO | NS | 16 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -20 to 70 | ULN2003A | Samples |
| ULN2003ANSRE4 | ACTIVE | SO | NS | 16 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -20 to 70 | ULN2003A | Samples |
| ULN2003ANSRG4 | ACTIVE | SO | NS | 16 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -20 to 70 | ULN2003A | Samples |
| ULN2003APW | ACTIVE | TSSOP | PW | 16 | 90 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -20 to 70 | UN2003A | Samples |
| ULN2003APWG4 | ACTIVE | TSSOP | PW | 16 | 90 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -20 to 70 | UN2003A | Samples |
| ULN2003APWR | ACTIVE | TSSOP | PW | 16 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU CU SN | Level-1-260C-UNLIM | -20 to 70 | UN2003A | Samples |
| ULN2003APWRG4 | ACTIVE | TSSOP | PW | 16 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -20 to 70 | UN2003A | Samples |
| ULN2004AD | ACTIVE | SOIC | D | 16 | 40 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -20 to 70 | ULN2004A | Samples |
| ULN2004ADE4 | ACTIVE | SOIC | D | 16 | 40 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -20 to 70 | ULN2004A | Samples |
| ULN2004ADG4 | ACTIVE | SOIC | D | 16 | 40 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -20 to 70 | ULN2004A | Samples |

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|------------------|---------------|--------------|-----------------|------|-------------|-------------------------|-------------------------|----------------------|--------------|-------------------------|-------------------------|
| ULN2004ADR | ACTIVE | SOIC | D | 16 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU CU SN | Level-1-260C-UNLIM | -20 to 70 | ULN2004A | Samples |
| ULN2004ADRE4 | ACTIVE | SOIC | D | 16 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -20 to 70 | ULN2004A | Samples |
| ULN2004ADRG4 | ACTIVE | SOIC | D | 16 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -20 to 70 | ULN2004A | Samples |
| ULN2004AN | ACTIVE | PDIP | N | 16 | 25 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type | -20 to 70 | ULN2004AN | Samples |
| ULN2004ANE4 | ACTIVE | PDIP | N | 16 | 25 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type | -20 to 70 | ULN2004AN | Samples |
| ULN2004ANSR | ACTIVE | SO | NS | 16 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -20 to 70 | ULN2004A | Samples |
| ULQ2003AD | ACTIVE | SOIC | D | 16 | 40 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | ULQ2003A | Samples |
| ULQ2003ADG4 | ACTIVE | SOIC | D | 16 | 40 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | | ULQ2003A | Samples |
| ULQ2003ADR | ACTIVE | SOIC | D | 16 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | ULQ2003A | Samples |
| ULQ2003ADRG4 | ACTIVE | SOIC | D | 16 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | | ULQ2003A | Samples |
| ULQ2003AN | ACTIVE | PDIP | N | 16 | 25 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type | -40 to 85 | ULQ2003A | Samples |
| ULQ2004AD | ACTIVE | SOIC | D | 16 | 40 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | ULQ2004A | Samples |
| ULQ2004ADG4 | ACTIVE | SOIC | D | 16 | 40 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | | ULQ2004A | Samples |
| ULQ2004ADR | ACTIVE | SOIC | D | 16 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | ULQ2004A | Samples |
| ULQ2004ADRG4 | ACTIVE | SOIC | D | 16 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | | ULQ2004A | Samples |
| ULQ2004AN | ACTIVE | PDIP | N | 16 | 25 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type | -40 to 85 | ULQ2004AN | Samples |

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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OTHER QUALIFIED VERSIONS OF ULQ2003A, ULQ2004A :

- Automotive: [ULQ2003A-Q1](#), [ULQ2004A-Q1](#)

NOTE: Qualified Version Definitions:

- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION



QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

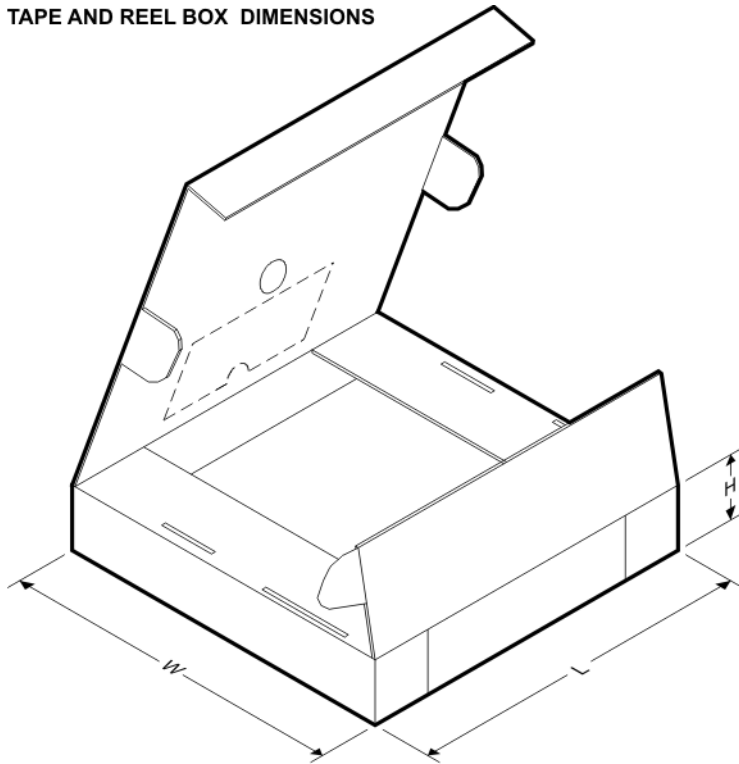


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|----------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| ULN2003ADR | SOIC | D | 16 | 2500 | 330.0 | 16.4 | 6.5 | 10.3 | 2.1 | 8.0 | 16.0 | Q1 |
| ULN2003ADR | SOIC | D | 16 | 2500 | 330.0 | 16.8 | 6.5 | 10.3 | 2.1 | 8.0 | 16.0 | Q1 |
| ULN2003ADR | SOIC | D | 16 | 2500 | 330.0 | 16.4 | 6.5 | 10.3 | 2.1 | 8.0 | 16.0 | Q1 |
| ULN2003ADRG3 | SOIC | D | 16 | 2500 | 330.0 | 16.8 | 6.5 | 10.3 | 2.1 | 8.0 | 16.0 | Q1 |
| ULN2003ADRG4 | SOIC | D | 16 | 2500 | 330.0 | 16.4 | 6.5 | 10.3 | 2.1 | 8.0 | 16.0 | Q1 |
| ULN2003AIDR | SOIC | D | 16 | 2500 | 330.0 | 16.4 | 6.5 | 10.3 | 2.1 | 8.0 | 16.0 | Q1 |
| ULN2003AIDR | SOIC | D | 16 | 2500 | 330.0 | 16.8 | 6.5 | 10.3 | 2.1 | 8.0 | 16.0 | Q1 |
| ULN2003AIDRG4 | SOIC | D | 16 | 2500 | 330.0 | 16.4 | 6.5 | 10.3 | 2.1 | 8.0 | 16.0 | Q1 |
| ULN2003AIPWR | TSSOP | PW | 16 | 2000 | 330.0 | 12.4 | 6.9 | 5.6 | 1.6 | 8.0 | 12.0 | Q1 |
| ULN2003AIPWR | TSSOP | PW | 16 | 2000 | 330.0 | 12.4 | 6.9 | 5.6 | 1.6 | 8.0 | 12.0 | Q1 |
| ULN2003AIPWRG4 | TSSOP | PW | 16 | 2000 | 330.0 | 12.4 | 6.9 | 5.6 | 1.6 | 8.0 | 12.0 | Q1 |
| ULN2003APWR | TSSOP | PW | 16 | 2000 | 330.0 | 12.4 | 6.9 | 5.6 | 1.6 | 8.0 | 12.0 | Q1 |
| ULN2003APWR | TSSOP | PW | 16 | 2000 | 330.0 | 12.4 | 6.9 | 5.6 | 1.6 | 8.0 | 12.0 | Q1 |
| ULN2003APWRG4 | TSSOP | PW | 16 | 2000 | 330.0 | 12.4 | 6.9 | 5.6 | 1.6 | 8.0 | 12.0 | Q1 |
| ULN2004ADR | SOIC | D | 16 | 2500 | 330.0 | 16.4 | 6.5 | 10.3 | 2.1 | 8.0 | 16.0 | Q1 |
| ULN2004ADR | SOIC | D | 16 | 2500 | 330.0 | 16.4 | 6.5 | 10.3 | 2.1 | 8.0 | 16.0 | Q1 |
| ULN2004ADR | SOIC | D | 16 | 2500 | 330.0 | 16.8 | 6.5 | 10.3 | 2.1 | 8.0 | 16.0 | Q1 |
| ULN2004ADRG4 | SOIC | D | 16 | 2500 | 330.0 | 16.4 | 6.5 | 10.3 | 2.1 | 8.0 | 16.0 | Q1 |

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|--------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| ULN2004ADRG4 | SOIC | D | 16 | 2500 | 330.0 | 16.4 | 6.5 | 10.3 | 2.1 | 8.0 | 16.0 | Q1 |
| ULQ2003ADR | SOIC | D | 16 | 2500 | 330.0 | 16.4 | 6.5 | 10.3 | 2.1 | 8.0 | 16.0 | Q1 |
| ULQ2003ADRG4 | SOIC | D | 16 | 2500 | 330.0 | 16.4 | 6.5 | 10.3 | 2.1 | 8.0 | 16.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|----------------|--------------|-----------------|------|------|-------------|------------|-------------|
| ULN2003ADR | SOIC | D | 16 | 2500 | 333.2 | 345.9 | 28.6 |
| ULN2003ADR | SOIC | D | 16 | 2500 | 364.0 | 364.0 | 27.0 |
| ULN2003ADR | SOIC | D | 16 | 2500 | 367.0 | 367.0 | 38.0 |
| ULN2003ADRG3 | SOIC | D | 16 | 2500 | 364.0 | 364.0 | 27.0 |
| ULN2003ADRG4 | SOIC | D | 16 | 2500 | 333.2 | 345.9 | 28.6 |
| ULN2003AIDR | SOIC | D | 16 | 2500 | 333.2 | 345.9 | 28.6 |
| ULN2003AIDR | SOIC | D | 16 | 2500 | 364.0 | 364.0 | 27.0 |
| ULN2003AIDRG4 | SOIC | D | 16 | 2500 | 333.2 | 345.9 | 28.6 |
| ULN2003AIPWR | TSSOP | PW | 16 | 2000 | 364.0 | 364.0 | 27.0 |
| ULN2003AIPWR | TSSOP | PW | 16 | 2000 | 367.0 | 367.0 | 35.0 |
| ULN2003AIPWRG4 | TSSOP | PW | 16 | 2000 | 367.0 | 367.0 | 35.0 |
| ULN2003APWR | TSSOP | PW | 16 | 2000 | 364.0 | 364.0 | 27.0 |
| ULN2003APWR | TSSOP | PW | 16 | 2000 | 367.0 | 367.0 | 35.0 |
| ULN2003APWRG4 | TSSOP | PW | 16 | 2000 | 367.0 | 367.0 | 35.0 |

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|--------------|--------------|-----------------|------|------|-------------|------------|-------------|
| ULN2004ADR | SOIC | D | 16 | 2500 | 367.0 | 367.0 | 38.0 |
| ULN2004ADR | SOIC | D | 16 | 2500 | 333.2 | 345.9 | 28.6 |
| ULN2004ADR | SOIC | D | 16 | 2500 | 364.0 | 364.0 | 27.0 |
| ULN2004ADRG4 | SOIC | D | 16 | 2500 | 367.0 | 367.0 | 38.0 |
| ULN2004ADRG4 | SOIC | D | 16 | 2500 | 333.2 | 345.9 | 28.6 |
| ULQ2003ADR | SOIC | D | 16 | 2500 | 333.2 | 345.9 | 28.6 |
| ULQ2003ADRG4 | SOIC | D | 16 | 2500 | 367.0 | 367.0 | 38.0 |

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



4040047-6/M 06/11

- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 -  C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
 -  D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
 - E. Reference JEDEC MS-012 variation AC.

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate designs.
 - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

MECHANICAL DATA

NS (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

PW (R-PDSO-G16)

PLASTIC SMALL OUTLINE



4040064-4/G 02/11

- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 -  Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
 -  Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
 - E. Falls within JEDEC MO-153

PW (R-PDSO-G16)

PLASTIC SMALL OUTLINE



- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Publication IPC-7351 is recommended for alternate designs.
 - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 - The 20 pin end lead shoulder width is a vendor option, either half or full width.

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