TPS51206 具有适用于 DDR2、DDR3、DDR3L 和 DDR4 的 VTTREF 缓冲参考输出的 2A 峰值灌/拉电流 DDR 终端稳压器

1 特性

- 电源输入电压：支持 3.3V 和 5V 电源轨
- VLDOIN 输入电压范围：VTT+0.4V 至 3.5V
- VTT 端接稳压器
  - 输出电压范围：0.5V 至 0.9V
  - 2A 峰值灌电流和拉电流
  - 仅需 10µF 的多层陶瓷电容 (MLCC) 输出电容
  - ±20mV 精度
- VTTREF 缓冲参考输出
  - VDDQ/2 ± 1% 精度
  - 10mA 灌/拉电流
- 支持高阻态（S3 状态）和软停止（S4 和 S5 状态），通过 S3 和 S5 输入选择
- 过热保护
- 10 引脚 2mm × 2mm 小外形尺寸无引线 (SON) (DSQ) 封装

2 应用

- DDR2、DDR3、DDR3L 和 DDR4 存储器电源
- SSTL_18、SSTL_15、SSTL_135 和 HSTL 端接

3 说明

TPS51206 是一款具有 VTTREF 缓冲参考输出的灌/拉电流双倍数据速率 (DDR) 终端稳压器。该器件专门针对低输入电压、低成本、低外部元件数的空间受限类系统而设计。TPS51206 可保持快速的瞬态响应，并且仅需 1 个 10µF 的陶瓷输出电容。TPS51206 支持远程感测功能，并且可满足 DDR2、DDR3 和低功耗 DDR3 (DDR3L) 及 DDR4 VTT 总线的所有电源要求。VTT 具有 ±2A 峰值电流能力。该器件支持所有 DDR 电源状态，在 S3 状态下将 VTT 置于高阻态（挂起到 RAM）；在 S4/S5 状态下使 VTT 和 VTTREF 放电（挂起到磁盘）。

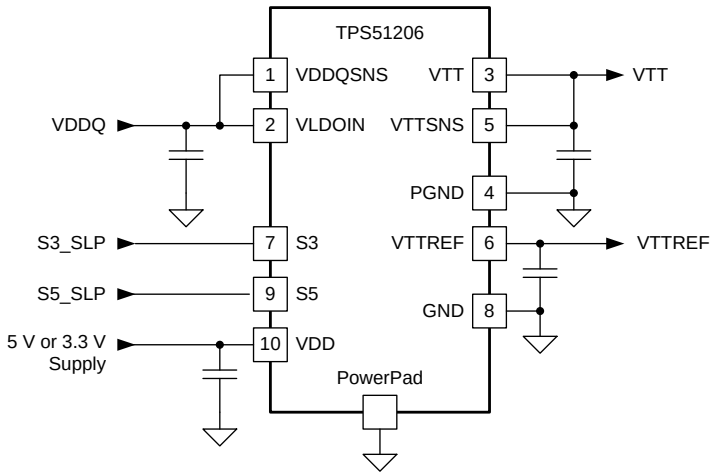
TPS51206 采用 10 引脚、2mm × 2mm SON (DSQ) PowerPAD™封装，额定工作温度范围为 –40°C 至 85°C。

器件信息(1)

器件型号	封装	封装尺寸（标称值）
TPS51206	WSON (10)	2.00mm x 2.00mm

(1) 如需了解所有可用封装，请见数据表末尾的可订购产品附录。

简化应用



目录

4 修订历史记录

注：之前版本的页码可能与当前版本有所不同。

Changes from Revision B (December 2014) to Revision C **Page**

- 已添加 参考至 DDR4 兼容性 ... 1
- 已添加 *接收文档更新通知* 部分 ... 18
- 已添加 *社区资源* 部分 ... 18

Changes from Revision A (October 2013) to Revision B **Page**

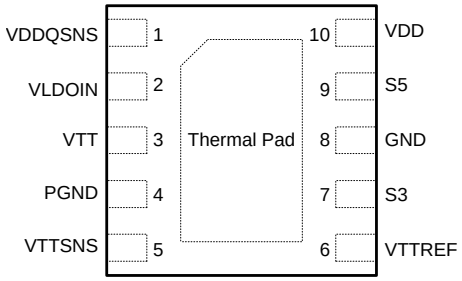
- 已添加 *引脚配置和功能*部分，*ESD 额定值*表，*特性 描述* 部分，*器件功能模式*，*应用和实施*部分，*电源相关建议*部分，*布局*部分，*器件和文档支持*部分以及*机械、封装和可订购信息*部分 ... 1

Changes from Original (MAY 2011) to Revision A **Page**

- 已添加 minimum and maximum values to the wake up condition of the VDD UVLO threshold voltage specification ... 5

5 Pin Configuration and Functions

DSQ Package
10-Pin WSON
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
GND	8	–	Signal ground
PGND	4	–	Power GND for VTT LDO
S3	7	I	S3 signal input
S5	9	I	S5 signal input
VDD	10	I	Device power supply input (3.3 V or 5 V)
VDDQSNS	1	I	VDDQ sense input, reference input for VTTREF
VLDOIN	2	I	Power supply input for VTT/ VTTREF
VTT	3	O	Power output for VTT LDO, need to connect 10-μF or greater MLCC for stability
VTTREF	6	O	VTTREF buffered reference output. Need to connect 0.22-μF or greater MLCC for stability
VTTSNS	5	I	VTT LDO voltage sense input
Thermal Pad		—	Solder to the ground plane for increased thermal performance.

6 Specifications

6.1 Absolute Maximum Ratings(1)

		MIN	MAX	UNIT
Input voltage (2)	VDD, S3, S5	–0.3	7	V
	VLDOIN, VTTSNS, VDDQSNS	–0.3	3.6	V
	PGND	–0.3	0.3	
Output voltage (2)	VTT, VTTREF	–0.3	3.6	
Junction temperature, T_J			125	°C
Operating free-air temperature, T_A		–55	150	°C
Storage temperature, T_{stg}		–55	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings*(1) may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to the network ground terminal unless otherwise noted.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

		MIN	NOM	MAX	UNIT
Supply voltage	VDD	3.1		6.5	V
Input voltage range(1)	S3, S5	–0.1		6.5	V
	VLDOIN, VTTSNS, VDDQSNS	–0.1		3.5	
	PGND	–0.1		0.1	
Output voltage range(1)	VTT, VTTREF	–0.1		3.5	V
Operating free-air temperature, T_A		–40		85	°C

(1) All voltage values are with respect to the network ground terminal unless otherwise noted.

6.4 Thermal Information

THERMAL METRIC(1)		TPS51206 DSQ (WSON) 10 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	70.3	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	46.3	
$R_{\theta JB}$	Junction-to-board thermal resistance	33.8	
ψ_{JT}	Junction-to-top characterization parameter	2.9	
ψ_{JB}	Junction-to-board characterization parameter	33.5	
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	16.3	

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report (SPRA953).

6.5 Electrical Characteristics

over operating free-air temperature range, V_{VDD} = 5 V, VLDOIN is connected to VDDQSNS, V_{S3} = V_{S5} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
SUPPLY CURRENT						
$I_{VDD(S0)}$	VDD supply current, in S0	T_A = 25°C, No load, V_{S3} = V_{S5} = 5 V, $V_{VDDQSNS}$ = 1.8 V		170		μA
$I_{VDD(S3)}$	VDD supply current, in S3	T_A = 25°C, No load, V_{S3} = 0 V, V_{S5} = 5 V, $V_{VDDQSNS}$ = 1.8 V		80		μA
I_{VDDSDN}	VDD shutdown current, in S4 and S5	T_A = 25°C, No load, V_{S3} = V_{S5} = 0 V, $V_{VDDQSNS}$ = 1.8 V			1	μA
$I_{VLDOIN(S0)}$	VLDOIN supply current, in S0	T_A = 25°C, No load, V_{S3} = V_{S5} = 5 V, V_{LDION} = 1.8 V			5	μA
$I_{VLDOIN(s3)}$	VLDOIN supply current, in S3	T_A = 25°C, No load, V_{S3} = 0 V, V_{S5} = 5 V, V_{LDION} = 1.8 V			5	μA
$I_{VLDOINSDN}$	VLDOIN shutdown current, in S4 and S5	T_A = 25°C, No load, V_{S3} = V_{S5} = 0 V, V_{LDION} = 1.8 V			5	μA
VTTREF OUTPUT						
V_{VTTREF}	Output voltage			$V_{VDDQSNS}$/2		V
$V_{VTTREFTOL}$	Output voltage tolerance to $V_{VDDQSNS}$	$\|I_{VTTREF}\|$< 10 mA, 1.5 V ≤ $V_{VDDQSNS}$ ≤ 1.8 V	49%	50%	51%	
		$\|I_{VTTREF}\|$< 10 mA, 1.2 V ≤ $V_{VDDQSNS}$ < 1.5 V	48.75%		51.25%	
$I_{VTTREFSRC}$	Source current	$V_{VDDQSNS}$ = 1.8 V, V_{VTTREF} = 0 V	10			mA
$I_{VTTREFSNK}$	Sink current	$V_{VDDQSNS}$ = 0 V, V_{VTTREF} = 1.8 V	10			mA
$I_{VTTREFDIS}$	VTTREF Discharge current	T_A = 25°C, V_{S3} = V_{S5} = 0V, V_{VTTREF} = 0.5 V		1.3		mA
VTT OUTPUT						
V_{VTT}	Output voltage			$V_{VDDQSNS}$/2		V
V_{VTTTOL}	Output voltage tolerance to $V_{VDDQSNS}$/2	$\|I_{VTT}\|$≤ 10 mA, 1.4 V ≤ $V_{VDDQSNS}$ ≤ 1.8 V	–20		20	mV
		$\|I_{VTT}\|$< 1 A, 1.4 V ≤ $V_{VDDQSNS}$ ≤ 1.8 V(1)	–30		30	
		$\|I_{VTT}\|$ < 2 A, 1.4 V ≤ $V_{VDDQSNS}$ ≤ 1.8 V(1)	–40		40	
		$\|I_{VTT}\|$≤ 10 mA, 1.2 V ≤ $V_{VDDQSNS}$ ≤ 1.4 V	–20		20	
		$\|I_{VTT}\|$ < 1 A, 1.2 V ≤ $V_{VDDQSNS}$ ≤ 1.4 V(1)	–30		30	
		$\|I_{VTT}\|$< 1.5 A, 1.2 V ≤ $V_{VDDQSNS}$ < 1.4 V(1)	–40		40	
$I_{VTTOCLSRC}$	Source current limit	$V_{VDDQSNS}$ = 1.8 V, V_{VTT} = V_{VTTSNS} = 0.7 V	2			A
$I_{VTTOCLSNK}$	Sink current limit	$V_{VDDQSNS}$ = 1.8 V, V_{VTT} = V_{VTTSNS} = 1.1 V	2			A
I_{VTTLK}	Leakage current	T_A = 25°C , V_{S3} = 0 V, V_{S5} = 5 V, V_{VTT} = V_{VTTREF}			5	μA
$I_{VTTSNSBIAS}$	VTTSNS input bias current	V_{S3} = 5 V, V_{S5} = 5 V, V_{VTTSNS} = V_{VTTREF}	–0.1		0.1	μA
$I_{VTTSNSLK}$	VTTSNS leakage current	V_{S3} = 0 V, V_{S5} = 5 V, V_{VTTSNS} = V_{VTTREF}	–0.1		0.1	μA
I_{VTTDIS}	VTT Discharge current	T_A = 25°C, V_{S3} = V_{S5} = $V_{VDDQSNS}$ = 0 V, V_{VTT} = 0.5 V		7		mA
VDDQ INPUT						
$I_{VDDQSNS}$	VDDQSNS input current	$V_{VDDQSNS}$ = 1.8 V		30		μA
UVLO/LOGIC THRESHOLD						
V_{VDDUV}	VDD UVLO threshold voltage	Wake up	2.67	2.90	3.00	V
		Hysteresis		0.2		
V_{LL}	S3 and S5 low-level voltage				0.5	V
V_{LH}	S3 and S5 high-level voltage		1.8			V
V_{LHYST}	S3 and S5 hysteresis voltage			0.3		V
I_{LHLK}	S3 and S5 input leak current		–1		1	μA
OVER-TEMPERATURE PROTECTION						
T_{OTP}	Over temperature protection	Shutdown temperature(1)		150		°C
		Hysteresis(1)		10		

(1) Ensured by design. Not production tested.

6.6 Typical Characteristics

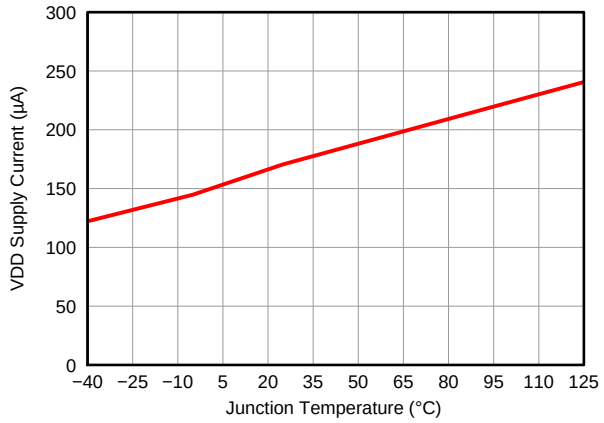


图 1. VDD Supply Current vs. Junction Temperature

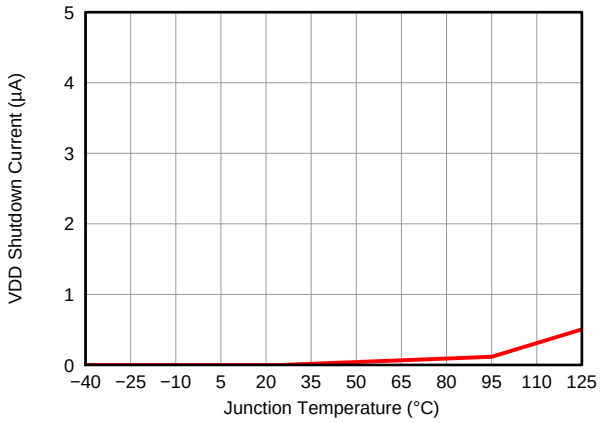


图 2. VDD Shutdown Current vs. Junction Temperature

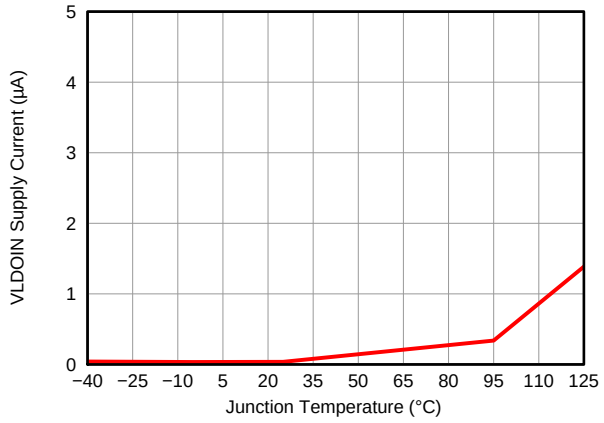


图 3. VLDOIN Supply Current vs. Junction Temperature

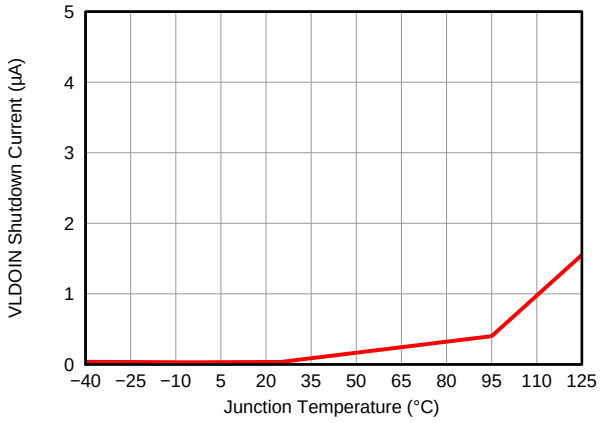


图 4. VLDOIN Shutdown Current vs. Junction Temperature

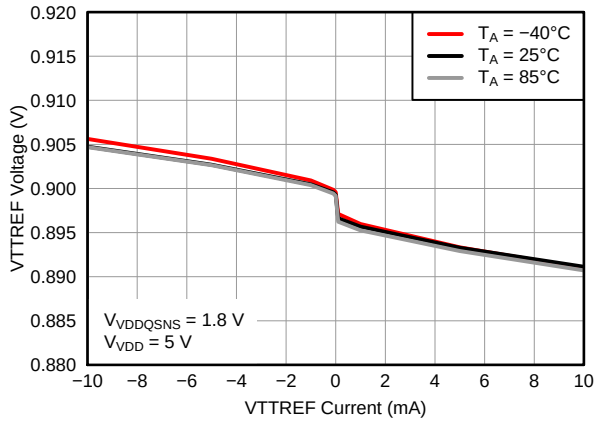


图 5. VTTREF Load Regulation (0.9 V)

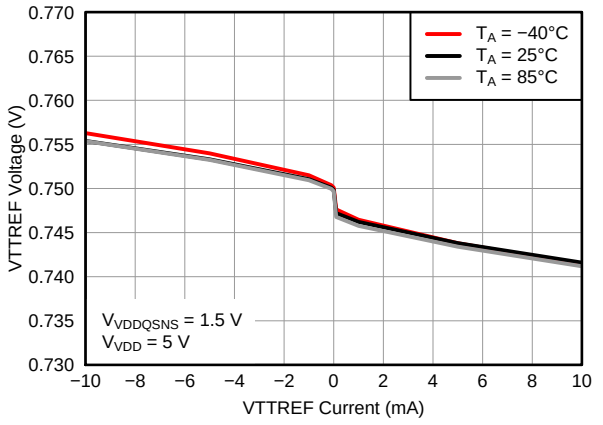


图 6. VTTREF Load Regulation (0.75 V)

Typical Characteristics (接下页)

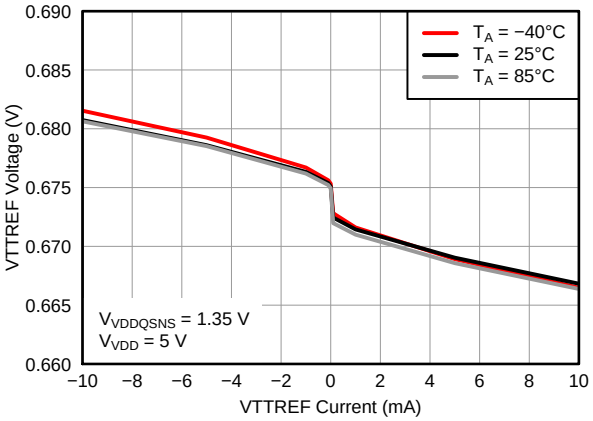


图 7. VTTREF Load Regulation (0.675 V)

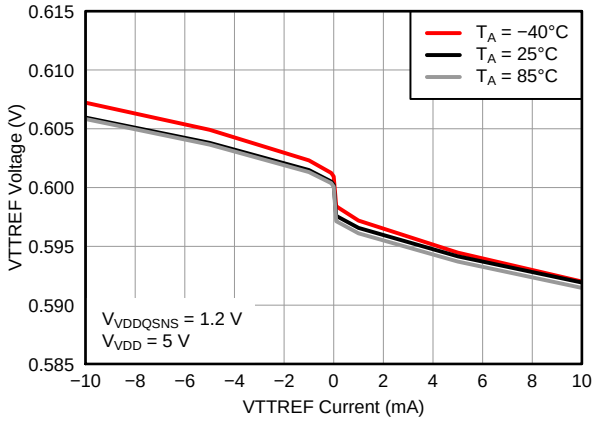


图 8. VTTREF Load Regulation (0.6 V)

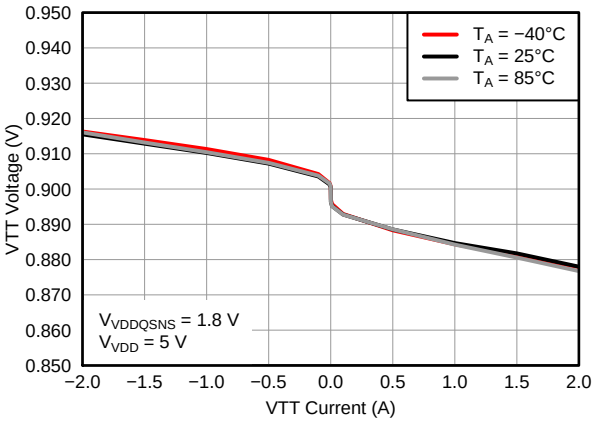


图 9. VTT Load Regulation (0.9 V)

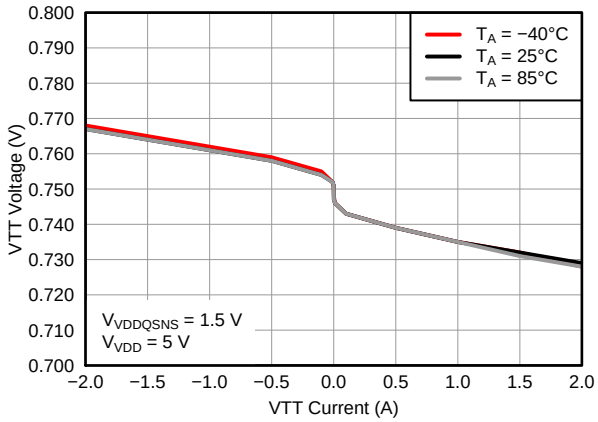


图 10. VTT Load Regulation (0.75 V)

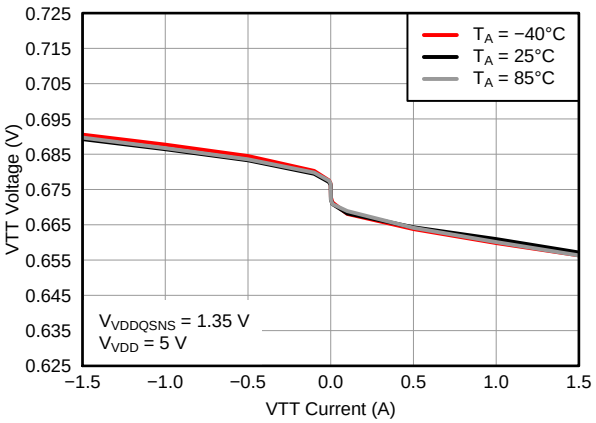


图 11. VTT Load Regulation (0.675 V)

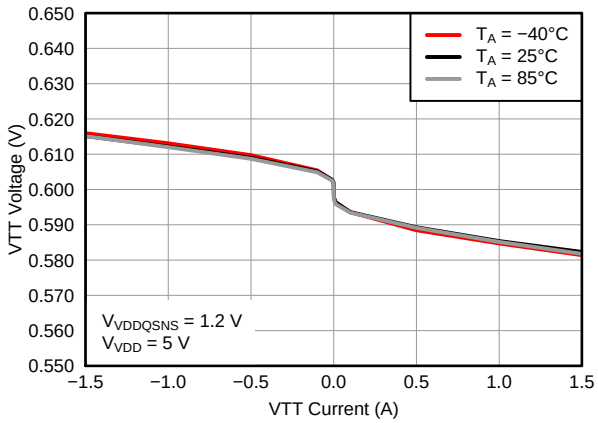


图 12. VTT Load Regulation (0.6 V)

Typical Characteristics (接下页)

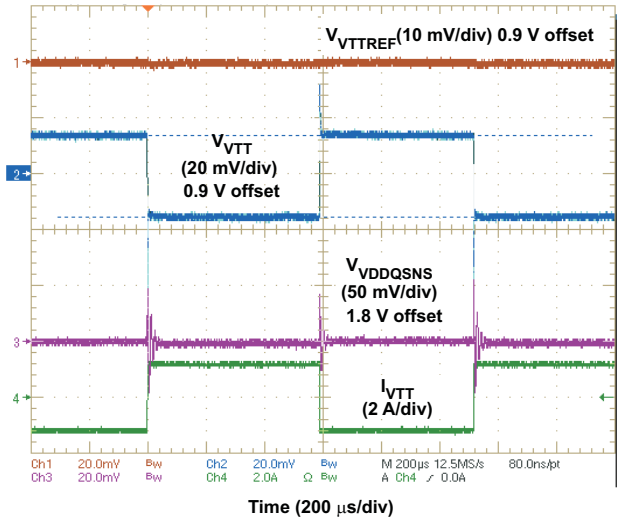


图 13. VTT Load Transient Response (0.9 V)

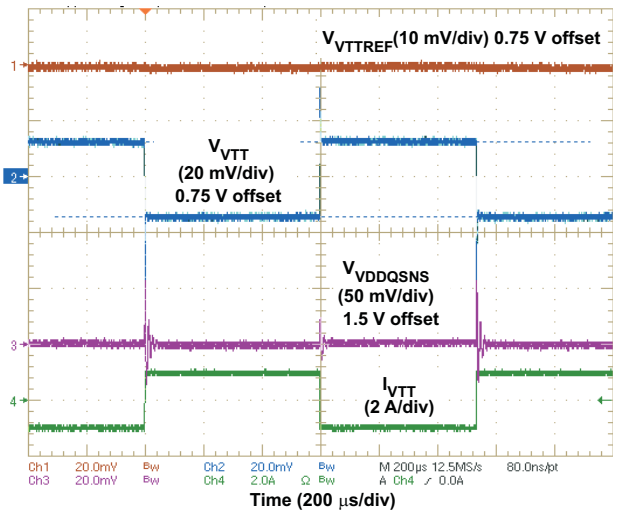


图 14. VTT Load Transient Response (0.75 V)

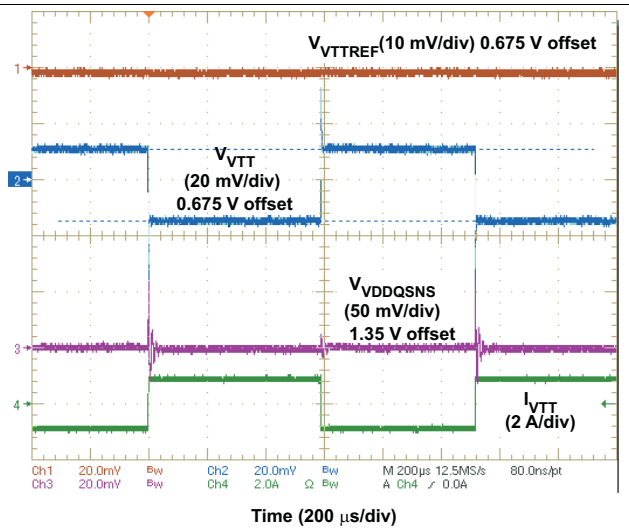


图 15. VTT Load Transient Response (0.675 V)

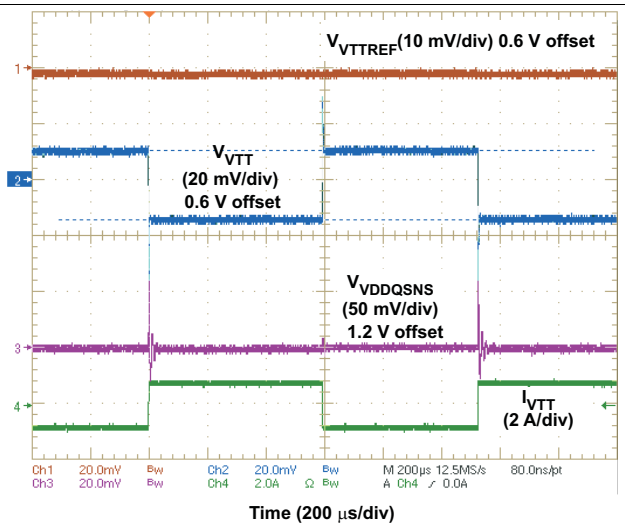


图 16. VTT Load Transient Response (0.6 V)

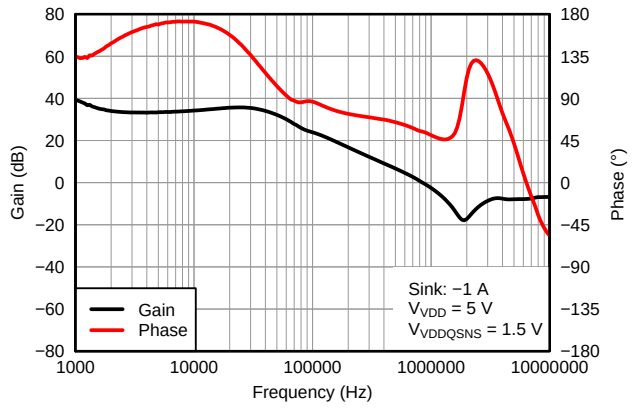


图 17. VTT (Sink: -1 A) Bode Plot (0.75 V)

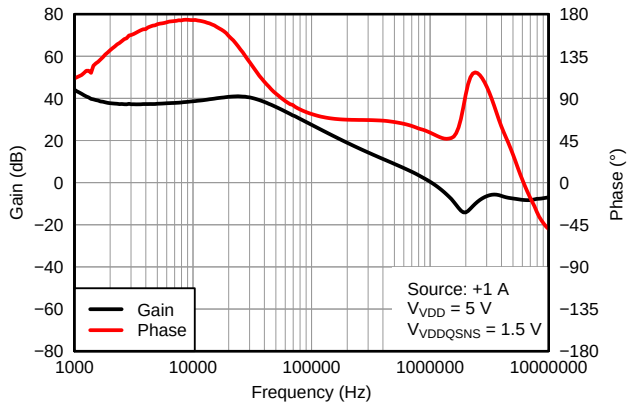


图 18. VTT (Source: +1 A) Bode Plot (0.75 V)

Typical Characteristics (接下页)

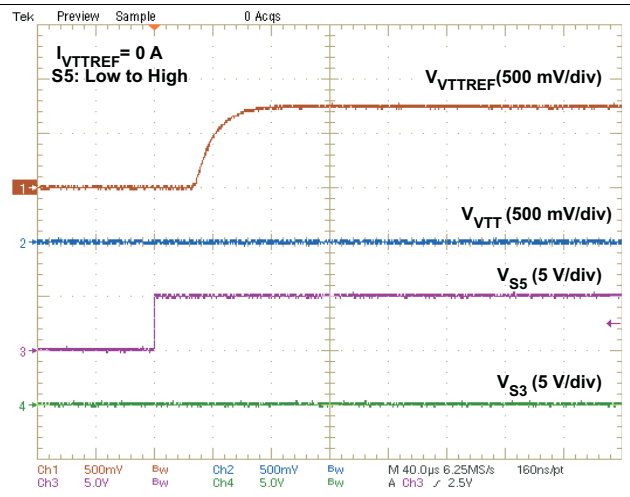


图 19. Start-Up Waveforms (S5: Low to High)

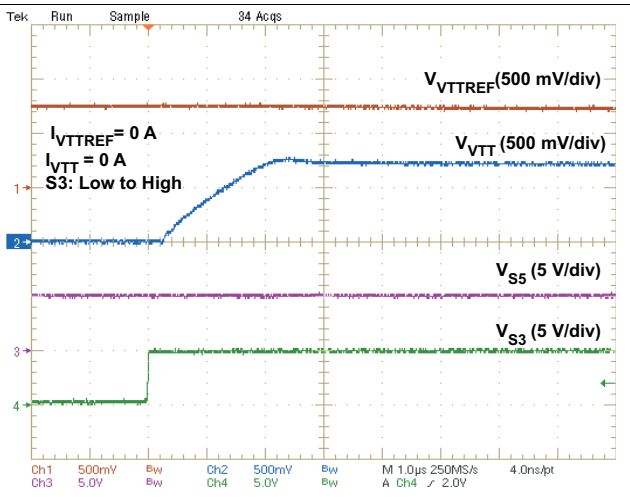


图 20. Start-Up Waveforms (S3: Low to High)

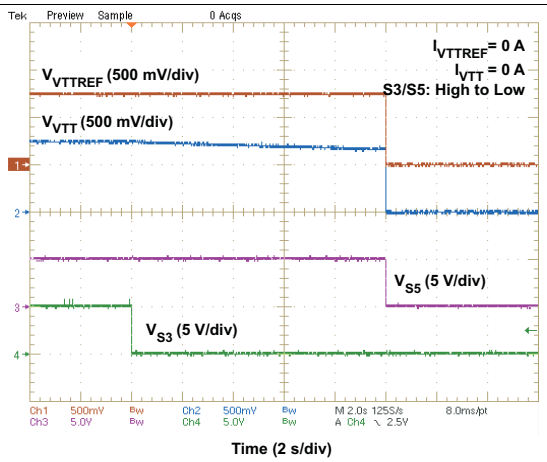


图 21. Shutdown Waveforms (S3/ S5: High to Low)

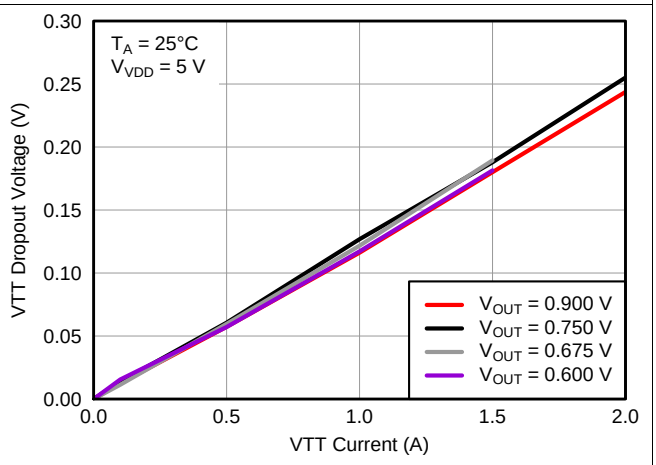


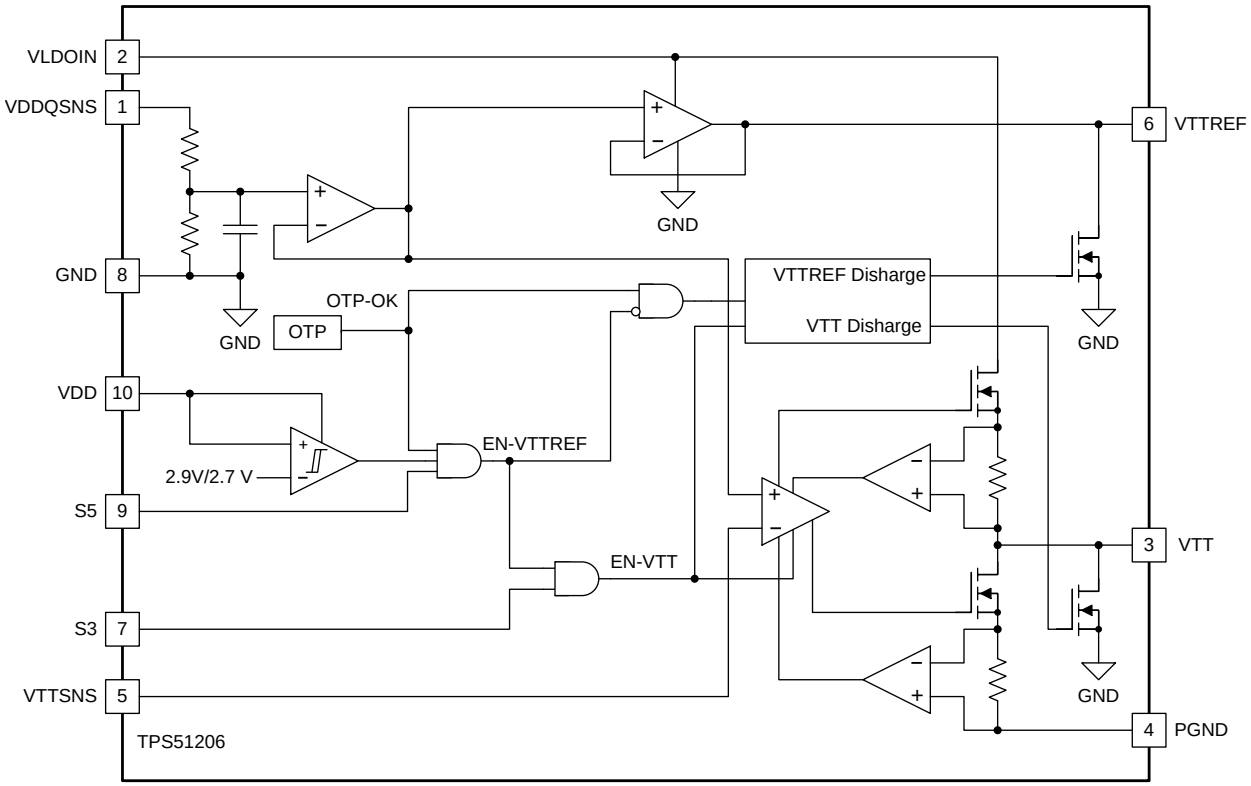
图 22. VTT Dropout Voltage

7 Detailed Description

7.1 Overview

The TPS51206 is a sink or source double date rate (DDR) termination regulator with VTTREF buffered reference output.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 VTT Sink and Source Regulator

The TPS51206 is a sink or source tracking termination regulator specifically designed for low input voltage, low cost, and low external component count systems where space is a key application parameter. The TPS51206 integrates a high-performance, low-dropout (LDO) linear regulator (VTT) that has ultimate fast response to track ½ VDDQSNS within 40 mV at all conditions, and its current capability is 2 A for both sink and source directions. A 10-µF (or greater) ceramic capacitor(s) need to be attached close to the VTT terminal for stable operation. A grade of X5R or better is recommended. To achieve tight regulation with minimum effect of trace resistance, the remote sensing terminal, VTTSNS, should be connected to the positive terminal of the output capacitor(s) as a separate trace from the high current path from the VTT pin.

The device has a dedicated pin, VLDOIN, for VTT power supply to minimize the LDO power dissipation on user application. The minimum VLDOIN voltage is 0.4 V above the ½ VDDQSNS voltage.

7.3.2 VTTREF

The VTTREF pin includes 10 mA of sink or source current capability, and tracks ½ of VDDQSNS with ±1% accuracy. A 0.22-µF ceramic capacitor needs to be attached close to the VTTREF terminal for stable operation; X5R or better grade is recommended.

Feature Description (接下页)

7.3.3 VDD Undervoltage Lockout Protection

The TPS51206 input voltage (VDD) includes undervoltage lockout protection (UVLO). When the VDD pin voltage is lower than UVLO threshold voltage, VTT and VTTREF are shut off. This is non-latch protection.

7.3.4 Overtemperature Protection

This device features internal temperature monitoring. If the temperature exceeds the threshold value, VTT and VTTREF are shut off. This is a non-latch protection.

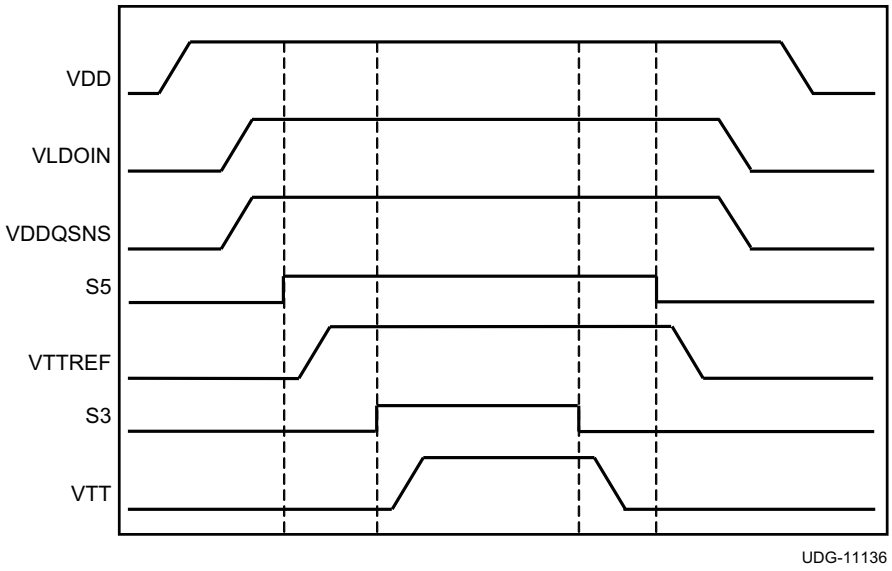


图 23. Typical Timing Diagram

7.4 Device Functional Modes

7.4.1 Power State Control

The TPS51206 has two input pins, S3 and S5, to provide simple control of the power state. 表 1 describes S3 and S5 terminal logic state and corresponding state of VTTREF and VTT outputs. VTT is turn-off and placed to high impedance (High-Z) state in S3. The VTT output is floated and does not sink or source current in this state. When both S5 and S3 pins are LOW, the power state is set to S4 and S5 . In S4 and S5 state, all the outputs are turn-off and discharged to GND.

表 1. S3 and S5 Control Table

STATE	S3	S5	VTTREF	VTT
S0	HI	HI	ON	ON
S3	LO	HI	ON	OFF(High-Z)
S4 and S5	LO	LO	OFF(Discharge)	OFF(Discharge)

8 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The TPS51206 is typically used as a sink and source tracking termination regulator which converts a voltage from VTT+0.4 V to 3.5 V

8.2 Typical Applications

8.2.1 VLDOIN = VDDQ Configuration

图 24 shows an application diagram for a configuration where VLDOIN and VDDQ are connected.

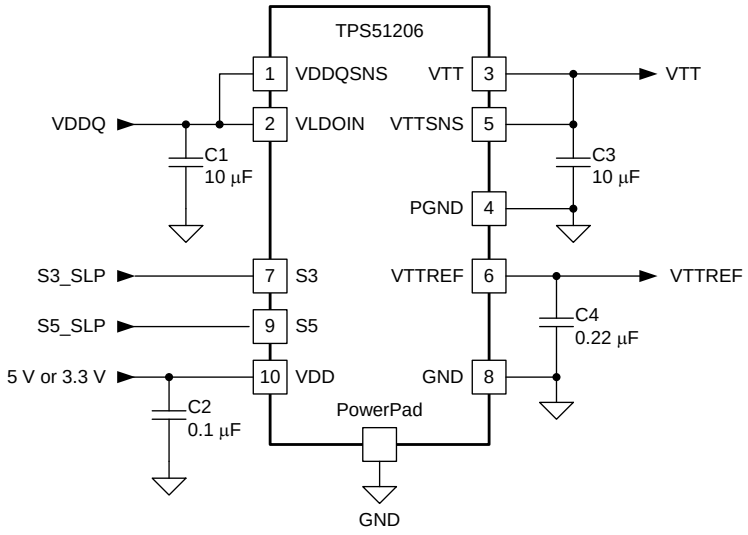


图 24. VLDOIN = VDDQ Configuration

8.2.1.1 Design Requirements

表 2. Design Parameters

PARAMETER	EXAMPLE VALUE
Supply Voltage (VDD)	3.3 V or 5 V
VLDOIN = VDDQ	1.5 V
Output Current	±2 A

8.2.1.2 Detailed Design Procedure

表 3. VLDOIN = VDDQ Configuration Components

REFERENCE DESIGNATOR	SPECIFICATION	MANUFACTURER	PART NUMBER
C1, C3	10 µF, 6.3 V, X5R, 1608 (0603)	Taiyo Yuden	JMK107BJ106MA
C2	0.1 µF, 6.3 V, X5R, 1005 (0402)	Taiyo Yuden	JWK105BJ104MP
C4	0.22 µF, 6.3 V, X5R, 1005 (0402)	Taiyo Yuden	JMK105BJ224KV

8.2.1.2.1 VDD Capacitor

Add a ceramic capacitor, with a value 0.1 µF (or greater) and X5R grade (or better), placed close to the VDD terminal, to stabilize the bias supply voltage from any parasitic impedance from the power supply rail.

8.2.1.2.2 VLDOIN Capacitor

Depending on the trace impedance between the VLDOIN bulk power supply to the device, a transient increase of source current is supplied mostly by the charge from the VLDOIN input capacitor. Use a 10-µF (or greater) and X5R grade (or better) ceramic capacitor to supply this transient charge.

8.2.1.2.3 VTTREF Capacitor

Add a ceramic capacitor, with a value 0.22 µF and X5R grade (or better), placed close to the VTTREF terminal for stable operation.

8.2.1.2.4 VTT Capacitor

For stable operation, a 10-µF (or greater) and X5R (or better) grade ceramic capacitor(s) need to be attached close to the VTT terminal. This capacitor is recommended to minimize any additional equivalent series resistance (ESR) and/or equivalent series inductance (ESL) of ground trace between the PGND terminal and the VTT capacitor(s).

8.2.1.2.5 VTTSNS Connection

To achieve tight regulation with minimum effect of trace resistance, a remote sensing terminal, the VTTSNS pin should be connected to the positive terminal of the VTT pin output capacitor(s) as a separate trace from the high-current path from VTT. Consider adding a low-pass R-C filter at the VTTSNS pin in case the ESR of the VTT output capacitor(s) is larger than 2 mΩ. The R-C filter time constant should be approximately the same or slightly lower than the time constant of the VTT output capacitance and ESR.

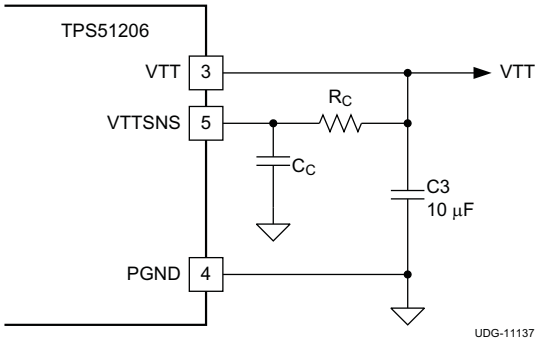


图 25. R-C Filter for VTTSNS

8.2.1.2.6 VDDQSNS Connection

VDDQSNS is a reference input of the VTTREF and VTT. Trace should be routed away from noise-generating lines.

8.2.1.3 Application Curves

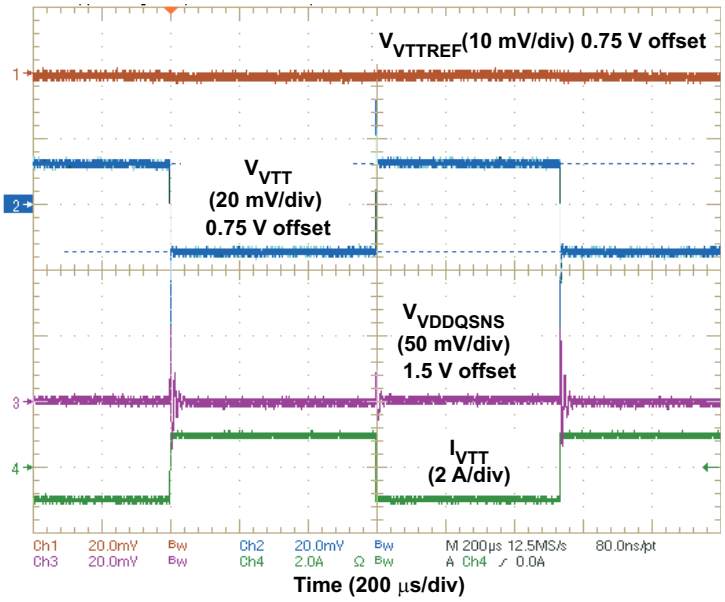


图 26. VTT Load Transient Response (0.75 V)

8.2.2 VLDOIN Separated from VDDQ Configuration

图 27 shows an application diagram for a configuration where VLDOIN and VDDQ are separated.

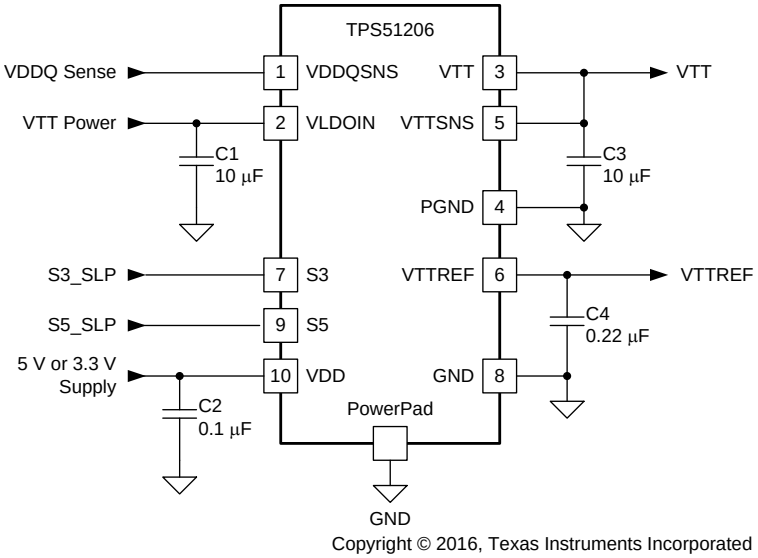


图 27. VLDOIN Separated from VDDQ Configuration

8.2.2.1 Design Requirements

表 4. Design Parameters

PARAMETER	EXAMPLE VALUE
Supply Voltage (VDD)	3.3 V or 5 V
VLDOIN = VDDQ	1.5 V
Output Current	±2 A

8.2.2.2 Detailed Design Procedure

表 5. VLDOIN Separated from VDDQ Configuration Components

REFERENCE DESIGNATOR	SPECIFICATION	MANUFACTURER	PART NUMBER
C1, C3	10 µF, 6.3V, X5R, 1608 (0603)	Taiyo Yuden	JMK107BJ106MA
C2	0.1 µF, 6.3V, X5R, 1005 (0402)	Taiyo Yuden	JWK105BJ104MP
C3	10 µF, 6.3V, X5R, 1608 (0603)	Taiyo Yuden	JMK107BJ106MA
C4	0.22 µF, 6.3V, X5R, 1005 (0402)	Taiyo Yuden	JMK105BJ224KV

8.2.2.3 Application Curves

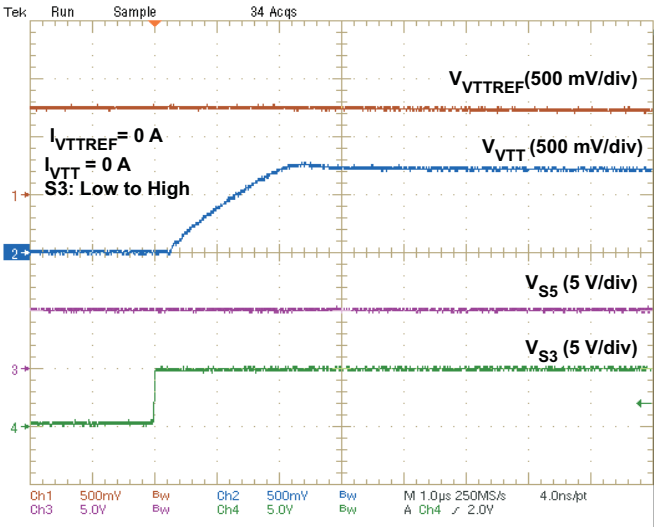


图 28. Start-Up Waveforms (S3: Low to High)

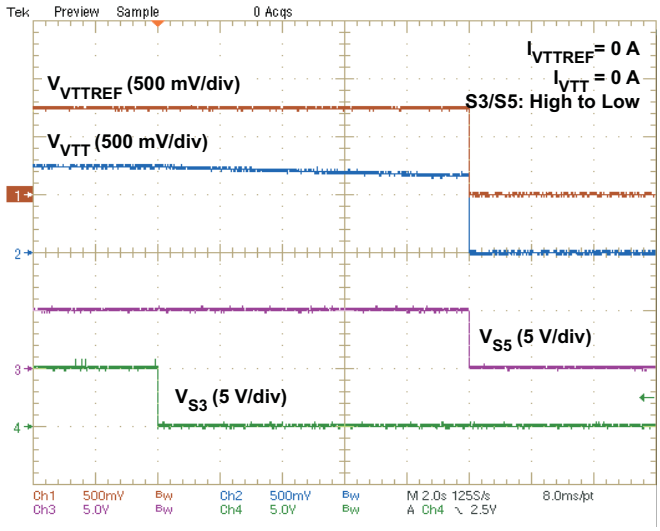


图 29. Shutdown Waveforms (S3 / S5: High to Low)

9 Power Supply Recommendations

TPS51206 is designed for a sink / source double date rate (DDR) termination regulator with VTTREF buffered reference output. Supply input voltage (VDD) supports 3.3-V rail and 5-V rail; VLDOIN input voltage supports VTT+0.4 V to 3.5 V.

10 Layout

10.1 Layout Guidelines

Consider the following before beginning a TPS51206 layout design.

- The input bypass capacitor for VLDOIN should be placed as close as possible to the terminal with short and wide connections.
- The output capacitor for VTT should be placed close to the terminals (VTT and PGND) with short and wide connection in order to avoid additional ESR and/or ESL trace inductance.
- VTTSNS should be connected to the positive node of VTT output capacitor(s) as a separate trace from the high current VTT power trace. In addition, VTTSNS trace should be routed away from high current trace, on the separate layer is recommended. This configuration is strongly recommended to avoid additional ESR and/or ESL. If sensing the voltage at the point of the load is required, it is recommended to attach the output capacitor(s) at that point. In addition, it is recommended to minimize any additional ESR and/or ESL of ground trace between the GND pin and the VTT capacitor(s).
- The GND pin (and the negative node of the VTTREF output capacitor) and PGND pins (and the negative node of the VTT output capacitor) should be connected to the internal system ground planes (for better result, use at least two internal ground planes) with multiple vias. Use as many vias as possible to reduce the impedance between GND pin or PGND pin and the system ground plane.
- In order to effectively remove heat from the package, properly prepare the thermal land. Apply solder directly to the package thermal pad. The wide traces of the component and the side copper connected to the thermal land pad help to dissipate heat. Numerous vias 0.33 mm in diameter connected from the thermal land to the internal/solder side ground plane(s) should also be used to help dissipation. Consult the TPS51206-EVM User's Guide for more detailed layout recommendations.

10.2 Layout Example

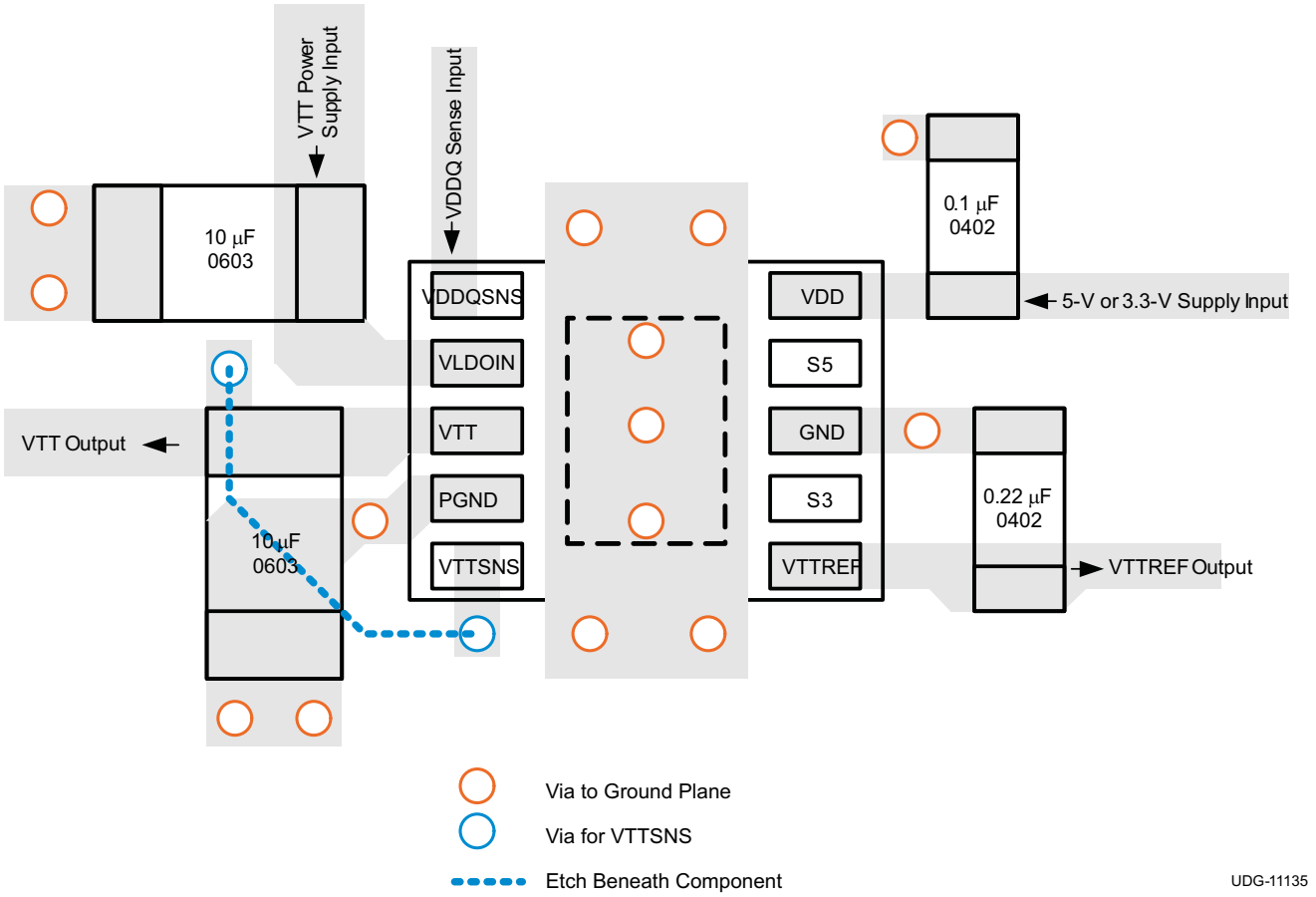


图 30. PCB Layout Guideline

10.3 Thermal Considerations

Because the TPS51206 is a linear regulator, the VTT current flows in both source and sink directions, thereby dissipating power from the device. When the device is sourcing current, the voltage difference between V_{VLDOIN} and V_{VTT} times I_{VTT} (VTT current) current becomes the power dissipation as shown in 公式 1.

$$P_{DISS(src)} = \left(V_{VLDOIN} - V_{VTT}\right) \times I_{VTT(src)} \quad (1)$$

In this case, if the VLDOIN pin is connected to an alternative power supply lower than the VDDQ voltage, overall power loss can be reduced. For the sink phase, VTT voltage is applied across the internal LDO regulator, and the power dissipation can be calculated by 公式 2.

$$P_{DISS(snk)} = V_{VTT} \times I_{VTT(snk)} \quad (2)$$

Maximum power dissipation allowed by the package is calculated by 公式 3.

$$P_{PKG} = \frac{T_{J(max)} - T_{A(max)}}{\theta_{JA}}$$

where

- $T_{J(max)}$ is 125°C
- $T_{A(max)}$ is the maximum ambient temperature in the system
- θ_{JA} is the thermal resistance from junction to ambient (3)

11 器件和文档支持

11.1 器件支持

11.1.1 Third-Party Products Disclaimer

TI'S PUBLICATION OF INFORMATION REGARDING THIRD-PARTY PRODUCTS OR SERVICES DOES NOT CONSTITUTE AN ENDORSEMENT REGARDING THE SUITABILITY OF SUCH PRODUCTS OR SERVICES OR A WARRANTY, REPRESENTATION OR ENDORSEMENT OF SUCH PRODUCTS OR SERVICES, EITHER ALONE OR IN COMBINATION WITH ANY TI PRODUCT OR SERVICE.

11.2 接收文档更新通知

如需接收文档更新通知，请访问 www.ti.com 网站的器件产品文件夹。点击右上角的*提醒我* (Alert me) 注册后，即可每周定期收到已更改的产品信息。有关更改的详细信息，请查阅已修订文档中包含的修订历史记录。

11.3 社区资源

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.4 商标

PowerPAD, E2E are trademarks of Texas Instruments.
All other trademarks are the property of their respective owners.

11.5 静电放电警告

这些装置包含有限的内置 ESD 保护。 存储或装卸时，应将导线一起截短或将装置放置于导电泡棉中，以防止 MOS 门极遭受静电损伤。

11.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 机械、封装和可订购信息

以下页中包括机械、封装和可订购信息。这些信息是针对指定器件可提供的最新数据。这些数据会在无通知且不对本文档进行修订的情况下发生改变。要获得这份数据表的浏览器版本，请查阅左侧的导航栏。

重要声明

德州仪器(TI) 及其下属子公司有权根据 JESD46 最新标准, 对所提供的产品和服务进行更正、修改、增强、改进或其它更改， 并有权根据 JESD48 最新标准中止提供任何产品和服务。客户在下订单前应获取最新的相关信息, 并验证这些信息是否完整且是最新的。所有产品的销售都遵循在订单确认时所提供的TI 销售条款与条件。

TI 保证其所销售的组件的性能符合产品销售时 TI 半导体产品销售条件与条款的适用规范。仅在 TI 保证的范围内，且 TI 认为 有必要时才会使用测试或其它质量控制技术。除非适用法律做出了硬性规定，否则没有必要对每种组件的所有参数进行测试。

TI 对应用帮助或客户产品设计不承担任何义务。客户应对其使用 TI 组件的产品和应用自行负责。为尽量减小与客户产品和应 用相关的风险，客户应提供充分的设计与操作安全措施。

TI 不对任何 TI 专利权、版权、屏蔽作品权或其它与使用了 TI 组件或服务的组合设备、机器或流程相关的 TI 知识产权中授予 的直接或隐含权限作出任何保证或解释。TI 所发布的与第三方产品或服务有关的信息，不能构成从 TI 获得使用这些产品或服 务的许可、授权、或认可。使用此类信息可能需要获得第三方的专利权或其它知识产权方面的许可，或是 TI 的专利权或其它 知识产权方面的许可。

对于 TI 的产品手册或数据表中 TI 信息的重要部分，仅在没有对内容进行任何篡改且带有相关授权、条件、限制和声明的情况 下才允许进行复制。TI 对此类篡改过的文件不承担任何责任或义务。复制第三方的信息可能需要服从额外的限制条件。

在转售 TI 组件或服务时，如果对该组件或服务参数的陈述与 TI 标明的参数相比存在差异或虚假成分，则会失去相关 TI 组件 或服务的所有明示或暗示授权，且这是不正当的、欺诈性商业行为。TI 对任何此类虚假陈述均不承担任何责任或义务。

客户认可并同意，尽管任何应用相关信息或支持仍可能由 TI 提供，但他们将独力负责满足与其产品及在其应用中使用 TI 产品 相关的所有法律、法规和安全相关要求。客户声明并同意，他们具备制定与实施安全措施所需的全部专业技术和知识，可预见 故障的危险后果、监测故障及其后果、降低有可能造成人身伤害的故障的发生机率并采取适当的补救措施。客户将全额赔偿因 在此类安全关键应用中使用任何 TI 组件而对 TI 及其代理造成的任何损失。

在某些场合中，为了推进安全相关应用有可能对 TI 组件进行特别的促销。TI 的目标是利用此类组件帮助客户设计和创立其特 有的可满足适用的功能安全性标准和要求的终端产品解决方案。尽管如此，此类组件仍然服从这些条款。

TI 组件未获得用于 FDA Class III（或类似的生命攸关医疗设备）的授权许可，除非各方授权官员已经达成了专门管控此类使 用的特别协议。

只有那些 TI 特别注明属于军用等级或"增强型塑料"的 TI 组件才是设计或专门用于军事/航空应用或环境的。购买者认可并同 意，对并非指定面向军事或航空航天用途的 TI 组件进行军事或航空航天方面的应用，其风险由客户单独承担，并且由客户独 力负责满足与此类使用相关的所有法律和法规要求。

TI 已明确指定符合 ISO/TS16949 要求的产品，这些产品主要用于汽车。在任何情况下，因使用非指定产品而无法达到 ISO/TS16949 要求，TI不承担任何责任。

	产品		应用
数字音频	www.ti.com.cn/audio	通信与电信	www.ti.com.cn/telecom
放大器和线性器件	www.ti.com.cn/amplifiers	计算机及周边	www.ti.com.cn/computer
数据转换器	www.ti.com.cn/dataconverters	消费电子	www.ti.com/consumer-apps
DLP® 产品	www.dlp.com	能源	www.ti.com/energy
DSP - 数字信号处理器	www.ti.com.cn/dsp	工业应用	www.ti.com.cn/industrial
时钟和计时器	www.ti.com.cn/clockandtimers	医疗电子	www.ti.com.cn/medical
接口	www.ti.com.cn/interface	安防应用	www.ti.com.cn/security
逻辑	www.ti.com.cn/logic	汽车电子	www.ti.com.cn/automotive
电源管理	www.ti.com.cn/power	视频和影像	www.ti.com.cn/video
微控制器 (MCU)	www.ti.com.cn/microcontrollers		
RFID 系统	www.ti.com.cn/rfidsys		
OMAP应用处理器	www.ti.com/omap		
无线连通性	www.ti.com.cn/wirelessconnectivity	德州仪器在线技术支持社区	www.deyisupport.com

邮寄地址： 上海市浦东新区世纪大道1568 号，中建大厦32 楼邮政编码： 200122

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS51206DSQR	ACTIVE	WSON	DSQ	10	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	1206	Samples
TPS51206DSQT	ACTIVE	WSON	DSQ	10	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	1206	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

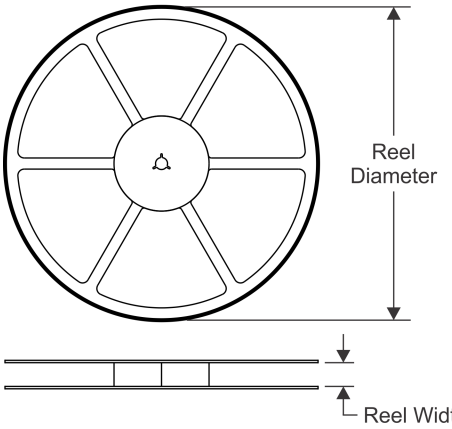
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

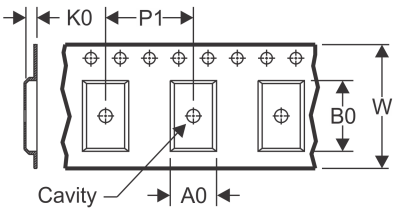
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

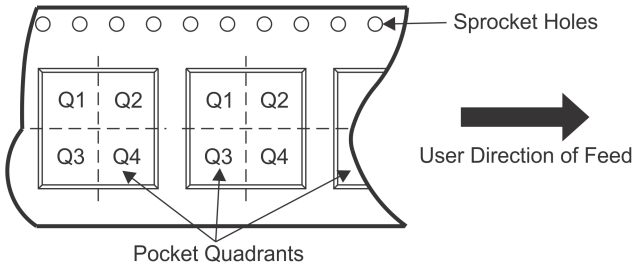


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

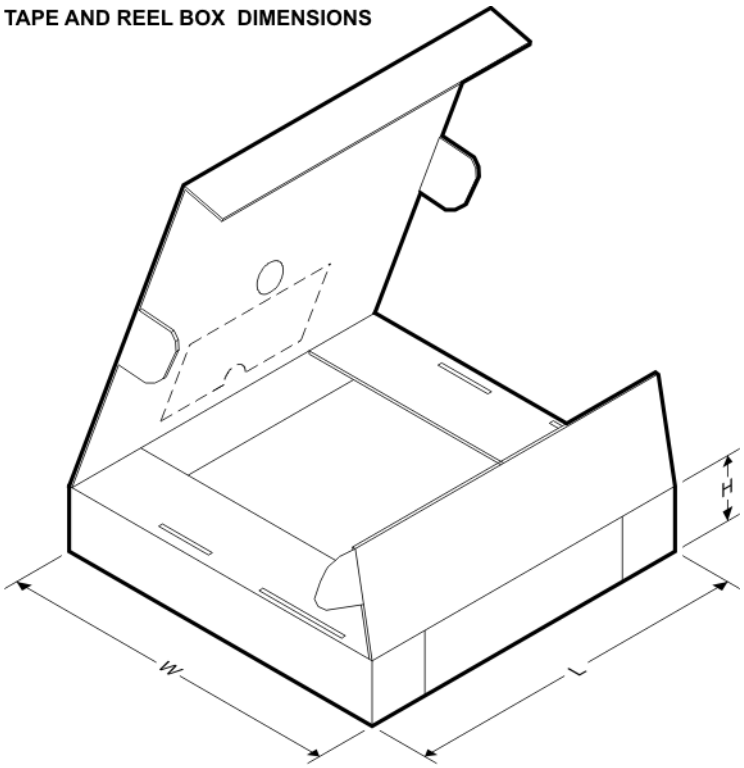
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS51206DSQR	WSON	DSQ	10	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
TPS51206DSQR	WSON	DSQ	10	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
TPS51206DSQT	WSON	DSQ	10	250	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
TPS51206DSQT	WSON	DSQ	10	250	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2

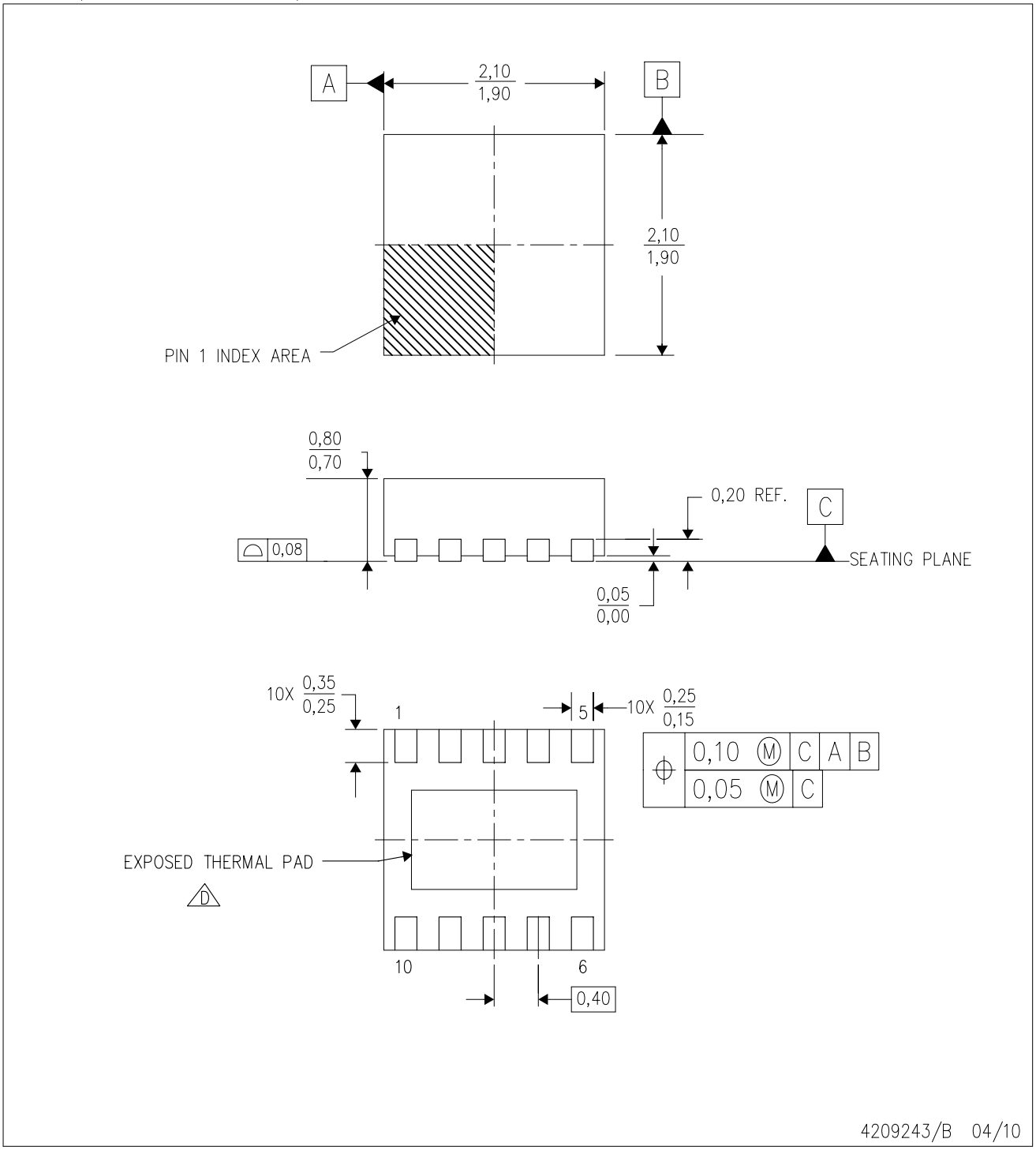
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS51206DSQR	WSON	DSQ	10	3000	210.0	185.0	35.0
TPS51206DSQR	WSON	DSQ	10	3000	210.0	185.0	35.0
TPS51206DSQT	WSON	DSQ	10	250	210.0	185.0	35.0
TPS51206DSQT	WSON	DSQ	10	250	210.0	185.0	35.0

DSQ (S–PWSON–N10) PLASTIC SMALL OUTLINE NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Small Outline No–Lead (SON) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.

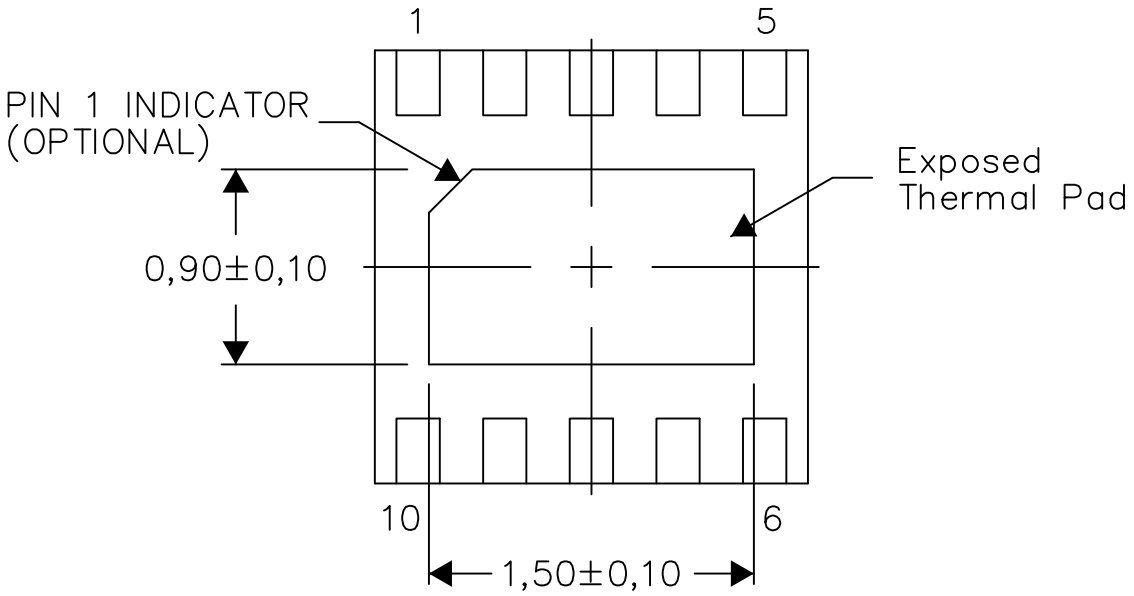
DSQ (R–PWSON–N10) PLASTIC SMALL OUTLINE NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



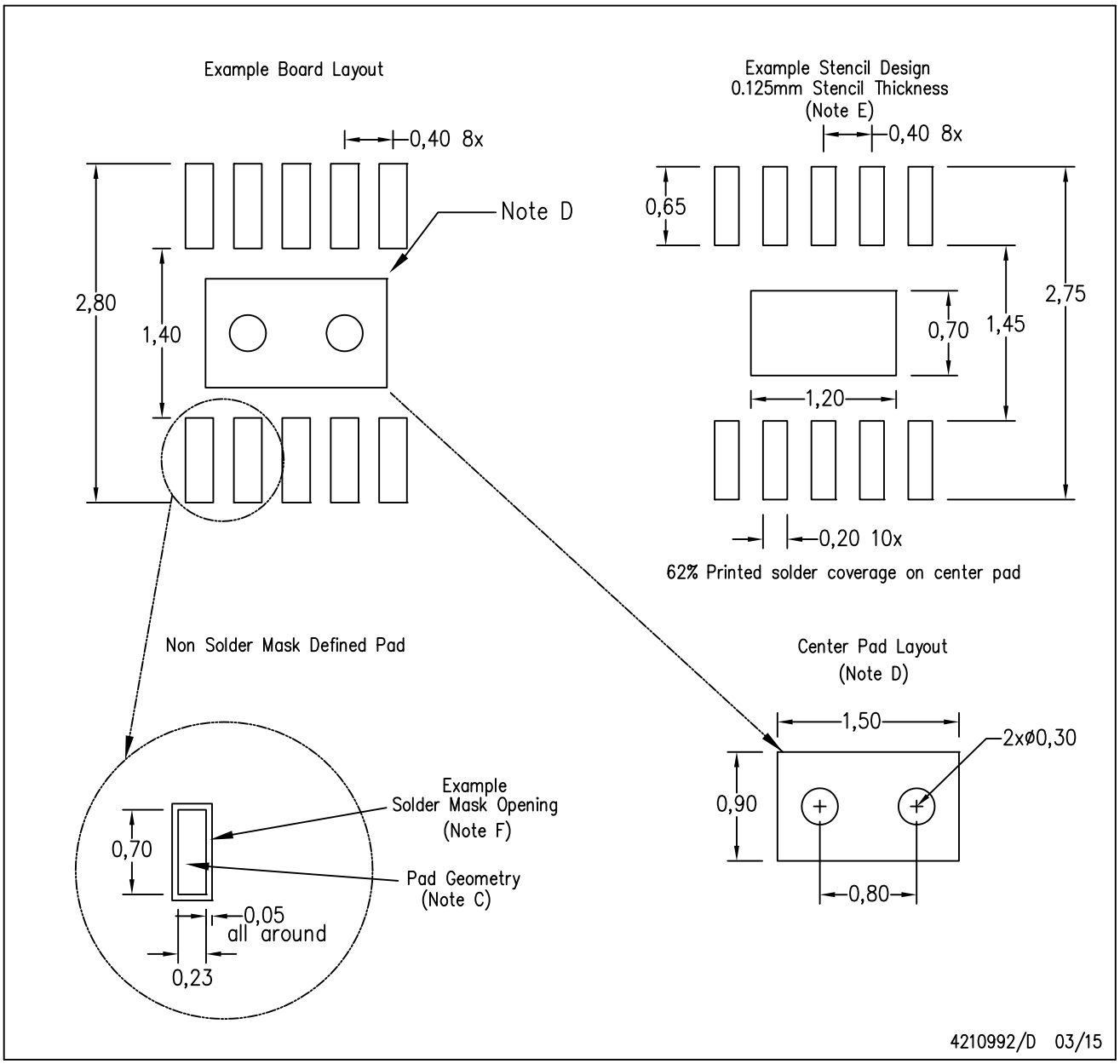
Bottom View

Exposed Thermal Pad Dimensions

4210993/E 06/15

NOTES: A. All linear dimensions are in millimeters

DSQ (R–PWSON–N10) PLASTIC SMALL OUTLINE NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for solder mask tolerances.

重要声明

德州仪器(TI) 及其下属子公司有权根据 JESD46 最新标准, 对所提供的产品和服务进行更正、修改、增强、改进或其它更改， 并有权根据 JESD48 最新标准中止提供任何产品和服务。客户在下订单前应获取最新的相关信息, 并验证这些信息是否完整且是最新的。所有产品的销售都遵循在订单确认时所提供的TI 销售条款与条件。

TI 保证其所销售的组件的性能符合产品销售时 TI 半导体产品销售条件与条款的适用规范。仅在 TI 保证的范围内，且 TI 认为 有必要时才会使用测试或其它质量控制技术。除非适用法律做出了硬性规定，否则没有必要对每种组件的所有参数进行测试。

TI 对应用帮助或客户产品设计不承担任何义务。客户应对其使用 TI 组件的产品和应用自行负责。为尽量减小与客户产品和应 用相关的风险，客户应提供充分的设计与操作安全措施。

TI 不对任何 TI 专利权、版权、屏蔽作品权或其它与使用了 TI 组件或服务的组合设备、机器或流程相关的 TI 知识产权中授予 的直接或隐含权限作出任何保证或解释。TI 所发布的与第三方产品或服务有关的信息，不能构成从 TI 获得使用这些产品或服 务的许可、授权、或认可。使用此类信息可能需要获得第三方的专利权或其它知识产权方面的许可，或是 TI 的专利权或其它 知识产权方面的许可。

对于 TI 的产品手册或数据表中 TI 信息的重要部分，仅在没有对内容进行任何篡改且带有相关授权、条件、限制和声明的情况 下才允许进行复制。TI 对此类篡改过的文件不承担任何责任或义务。复制第三方的信息可能需要服从额外的限制条件。

在转售 TI 组件或服务时，如果对该组件或服务参数的陈述与 TI 标明的参数相比存在差异或虚假成分，则会失去相关 TI 组件 或服务的所有明示或暗示授权，且这是不正当的、欺诈性商业行为。TI 对任何此类虚假陈述均不承担任何责任或义务。

客户认可并同意，尽管任何应用相关信息或支持仍可能由 TI 提供，但他们将独力负责满足与其产品及在其应用中使用 TI 产品 相关的所有法律、法规和安全相关要求。客户声明并同意，他们具备制定与实施安全措施所需的全部专业技术和知识，可预见 故障的危险后果、监测故障及其后果、降低有可能造成人身伤害的故障的发生机率并采取适当的补救措施。客户将全额赔偿因 在此类安全关键应用中使用任何 TI 组件而对 TI 及其代理造成的任何损失。

在某些场合中，为了推进安全相关应用有可能对 TI 组件进行特别的促销。TI 的目标是利用此类组件帮助客户设计和创立其特 有的可满足适用的功能安全性标准和要求的终端产品解决方案。尽管如此，此类组件仍然服从这些条款。

TI 组件未获得用于 FDA Class III（或类似的生命攸关医疗设备）的授权许可，除非各方授权官员已经达成了专门管控此类使 用的特别协议。

只有那些 TI 特别注明属于军用等级或“增强型塑料”的 TI 组件才是设计或专门用于军事/航空应用或环境的。购买者认可并同 意，对并非指定面向军事或航空航天用途的 TI 组件进行军事或航空航天方面的应用，其风险由客户单独承担，并且由客户独 力负责满足与此类使用相关的所有法律和法规要求。

TI 已明确指定符合 ISO/TS16949 要求的产品，这些产品主要用于汽车。在任何情况下，因使用非指定产品而无法达到 ISO/TS16949 要求，TI不承担任何责任。

	产品		应用
数字音频	www.ti.com.cn/audio	通信与电信	www.ti.com.cn/telecom
放大器和线性器件	www.ti.com.cn/amplifiers	计算机及周边	www.ti.com.cn/computer
数据转换器	www.ti.com.cn/dataconverters	消费电子	www.ti.com/consumer-apps
DLP® 产品	www.dlp.com	能源	www.ti.com/energy
DSP - 数字信号处理器	www.ti.com.cn/dsp	工业应用	www.ti.com.cn/industrial
时钟和计时器	www.ti.com.cn/clockandtimers	医疗电子	www.ti.com.cn/medical
接口	www.ti.com.cn/interface	安防应用	www.ti.com.cn/security
逻辑	www.ti.com.cn/logic	汽车电子	www.ti.com.cn/automotive
电源管理	www.ti.com.cn/power	视频和影像	www.ti.com.cn/video
微控制器 (MCU)	www.ti.com.cn/microcontrollers		
RFID 系统	www.ti.com.cn/rfidsys		
OMAP应用处理器	www.ti.com/omap		
无线连通性	www.ti.com.cn/wirelessconnectivity	德州仪器在线技术支持社区	www.deyisupport.com

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265