用于电池供电系统的单芯片电源管理类集成电路 (PMIC)

查询样品: **TPS65217A**, **TPS65217B**, **TPS65217C**, **TPS65217D**

特性

充电器/电源路径

- 电源路径上的 **2A** 输出电流
- 线性充电器；最大充电电流 **700mA**
- 耐压达 **20V** 的 **USB** 和交流输入
- **USB** 输入上的 **100mA**，**500mA**，**1300mA** 或者 **1800mA** 的电流限制
- 热调节、安全定时器
- 温度感测输入

降压转换器 (DCDC1，2，3)

- 具有集成开关场效应晶体管 **(FET)** 的三个降压转换器
  - **1.2A** 时 **DCDC1**：**0.9V-1.8V**
  - **1.2A** 时 **DCDC2**：**0.9V-3.3V**
  - **1.2A** 时 **DCDC3**：**0.9V-1.5V**
- 输入电压范围：**2.7V-5.8V**
- **2.25MHz** 固定频率工作
- 轻载电流状态下的节电模式
- 脉宽调制 **(PWM)** 模式中的输出电压精度为 **±2.0%**
- 针对最低压降的 **100%** 占空比
- 每转换器的静态电流典型值为 **15μA**
- 当被禁用时对地被动放电

低压降稳压器 (LDO)(LDO1，2)

- **2** 个可调节 **LDO**
  - **100mA** 时，**LDO1**：**1.0V-3.3V**（缺省值 **1.8V**）
  - **100mA** 时，**LDO2**：**0.9V-3.3V**（缺省值 **3.3V**）
- 输入电压范围：**1.8V-5.8V**
- **LDO2** 可被配置为跟踪 **DCDC3**
- 静态电流典型值为 **15μA**

负载开关 (LDO3，4)

- **2** 个可被配置为 **LDO** 的独立负载开关
- 当被配置为开关时：
  - 输入电压范围：**1.8V-5.8V**
  - 开关阻抗 **300mΩ**（典型值）
  - 流限 **200mA**
  - 当被禁用时对地被动放电
- 当被配置为 **LDO** 时：
  - **LDO** 输出电压范围：**1.5V-3.3V**
  - 输入电压范围：**2.7V-5.8V**
  - 流限 **200mA (TPS65217A，B)**
  - 流限 **400mA (TPS65217C，D)**
  - 当被禁用时对地被动放电

白色发光二极管 (WLED) 驱动器

- 用于亮度控制的内部生成 **PWM**
- **38V** 开 **LED** 保护
- 在每个 **LED** 电流为 **25mA** 时，可支持两串多达 **10** 个 **LED**
- 内部低侧电流吸收

保护

- 欠压闭锁和电池故障比较器
- 常开按钮监视器
- 硬件复位引脚
- 受密码保护 **I²C®** 寄存器

接口

- **I²C** 接口（地址 **0x24**）
- 受密码保护的**I²**寄存器

封装

- 采用 **6mm x 6mm**，**48** 引脚四方扁平无引线封装 **(QFN)**

应用范围

- **AM335x ARM® Cortex™-A8** 微处理器
- 便携式导航系统
- 平板电脑
- **5V** 工业用设备

English Data Sheet: SLVSB64

说明

TPS65217 是一款单芯片电源管理 IC，此 IC 特别设计用于支持便携式和 5V，非便携式应用中的 AM335x 系列应用处理器。 它为单节锂离子电池和锂聚合物电池、双输入电源路径、三个降压转化器、四个 LDO 提供一个线性电池充电器，并提供一个高效升压转换器为每串多达 10 个 LED 的 2 串 LED 供电。 此系统可由 USB 端口，5V 交流适配器，或者锂离子电池的任意组合供电。 此器件的额定运行温度范围为 -40°C 至 +105°C ，这使得它适合于工业应用。 三个高效 2.25MHz 降压转换器为一个基于处理器的系统提供内核电压、存储器、和/或者 I/O 电压。

为了在最大可能的负载电流范围内实现最大效率，它们在轻负载时进入低功率模式。 对于低噪音应用，通过使用 I^2C 接口，这个器件能被强制进入固定频率 PWM。 此降压转换器允许使用小型电感器和电容器以实现一个小型解决方案尺寸。

LDO1 和 LDO2 是为了支持系统待机模式。 SLEEP（睡眠）状态时，输出电流被限制在
1mA 以减少静态电流，而在正常模式下，它们每个都可以支持高达 100mA 的电流。 LDO3 和 LDO4 每个可以支持高达 200mA 的电流并可被配置为负载开关而不是稳压器。 所有 4 个 LDO 都有一个宽泛的输入电压范围，这个电压范围使得它们能够由 DCDC 转换器中的一个供电或者直接由系统电压结点供电。

在默认情况下，只有 LDO1 一直打开 (ON)，但是任何一个电源轨可被配置成保持在睡眠状态。 特别是 DCDC 转换器可继续处于一个低功率脉冲频率调制 (PFM) 模式以支持处理器暂停模式。

TPS65217 提供灵活的加电和断电排序和几个诸如电源正常输出、按钮监视器，硬件复位功能和温度传感器的内务功能以保护电池。

TPS65217A 支持 ZCE 封装内的 AM335x 处理器，此封装不支持 DVFS（动态电压和频率缩放）。 在这个封装内，VDD_MPU 和 VDD_CORE 电源短接在一起并且只需要一个单电源轨。 为了给 DDR2 内存供电，DCDC1 输出电压被设定在 1.8V。 TPS65217B 面向 ZCZ 封装内的 AM335x 处理器，此封装支持 DVFS 并需要用于 VDD_MPU 和 VDD_CORE 电源轨的专用 DCDC 转换器。 为了给 DDR2 内存供电，DCDC1 输出电压被设定在 1.8V。 TPS65217C 用于采用 ZCZ 封装的 AM335x 处理器，但是为了给 DDR3 内存供电，DCDC1 输出电压被设定在 1.5V。 LDO3 被设定在 1.8V 且支持高达 400mA 的电流。 细节请参见应用注释（文献号：SLVU551）。

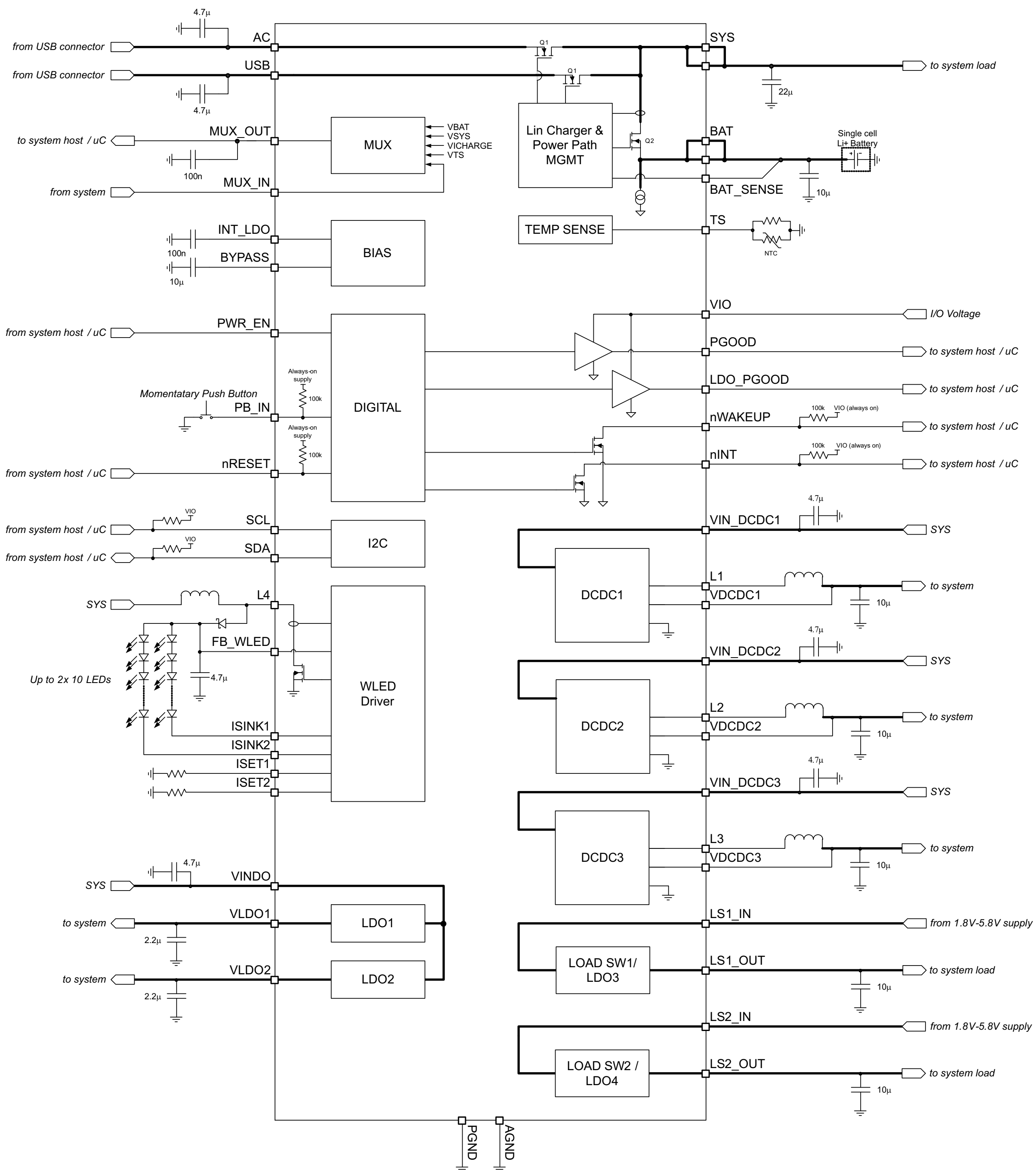
TPS65217D 与 TPS65217C 完全一样，唯一的区别是 DCDC1 输出电压的缺省值为 1.35V，以支持 DDR3L 存储器。

TPS65217A，TPS65217B，TPS65217C 和 TPS65217D 采用焊球间距为 0.4mm 的 48 引脚无引线封装 (6mm x 6mm QFN)。

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

FUNCTIONAL BLOCK DIAGRAM



ORDERING INFORMATION(1)

T_A	PACKAGE	ORDERABLE PART NUMBER(2)	TOP-SIDE MARKING
-40°C to 105°C	RSL	TPS65217ARSL	TPS65217A
		TPS65217BRSL	TPS65217B
		TPS65217CRSL	TPS65217C
		TPS65217DRSL	TPS65217D

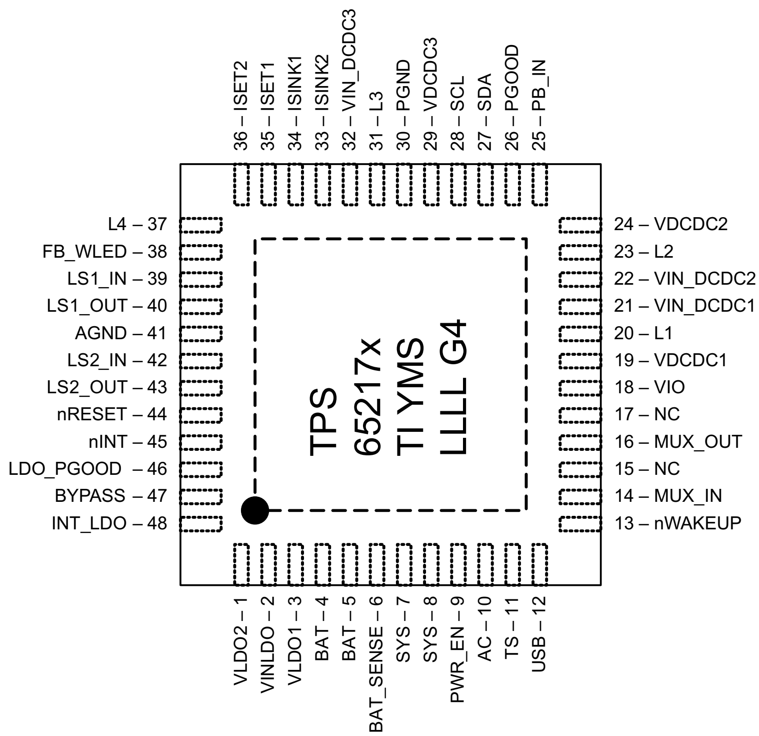
(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.
(2) The RSL package is available in tape and reel. Add R suffix (TPS65217xRSL**R**) to order quantities of 2500 parts per reel or suffix T (TPS65217xRSL**T**) to order quantities of 250 parts per reel.

	TPS65217A (Targeted at AM335x - ZCE)		TPS65217B (Targeted at AM335x - ZCZ)		TPS65217C (Targeted at AM335x - ZCZ)		TPS65217D (Targeted at AM335x - ZCZ)	
	VOLTAGE (V)	SEQUENCE (STROBE)	VOLTAGE (V)	SEQUENCE (STROBE)	VOLTAGE (V)	SEQUENCE (STROBE)	VOLTAGE (V)	SEQUENCE (STROBE)
DCDC1	1.8	1	1.8	1	1.5	1	1.35	1
DCDC2	3.3	2	1.1	5	1.1	5	1.1	5
DCDC3	1.1	3	1.1	5	1.1	5	1.1	5
LDO1(1)	1.8	15	1.8	15	1.8	15	1.8	15
LDO2	3.3	2	3.3	2	3.3	3	3.3	3
LS1/LDO3	Load switch	1	3.3 (LDO, 200 mA)	3	1.8 (LDO, 400 mA)	2	1.8 (LDO, 400 mA)	2
LS2/LDO4	Load switch	4	3.3 (LDO, 200 mA)	4	3.3 (LDO, 400 mA)	4	3.3 (LDO, 400 mA)	4

(1) Strobe 15 (LDO1) is the first rail to be enabled in a sequence, followed by strobe 1-7. See “Wake-Up and Power Up Sequencing” section for details.

DEVICE INFORMATION

RSL PACKAGE
(TOP VIEW)



x = CHIP DESIGNATOR (A, B, or C)
TI = TI LETTERS
YM = YEAR / MONTH DATE CODE
LLLL = LOT TRACE CODE
S = ASSEMBLY SITE CODE

O = Pin 1 (MARKED)

48-PIN 6mm x 6mm x 1mm QFN

TERMINAL FUNCTIONS

TERMINAL		I/O	DESCRIPTION
NAME	NO.		
VLDO2	1	O	Output voltage of LDO2
VINLDO	2	I	Input voltage for LDO1 and LDO2
VLDO1	3	O	Output voltage of LDO1
BAT	4, 5	I/O	Battery charger output. Connect to battery.
BAT_SENSE	6	I	Battery voltage sense input, connect to BAT directly at the battery terminal.
SYS	7, 8	O	System voltage pin and output of the power path. All voltage regulators are typically powered from this output.
PWR_EN	9	I	Enable input for DCDC1, 2, 3 converters and LDO1, 2, 3, 4. Pull this pin high to start the power-up sequence.
AC	10	I	AC adapter input to power path. Connect to an external DC supply.
TS	11	I	Temperature sense input. Connect to NTC thermistor to sense battery temperature. Works with 10k and 100k thermistors. See charger section for details.
USB	12	I	USB voltage input to power path. Connect to external voltage from a USB port.
nWAKEUP	13	O	Signal to host to indicate a power on event (active low, open-drain output)
MUX_IN	14	O	Input to analog multiplexer
NC	15		Not used
MUX_OUT	16	O	Output pin of analog multiplexer
NC	17		Not used
VIO	18	I	Output-high supply for output buffers
VDCDC1	19	I	DCDC1 output/ feedback voltage sense input

TERMINAL		I/O	DESCRIPTION
NAME	NO.		
L1	20	O	Switch pin for DCDC1. Connect to inductor.
VIN_DCDC1	21	I	Input voltage for DCDC1. Must be connected to SYS pin.
VIN_DCDC2	22	I	Input voltage for DCDC2. Must be connected to SYS pin.
L2	23	O	Switch pin for DCDC2. Connect to inductor.
VDCDC2	24	O	DCDC2 output/feedback voltage sense input
PB_IN	25	I	Push-button monitor input. Typically connected to a momentary switch to ground (active low).
PGOOD	26	O	Power-good output (push/pull output). Pulled low when any of the power rails are out of regulation. Behavior is register programmable.
SDA	27	I/O	Data line for the I^2C interface
SCL	28	I	Clock input for the I^2C interface
VDCDC3	29	O	DCDC3 output/feedback voltage sense input
PGND	30		Power ground. Connect to ground plane.
L3	31	O	Switch pin for DCDC3. Connect to Inductor.
VIN_DCDC3	32	I	Input voltage for DCDC3. Must be connected to SYS pin.
ISINK2	33	I	Input to the WLED current SINK2. Connect to the cathode of the WLED string. Current through SINK1 equals current through ISINK2. If only one WLED string is used, short ISINK1 and ISINK2 together.
ISINK1	34	I	Input to the WLED current SINK1. Connect to the cathode of the WLED string. Current through SINK1 equals current through ISINK2. If only one WLED string is used, short ISINK1 and ISINK2 together.
ISET1	35	I	Low-level WLED current set. Connect a resistor to ground to set the WLED low-current level.
ISET2	36	I	High-level WLED current set. Connect a resistor to ground to set the WLED high-current level.
L4	37	O	Switch Pin of the WLED boost converter. Connected to Inductor.
FB_WLED	38	I	Feedback pin for WLED boost converter. Also connected to the Anode of the WLED strings.
LS1_IN	39	I	Input voltage pin for load switch 1/LDO3
LS1_OUT	40	O	Output voltage pin for load switch 1/LDO3
AGND	41	POWER	Analog GND, connect to PGND (PowerPad)
LS2_IN	42	I	Input voltage pin for load switch 2/LDO4
LS2_OUT	43	O	Output voltage pin for load switch 2/LDO4
nRESET	44	I	Reset pin (active low). Pull this pin low and the PMIC will shut down, and after 1s power-up in its default state.
nINT	45	O	Interrupt output (active low, open drain). Pin is pulled low if an interrupt bit is set. The output goes high after the bit causing the interrupt in register INT has been read. The interrupt sources can be masked in register INT, so no interrupt is generated when the corresponding interrupt bit is set.
LDO_PGOOD	46	O	LDO power good (LDO1 and LDO2 only, push/pull output). Pulled low when either LDO1 or LDO2 is out of regulation.
BYPASS	47	O	Internal bias voltage (2.25 V). It is not recommended to connect any external load to this pin.
INT_LDO	48	O	Internal bias voltage (2.30 V). It is not recommended to connect any external load to this pin.
POWERPAD		POWER	Power ground connection for the PMU. Connect to GND

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted) [1][2]

			VALUE	UNIT
	Supply voltage range (with respect to PGND)	BAT	-0.3 to 7	V
		USB, AC	-0.3 to 20	
	Input/Output voltage range (with respect to PGND)	All pins unless specified separately	-0.3 to 7	V
		ISINK	-0.3 to 20	
		L4, FB_WLED	-0.3 to 44	
	Absolute voltage difference between SYS and any VIN_DCDCx pin or SYS and VINLDO		0.3	V
	Terminal current	SYS, USB, BAT	3000	mA
	Source or Sink current	PGOOD, LDO_PGOOD	6	mA
	Sink current	nWAKEUP, nINT	2	mA
θ_{JA}	Junction-to-ambient thermal resistance	JEDEC 4-layer high-K board	30	°C/W
T_J	Operating junction temperature		125	°C
T_A	Operating ambient temperature		-40 to 105	°C
T_{stg}	Storage temperature		-65 to 150	°C
	ESD rating	(HBM) Human body model	±2000	V
		(CDM) Charged device model	±500	

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions is not implied. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to network ground terminal.

RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
Supply voltage, USB, AC		4.3		5.8	V
Supply voltage, BAT		2.75		5.5	V
Input current from AC				2.5	A
Input current from USB				1.3	A
Battery current				2	A
Input voltage range for DCDC1, DCDC2, and DCDC3		2.7		5.8	V
Input voltage range for LDO1, LDO2		1.8		5.8	V
Input voltage range for LS1/LDO, LS2/LDO4 configured as LDOs		2.7		5.8	V
Input voltage range for LS1/LDO, LS2/LDO4 configured as load switches		1.8		5.8	V
Output voltage range for LDO1		1.0		3.3	V
Output voltage range for LDO2		0.9		3.3	V
Output voltage range for LS1/LDO3, LS2/LDO4		1.8		3.3	V
Output current DCDC1		0		1.2	A
Output current DCDC2		0		1.2	A
Output current DCDC3		0		1.2	A
Output current LDO1, LDO2		0		250	mA
Output current LS1/LDO3, LS2/LDO4 configured as LDOs	TPS65217A	0		200	mA
	TPS65217B	0		200	
	TPS65217C	0		400	
	TPS65217D	0		400	
Output current LS1/LDO, LS2/LDO4 configured as load switches		0		200	mA

ELECTRICAL CHARACTERISTICS

V_{BAT} = 3.6 V ±5%, T_J = 27ºC (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
INPUT VOLTAGE AND CURRENTS							
V_{BAT}	Battery input voltage range	USB or AC supply connected		0		5.5	V
		USB and AC not connected		2.75		5.5	
V_{AC}	AC adapter input voltage range	Valid range for charging		4.3		5.8	V
V_{USB}	USB input voltage range	Valid range for charging		4.3		5.8	V
V_{UVLO}	Under voltage lock-out	Measured in respect to V_{BAT}; supply falling; V_{AC} = V_{USB} = 0 V	UVLO[1:0] = 00		2.73		V
			UVLO[1:0] = 01		2.89		
			UVLO[1:0] = 10		3.18		
			UVLO[1:0] = 11		3.3		
	Accuracy			-2		2	%
	Deglitch time	Not tested in production		4		6	ms
V_{OFFSET}	AC/USB UVLO offset	V_{BAT} < V_{UVLO}; Device shuts down when V_{AC}, V_{USB} drop below V_{UVLO} + V_{OFFSET}			200		mV
I_{OFF}	OFF current, Total current into VSYS, VINDCDCx, VINLDO	All rails disabled, T_A = 27°C			6		µA
I_{SLEEP}	Sleep current, Total current into VSYS, VINDCDCx, VINLDO	LDO1 and LDO2 enabled, no load. All other rails disabled. V_{SYS} = 4 V, T_A = 0.105°C			80	106	µA
POWER PATH USB/AC DETECTION LIMITS							
$V_{IN(DT)}$	AC/USB voltage detection threshold	V_{BAT} > V_{UVLO}	AC/USB valid when $V_{AC/USB}$ - V_{BAT} > $V_{IN(DT)}$	190			mV
		V_{BAT} < V_{UVLO}	AC/USB valid when $V_{AC/USB}$ > $V_{IN(DT)}$	4.3			V
$V_{IN(NDT)}$	AC/USB voltage removal detection threshold	V_{BAT} > V_{UVLO}	AC/USB invalid when $V_{AC/USB}$ - V_{BAT} < $V_{IN(DT)}$			125	mV
		V_{BAT} < V_{UVLO}	AC/USB invalid when $V_{AC/USB}$ < $V_{IN(DT)}$		V_{UVLO} + V_{OFFSET}		V
T_{RISE}	VAC, VUSB rise time	Voltage rising from 100 mV to 4.5 V. If rise time is exceeded, device may not power-up.				50	ms
$T_{DG(DT)}$	Power detected deglitch	AC or USB voltage increasing; Not tested in production			22.5		ms
$V_{IN(OVP)}$	Input over voltage detection threshold	USB and AC input		5.8	6	6.4	V
POWER PATH TIMING							
$T_{SW(PSEL)}$	Switching from AC to USB	Not tested in production				150	µs
POWER PATH MOSFET CHARACTERISTICS							
$V_{DO,\ AC}$	AC input switch dropout voltage	IAC[1:0] = 11 (2.5 A), I_{SYS} = 1 A			150		mV
$V_{DO,\ USB}$	USB input switch dropout voltage	IUSB[1:0] = 01 (500 mA), I_{SYS} = 500 mA			100		mV
		IUSB[1:0] = 10 (1300 mA), I_{SYS} = 800 mA			160		
$V_{DO,\ BAT}$	Battery switch dropout voltage	V_{BAT} = 3 V, I_{BAT} = 1 A			60		mV

ELECTRICAL CHARACTERISTICS (continued)

V_{BAT} = 3.6 V ±5%, T_J = 27ºC (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER PATH INPUT CURRENT LIMITS						
I_{ACLMT}	Input current limit; AC pin	IAC[1:0] = 00	90		130	mA
		IAC[1:0] = 01	480		580	
		IAC[1:0] = 10	1000	1500		
		IAC[1:0] = 11	2000	2500		
I_{USBLMT}	Input current limit; USB pin	IUSB[1:0] = 00	90		100	mA
		IUSB[1:0] = 01	460		500	
		IUSB[1:0] = 10	1000	1300		
		IUSB[1:0] = 11	1500	1800		
I_{BAT}	Battery load current	Not tested in production			2	A
POWER PATH BATTERY SUPPLEMENT DETECTION						
V_{BSUP}	Battery supplement threshold	V_{SYS} ≤ V_{BAT} - VBSUP1, V_{SYS} falling IUSB[1:0] = 10		40		mV
	Hysteresis	V_{SYS} rising		20		
POWER PATH BATTERY PROTECTION						
$V_{BAT(SC)}$	BAT pin short-circuit detection threshold		1.3	1.5	1.7	V
$I_{BAT(SC)}$	Source current for BAT pin short-circuit detection			7.5		mA
INPUT BASED DYNAMIC POWER MANAGEMENT						
V_{DPM}	Threshold at which DPPM loop is enabled	I^2C selectable	3.5		4.25	V
BATTERY CHARGER						
V_{OREG}	Battery charger voltage	I^2C selectable	4.10		4.45	V
	Accuracy		-2		1	%
V_{LOWV}	Pre-charge to fast-charge transition threshold	VPRECHG = 0		2.9		V
		VPRECHG = 1		2.5		
$t_{DGL1(LOWV)}$	Deglitch time on pre-charge to fast-charge transition	Not tested in production		25		ms
$t_{DGL2(LOWV)}$	Deglitch time on fast-charge to pre-charge transition	Not tested in production		25		ms
I_{CHG}	Battery fast charge current range V_{OREG} > V_{BAT} > V_{LOWV}, V_{IN} = V_{USB} = 5 V	ICHRG[1:0] = 00		300		mA
		ICHRG[1:0] = 01		400		
		ICHRG[1:0] = 10	450	500	550	
		ICHRG[1:0] = 11		700		
I_{PRECHG}	Pre-charge current	ICHRG[1:0] = 00		30		mA
		ICHRG[1:0] = 01		40		
		ICHRG[1:0] = 10	25	50	75	
		ICHRG[1:0] = 11		70		
I_{TERM}	Charge current value for termination detection threshold (fraction of I_{CHG})	TERMIF[1:0] = 00		2.5		%
		TERMIF[1:0] = 01	3	7.5	10	
		TERMIF[1:0] = 10		15		
		TERMIF[1:0] = 11		18		
$t_{DGL(TERM)}$	Deglitch time, termination detected	Not tested in production		125		ms
V_{RCH}	Recharge detection threshold	Voltage below V_{OREG}	150	100	70	mV
$t_{DGL(RCH)}$	Deglitch time, recharge threshold detected	Not tested in production		125		ms
$I_{BAT(DET)}$	Sink current for battery detection	T_J = 27°C	3	7.5	10	mA
t_{DET}	Battery detection timer. $I_{BAT(DET)}$ is pulled from the battery for t_{DET}. If BAT voltage remains above V_{RCH} threshold the battery is connected.	V_{BAT} < $V_{RCH;}$ Not tested in production		250		ms
T_{CHG}	Charge safety timer	Safety timer range, thermal and DPM not active, selectable by I^2C; Not tested in production	4		8	h

ELECTRICAL CHARACTERISTICS (continued)

V_{BAT} = 3.6 V ±5%, T_J = 27ºC (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
T_{PRECHG}	Precharge timer	Pre charge timer, thermal and DPM/DPPM loops not active, selectable by I^2C; Not tested in production	PCHRGT = 0		30	60	min
			PCHRGT = 1		60		
BATTERY NTC MONITOR							
T_{THON}	Thermistor power on time at charger off, sampling mode on				10		ms
T_{THOFF}	Thermistor power sampling period at charger off, sampling mode on				1		s
R_{NTC_PULL}	Pull-up resistor from thermistor to Internal LDO . I2C selectable	NTC_TYPE = 1 (10k NTC)			7.35		kΩ
		NTC_TYPE = 0 (100K NTC)			60.5		
	Accuracy	T_A = 27°C		-3		3	%
V_{LTF}	Low temp failure threshold	Temperature falling			1660		mV
		Temperature rising			1610		
V_{HTF}	High temp failure threshold	Temperature falling	TRANGE = 0		910		mV
		Temperature rising			860		
		Temperature falling	TRANGE = 1		667		
		Temperature rising			622		
V_{DET}	Thermistor detection threshold			1750		1850	mV
t_{BATDET}	Thermistor not detected. Battery not present deglitch.	Not tested in production			26		ms
THERMAL REGULATION							
$T_{J(REG)}$	Temperature regulation limit	Temperature at which charge current is reduced		111		123	°C
DCDC1 (BUCK)							
V_{IN}	Input voltage range	VIN_DCDC1 pin		2.7		V_{SYS}	V
$I_{Q,SLEEP}$	Quiescent current in SLEEP mode	No load, V_{SYS} = 4 V, T_A = 25°C			30		μA
V_{OUT}	Output voltage range	External resistor divider (XADJ1 = 1)		0.6		V_{IN}	V
		I^2C selectable in 25-mV steps (XADJ1 = 0)		0.9		1.8 (1)	
	DC output voltage accuracy	V_{IN} = V_{OUT} + 0.3 V to 5.8 V; 0 mA ≤ I_{OUT} ≤ 1.2 A		-2		3	%
	Power save mode (PSM) ripple voltage	I_{OUT} = 1 mA, PFM mode L = 2.2 μH, C_{OUT} = 20 μF			40		mV_{pp}
I_{OUT}	Output current range			0		1.2	A
$R_{DS(ON)}$	High side MOSFET on-resistance	V_{IN} = 2.7 V			170		mΩ
	Low side MOSFET on-resistance	V_{IN} = 2.7 V			120		
I_{LEAK}	High side MOSFET leakage current	V_{IN} = 5.8 V				2	μA
	Low side MOSFET leakage current	V_{DS} = 5.8 V				1	
I_{LIMIT}	Current limit (high and low side MOSFET).	2.7 V < V_{IN} < 5.8 V			1.6		A
f_{SW}	Switching frequency			1.95	2.25	2.55	MHz
V_{FB}	Feedback voltage	XADJ = 1			600		mV
t_{SS}	Soft-start time	Time to ramp V_{OUT} from 5% to 95%, no load			750		μs
R_{DIS}	Internal discharge resistor at L1 (2)				250		Ω
L	Inductor			1.5	2.2		μH
C_{OUT}	Output capacitor	Ceramic		10	22		μF
	ESR of output capacitor				20		mΩ
DCDC2 (BUCK)							
V_{IN}	Input voltage range	VIN_DCDC2 pin		2.7		V_{SYS}	V
$I_{Q,SLEEP}$	Quiescent current in SLEEP mode	No load, V_{SYS} = 4 V, T_A = 25°C			30		μA

(1) Contact factory for 3.3-V option.
(2) Can be factory disabled.

ELECTRICAL CHARACTERISTICS (continued)

V_{BAT} = 3.6 V ±5%, T_J = 27ºC (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OUT}	Output voltage range	External resistor divider (XADJ2 = 1)	0.6		V_{IN}	V
		I^2C selectable in 25-mV steps (XADJ2 = 0)	0.9		3.3	
	DC output voltage accuracy	$V_{IN} = V_{OUT}$ + 0.3 V to 5.8 V; 0 mA ≤ I_{OUT} ≤ 1.2 A	-2		3	%
	Power save mode (PSM) ripple voltage	I_{OUT} = 1 mA, PFM mode L = 2.2 µH, C_{OUT} = 20 µF		40		mV_{pp}
I_{OUT}	Output current range		0		1.2	A
$R_{DS(ON)}$	High side MOSFET on-resistance	V_{IN} = 2.7 V		170		mΩ
	Low side MOSFET on-resistance	V_{IN} = 2.7 V		120		
I_{LEAK}	High side MOSFET leakage current	V_{IN} = 5.8 V			2	µA
	Low side MOSFET leakage current	V_{DS} = 5.8 V			1	
I_{LIMIT}	Current limit (high and low side MOSFET).	2.7 V < V_{IN} < 5.8 V		1.6		A
f_{SW}	Switching frequency		1.95	2.25	2.55	MHz
V_{FB}	Feedback voltage	XADJ = 1		600		mV
t_{SS}	Soft-start time	Time to ramp V_{OUT} from 5% to 95%, no load		750		µs
R_{DIS}	Internal discharge resistor at L2			250		Ω
L	Inductor		1.5	2.2		µH
C_{OUT}	Output capacitor	Ceramic	10	22		µF
	ESR of output capacitor			20		mΩ
DCDC3 (BUCK)						
V_{IN}	Input voltage range	VIN_DCDC3 pin	2.7		V_{SYS}	V
$I_{Q,SLEEP}$	Quiescent current in SLEEP mode	No load, V_{SYS} = 4 V, T_A = 25°C		30		µA
V_{OUT}	Output voltage range	External resistor divider (XADJ3 = 1)	0.6		V_{IN}	V
		I^2C selectable in 25-mV steps (XADJ3 = 0)	0.9		1.5(3)	
	DC output voltage accuracy	$V_{IN} = V_{OUT}$ + 0.3 V to 5.8 V; 0 mA ≤ I_{OUT} ≤ 1.2 A	-2		3	%
	Power save mode (PSM) ripple voltage	I_{OUT} = 1 mA, PFM mode L = 2.2 µH, C_{OUT} = 20 µF		40		mV_{pp}
I_{OUT}	Output current range		0		1.2	A
$R_{DS(ON)}$	High side MOSFET on-resistance	V_{IN} = 2.7 V		170		mΩ
	Low side MOSFET on-resistance	V_{IN} = 2.7 V		120		
I_{LEAK}	High side MOSFET leakage current	V_{IN} = 5.8 V			2	µA
	Low side MOSFET leakage current	V_{DS} = 5.8 V			1	
I_{LIMIT}	Current limit (high and low side MOSFET).	2.7 V < V_{IN} < 5.8 V		1.6		A
f_{SW}	Switching frequency		1.95	2.25	2.55	MHz
V_{FB}	Feedback voltage	XADJ = 1		600		mV
t_{SS}	Soft-start time	Time to ramp V_{OUT} from 5% to 95%, no load		750		µs
R_{DIS}	Internal discharge resistor at L1, L2			250		Ω
L	Inductor		1.5	2.2		µH
C_{OUT}	Output capacitor	Ceramic	10	22		µF
	ESR of output capacitor			20		mΩ
LDO1, LDO2						
V_{IN}	Input voltage range		1.8		5.8	V
$I_{Q,SLEEP}$	Quiescent current in SLEEP mode	No load, V_{SYS} = 4 V, T_A = 25°C		5		µA

(3) Contact factory for 3.3-V option.

ELECTRICAL CHARACTERISTICS (continued)

V_{BAT} = 3.6 V ±5%, T_J = 27ºC (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{OUT}	Output voltage range	LDO1, I^2C selectable		1.0		3.3	V
		LDO2, I^2C selectable		0.9		3.3	
	DC output voltage accuracy	I_{OUT} = 10 mA, V_{IN} > V_{OUT} + 200 mV, V_{OUT} > 0.9 V		-2		2	%
	Line regulation	V_{IN} = 2.7 V - 5.5 V, V_{OUT} = 1.2 V, I_{OUT} = 100 mA		-1		1	
	Load regulation	I_{OUT} = 1 mA - 100 mA, V_{OUT} = 1.2 V, V_{IN} = 3.3 V		-1		1	
		I_{OUT} = 0 mA - 1 mA, V_{OUT} = 1.2 V, V_{IN} = 3.3 V		-2.5		2.5	
I_{OUT}	Output current range	Sleep state		0		1	mA
		Active state		0		100	
I_{SC}	Short circuit current limit	Output shorted to GND		100	250		mA
V_{DO}	Dropout voltage	I_{OUT} = 100 mA, V_{IN} = 3.3 V				200	mV
R_{DIS}	Internal discharge resistor at output				430		Ω
C_{OUT}	Output capacitor	Ceramic			2.2		µF
	ESR of output capacitor				20		mΩ
LS1/LDO3 & LS2/LDO4, CONFIGURED AS LDOs							
V_{IN}	Input voltage range			2.7		5.8	V
$I_{Q,SLEEP}$	Quiescent current in SLEEP mode	No load, V_{SYS} = 4 V, T_A = 25°C			30		µA
V_{OUT}	Output voltage range	LS1LDO3 = 1, LS2LDO4 =1 I^2C selectable		1.5		3.3	V
	DC output voltage accuracy	I_{OUT} = 10 mA, V_{IN} > V_{OUT} + 200 mV, V_{OUT} > 1.8 V		-2		2	%
	Line regulation	V_{IN} = 2.7 V - 5.5 V, V_{OUT} = 1.8 V, I_{OUT} = 200 mA		-1		1	
	Load regulation	I_{OUT} = 1 mA - 200 mA, V_{OUT} = 1.8 V, V_{IN} = 3.3 V		-1		1	
I_{OUT}	Output current range	TPS65217A		0		200	mA
		TPS65217B		0		200	
		TPS65217C		0		400	
		TPS65217D		0		400	
I_{SC}	Short circuit current limit	Output shorted to GND	TPS65217A	200	280		mA
			TPS65217B	200	280		
			TPS65217C	400	480		
			TPS65217D	400	480		
V_{DO}	Dropout voltage	I_{OUT} = 200 mA, V_{IN} = 3.3 V				200	mV
R_{DIS}	Internal discharge resistor at output(4)				375		Ω
C_{OUT}	Output capacitor	Ceramic		8	10	12	µF
	ESR of output capacitor				20		mΩ

(4) Can be factory disabled.

ELECTRICAL CHARACTERISTICS (continued)

V_{BAT} = 3.6 V ±5%, T_J = 27ºC (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
LS1/LDO3 & LS2/LDO4, CONFIGURED AS LOAD SWITCHES						
V_{IN}	Input voltage range	LS1_VIN, LS2_VIN pins	1.8		5.8	V
$R_{DS(ON)}$	P-channel MOSFET on-resistance	V_{IN} = 1.8 V, over full temperature range		300	650	mΩ
I_{SC}	Short circuit current limit	Output shorted to GND	200	280		mA
R_{DIS}	Internal discharge resistor at output			375		Ω
C_{OUT}	Output capacitor	Ceramic	1	10	12	µF
	ESR of output capacitor			20		mΩ
WLED BOOST						
V_{IN}	Input voltage range		2.7		5.8	V
V_{OUT}	Max output voltage	I_{SINK} = 20 mA	32			V
V_{OVP}	Output over-voltage protection		37	38	39	V
$R_{DS(ON)}$	N-channel MOSFET on-resistance	V_{IN} = 3.6 V		0.6		Ω
I_{LEAK}	N-channel leakage current	V_{DS} = 25 V, T_A = 25°C		2		µA
I_{LIMIT}	N-channel MOSFET current limit			1.6	1.9	A
f_{SW}	Switching frequency			1.125		MHz
I_{INRUSH}	Inrush current on start-up	V_{IN} = 3.6 V, 1% duty cycle setting		1.1		A
		V_{IN} = 3.6 V, 100% duty cycle setting		2.1		
L	Inductor			18		µH
C_{OUT}	Output capacitor	Ceramic		4.7		µF
	ESR of output capacitor			20		mΩ
WLED CURRENT SINK1, SINK2						
$V_{SINK1,2}$	Over-voltage protection threshold at ISINK1, ISINK2 pins				19	V
$V_{DO,\ SINK1,2}$	Current sink drop-out voltage	Measured from ISINK to GND		400		mV
$V_{ISET1,2}$	ISET1, ISET2 pin voltage			1.24		V
$I_{SINK1,2}$	WLED current range (ISINK1, ISINK2)		1		25	mA
	WLED sink current	R_{ISET} = 130.0 kΩ		10		
		R_{ISET} = 86.6 kΩ		15		
		R_{ISET} = 64.9 kΩ		20		
		R_{ISET} = 52.3 kΩ		25		
	DC current set accuracy	I_{SINK} = 5 mA to 25 mA, 100% duty cycle	-5		5	%
	DC current matching	R_{SET1} = 52.3 kΩ, I_{SINK} = 25 mA, V_{BAT} = 3.6 V, 100% duty cycle	-5		5	
		R_{SET1} = 130 kΩ, I_{SINK} = 10 mA, V_{BAT} = 3.6 V, 100% duty cycle	-5		5	
f_{PWM}	PWM dimming frequency	FDIM[1:0] = 00		100		Hz
		FDIM[1:0] = 01		200		
		FDIM[1:0] = 10		500		
		FDIM[1:0] = 11		1000		

ELECTRICAL CHARACTERISTICS (continued)

V_{BAT} = 3.6 V ±5%, T_J = 27ºC (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
ANALOG MULTIPLEXER							
g	Gain, VBAT, VSYS	$V_{BAT}/V_{OUT,MUX}$; $V_{SYS}/V_{OUT,MUX}$			3		V/V
	Gain, VTS, MUX_IN	$V_{TS}/V_{OUT,MUX}$; V_{MUX_IN}/V_{MUX_OUT}			1		
	Gain, VICHARGE	$V_{OUT,MUX}/V_{ICHARGE}$	ICHRG[1:0] = 00b		7.575		V/A
			ICHRG[1:0] = 01b		5.625		
			ICHRG[1:0] = 10b		4.500		
			ICHRG[1:0] = 11b		3.214		
V_{OUT}	Buffer headroom	V_{SYS} - V_{MUX_OUT}, V_{SYS} = 3.6 V, MUX[2:0] = 101 (V_{MUX_IN} - V_{MUX_OUT})/V_{MUX_IN} > 1%			0.7	1	V
R_{OUT}	Output Impedance				180		Ω
I_{LEAK}	Leakage current	MUX[2:0] = 000 (HiZ), V_{MUX} = 2.25 V				1	µA
LOGIC LEVELS AND TIMING CHARACTERISTICS (SCL, SDA, PB_IN, PGOOD, LDO_PGOOD, PWR_EN, nINT, nWAKEUP, nRESET)							
P_{GTH}	PGOOD comparator treshold, All DCDC converters and LDOs	Output voltage falling, % of set voltage (not tested in production)			90		%
		Output voltage rising, % of set voltage (not production tested)			95		
P_{GDG}	PGOOD deglitch time	Output voltage falling, DCDC1, 2, 3		2		4	ms
		Output voltage falling, LDO1, 2, 3, 4		1		2	
P_{GDLY}	PGOOD delay time	PGDLY[1:0] = 00			20		ms
		PGDLY[1:0] = 01			100		
		PGDLY[1:0] = 10			200		
		PGDLY[1:0] = 11			400		
t_{HRST}	PB-IN “Hard Reset Detect” time	Not tested in production			8		s
t_{DG}	PB_IN pin deglitch time	Not tested in production			50		ms
	PWR_EN pin deglitch time	Not tested in production			50		
	nRESET pin deglitch time	Not tested in production			30		
R_{PULLUP}	PB_IN internl pull-up resistor				100		kΩ
	nRESET internl pull-up resistor				100		
V_{IH}	High level input voltage PB_IN, SCL, SDA, PWR_EN, nRESET			1.2		V_{IN}	V
V_{IL}	Low level input voltage PB_IN, SCL, SDA, PWR_EN, nRESET			0		0.4	V
I_{BIAS}	Input bias current PB_IN, SCL, SDA				0.01	1	µA
V_{OL}	Output low voltage	nINT, nWAKEUP	I_O = 1 mA			0.3	V
		PGOOD, LDO_PGOOD	I_O = 1 mA			0.3	
V_{OH}	Output high voltage	PGOOD, LDO_PGOOD	I_O = 1 mA	V_{IO} - 0.3			V
I_{LEAK}	Pin leakage current nINT, nWAKEUP	Pin pulled up to 3.3-V supply				0.2	µA
	I^2C slave address				0x24h		
OSCILLATOR							
f_{OSC}	Oscillator frequency				9		MHz
	Frequency accuracy	T_A = –40°C to 105°C		-10		10	%
OVER TEMPERATURE SHUTDOWN							
T_{OTS}	Over temperature shutdown	Increasing junction temperature			150		°C
	Hysteresis	Decreasing junction temperature			20		°C

MODES OF OPERATION

OFF In OFF mode the PMIC is completely shut down with the exception of a few circuits to monitor the AC, USB, and push-button input. All power rails are turned off and the registers are reset to their default values. The I^2C communication interface is turned off. This is the lowest-power mode of operation. To exit OFF mode one of the following wake-up events has to occur:

- The push button input is pulled low.
- The USB supply is connected (positive edge).
- The AC adapter is connected (positive edge).

To enter OFF state, set the OFF bit in the STATUS register to ‘1’ and then pull the PWR_EN pin low. Please note that in normal operation OFF state can only be entered from ACTIVE state. Whenever a fault occurs during operation such as thermal shutdown, power-good fail, under voltage lockout, or PWR_EN pin timeout, all power rails are shut-down and the device goes to OFF state. The device will remain in OFF state until the fault has been removed and a new power-up event has occurred.

ACTIVE This is the typical mode of operation when the system is up and running. All DCDC converters, LDOs, load switches, WLED driver, and battery charger are operational and can be controlled through the I^2C interface.

After a wake-up event the PMIC enables all rails not controlled by the sequencer and pulls the nWAKEUP pin low to signal the event to the host processor. The device will enter ACTIVE state only if the host asserts the PWR_EN pin within 5 seconds after the wake-up event. Otherwise it will enter OFF state. In ACTIVE state the sequencer is triggered to bring up the remaining power rails. The nWAKEUP pin returns to HiZ mode after PWR_EN pin has been asserted. A timing diagram is shown in Figure 2. ACTIVE state can also be entered from SLEEP state directly by pulling the PWR_EN pin high. See SLEEP state description for details.

To exit ACTIVE mode the PWR_EN pin needs to be pulled low.

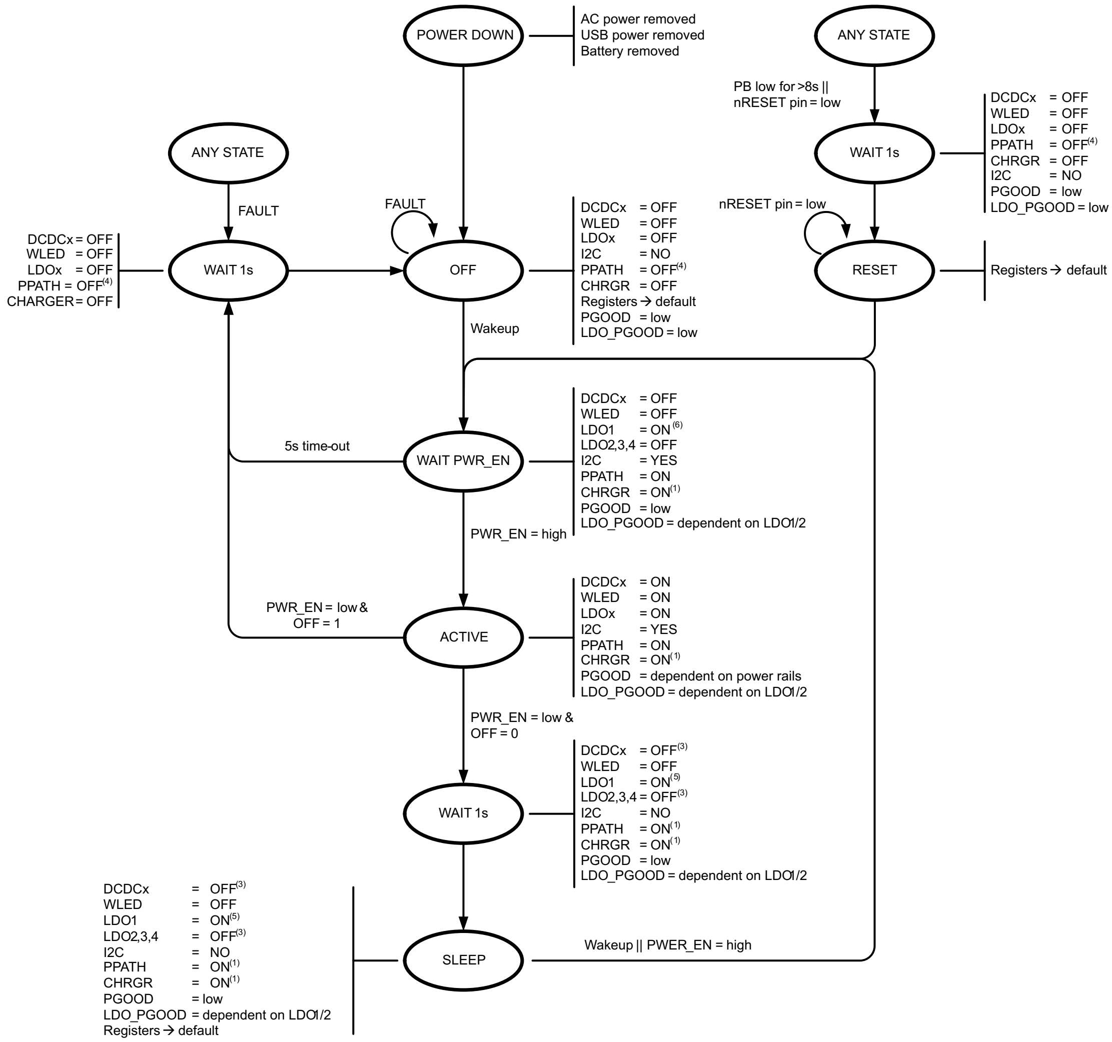
SLEEP SLEEP state is a low-power mode of operation intended to support system standby. Typically all power rails are turned off with the exception of LDO1 and the registers are reset to their default values. LDO1 remains operational but can support only limited amount of current (1 mA typical).

To enter SLEEP state, set the OFF bit in the STATUS register to ‘0’ (default) and then pull the PWR_EN pin low. All power rails controlled by the power-down sequencer will be shut down and after 1s the device enters SLEEP state. If LDO1 was enabled in ACTIVE state, it will remain enabled in SLEEP sate. All rails not controlled by the power-down sequencer will also maintain state. The battery charger will remain active for as long as either USB or AC supply is connected to the device. Please note that all register values are reset as the device enters in SLEEP state, including charger parameters.

The device enters ACTIVE state after it detects a wake-up event as described in the sections above. In addition, the device transitions from SLEEP to ACTIVE state when the PWR_EN pin is pulled high. This allows the system host to switch the PMIC between ACTIVE to SLEEP state by control of the PWR_EN pin only.

RESET The TPS65217 can be reset by either pulling the nRESET pin low or holding the PB_IN pin low for more than 8 seconds. All rails will be shut-down by the sequencer and all register values are reset to their default values. Rails not controlled by the sequencer are shut down immediately. The device remains in this state for as long as the reset pin is held low and the nRESET pin must be high to exit RESET state. However, the device will remain in RESET state for a minimum of 1s before it returns to ACTIVE state. As described in the ACTIVE section, the PWR_EN pin must be asserted within 5 seconds of nWAKEUP-pin-low to enter ACTIVE state. Please note that the RESET function power-cycles the device and only shuts down the output rails temporarily. Resetting the device does not lead to OFF state.

If the PB_IN pin is kept low for an extended amount of time, the device will continue to cycle between ACTIVE and RESET state, entering RESET every 8 s.



NOTES:

Wakeup = V_{USB} (↑) || V_{AC} (↑) || PB (↓) || Returning from RESET state || SEQUP bit = 1

FAULT = UVLO || OTS || PGOOD low || PWR_EN pin not asserted within 5s of Wakeup event

If no battery is present, OVP on AC input also leads to OFF mode. With battery present, device switches automatically from AC to BAT if AC is >6.5V and back to AC when voltage recovers to <6.5V.

Device will remain in RESET state for at least 1s.

Sequencer is triggered when entering ACTIVE state.

(1) Only if USB or AC supply is present

(3) All rails not controlled by the sequencer maintain state when entering SLEEP mode, i.e. they will not be powered down when entering SLEEP mode

(4) Battery voltage always supplies the system (SYS pin)

(5) LDO1/2 are not powered down when entering SLEEP mode if assigned to STROBE 14/15 or not under sequencer control. In SLEEP mode, LDO1 and 2 can source 1 mA only. By default LDO1 is asigned to STROBE15 and LDO2 to STROBE2.

(6) LDO1 and/or LDO2 are powered up if assigned to to STROBE 14/15. By default LDO1 is asigned to STROBE15 and LDO2 to STROBE2.

Figure 1. Global State Diagram

WAKE-UP AND POWER UP SEQUENCING

The TPS65217 has a pre-defined power-up / power-down sequence which in a typical application does not need to be changed. However, it is possible to define custom sequences under I^{2}C control. The power-up sequence is defined by strobes and delay times. Each output rail is assigned to a strobe to determine the order in which the rails are enabled and the delay times between strobes are selectable in a range from 1 ms to 10 ms.

NOTE

Although the user can modify the power-up and power-down sequence through the SEQx registers, those registers are reset to default values when the device enters SLEEP, OFF or RESET state. In practice this means that the power-up sequence is fixed and a other-than-default power-down sequence has to be written every time the device is powered up.

Custom power-up/down sequences can be checked out in ACTIVE mode (PWR_EN pin high) by using the SEQUP and SEQDWN bits. To change the power-up default values, please contact the factory.

Power-Up Sequencing

When the main power-up sequence is initiated, STROBE1 occurs and any rail assigned to this strobe will be enabled. After a delay time of DLY1 STROBE2 occurs and the rail assigned to this strobe is powered up. The sequence continues until all strobes have occurred and all DLYx times have been executed.

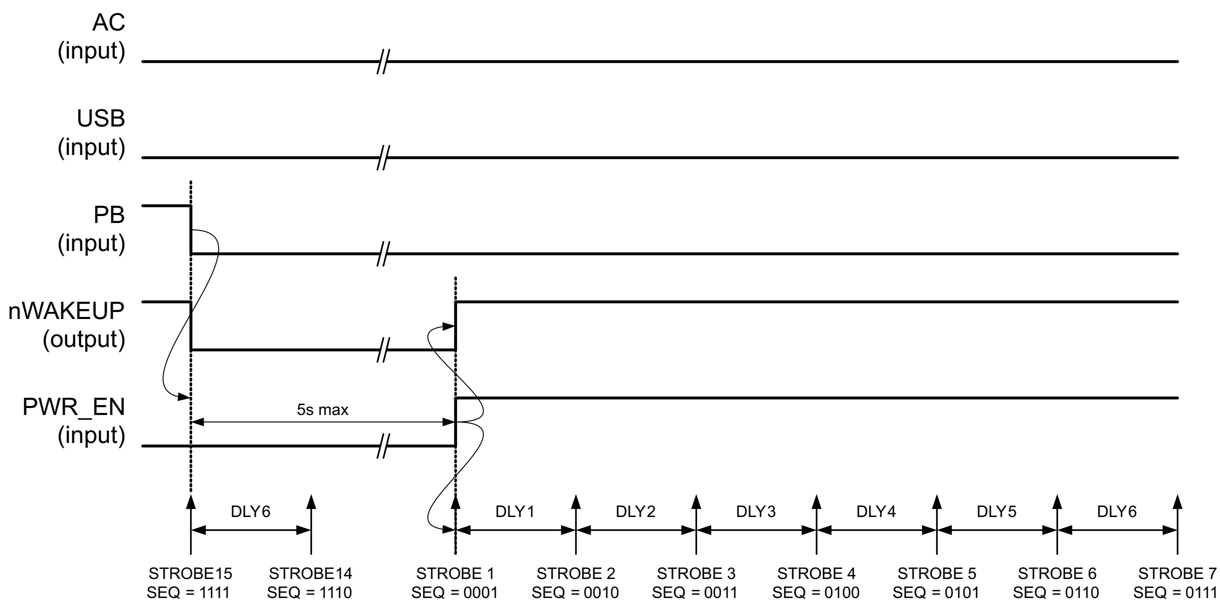


Figure 2. Power-Up Sequence is Defined by Strobes and Delay Times. In This Example Push-Button Low is the Power-Up Event.

The default power-up sequence can be changed by writing to the SEQ1-6 registers. Strobes are assigned to rails by writing to the SEQ1-4 registers. A rail can be assigned to only one strobe but multiple rails can be assigned to the same strobe. Delays between strobes are defined in registers SEQ5 and SEQ6.

The power up sequence is executed if one of the following events occurs:

From OFF State:

- Push-button is pressed (falling edge on PB_IN) OR
- USB voltage is asserted (rising edge on USB) OR
- AC adaptor is inserted (rising edge on AC) AND
- PWR_EN pin is asserted (pulled high) AND
- Device is not in Under Voltage Lockout (UVLO) or Over Temperature Shutdown (OTS).

The PWR_EN pin is level sensitive (opposed to edge sensitive) and it makes no difference if it is asserted before or after the above power-up events. However, it must be asserted within 5 seconds of the power-up event otherwise the power-down sequence will be triggered and the device enters either OFF state.

From SLEEP State:

- Push-button is pressed (falling edge on PB_IN) OR
- USB voltage is asserted (rising edge on USB) OR
- AC adaptor is inserted (rising edge on AC) AND
- Device is not in Under Voltage Lockout (UVLO) or Over Temperature Shutdown (OTS) OR
- PWR_EN pin is asserted (pulled high).

In SLEEP state the power-up sequence can be triggered by asserting the PWR_EN pin only and the push-button press or USB/AC assertion are not required.

From ACTIVE State:

The sequencer can be triggered any time by setting the SEQUP bit of the SEQ6 register high. The SEQUP bit is automatically cleared after the sequencer is done.

Rails that are not assigned to a strobe (SEQ=0000b) are not affected by power-up and power-down sequencing and will remain in their current ON/OFF state regardless of the sequencer. Any rail can be enabled/disabled at any time by setting the corresponding enable bit in the ENABLE register with the only exception that the ENABLE register cannot be accessed while the sequencer is active. Enable bits always reflect the current enable state of the rail, i.e. the sequencer will set/reset the enable bits for the rails under its control. Also, whenever faults occur that shut-down the power-rails, the corresponding enable bits will be reset.

Power-Down Sequencing

By default, power-down sequencing follows the reverse power-up sequence. When the power-down sequence is triggered, STROBE7 occurs first and any rail assigned to STROBE7 will be shut down. After a delay time of DLY6, STROBE6 occurs and any rail assigned to it will be shut down. The sequence continues until all strobes have occurred and all DLYx times have been executed.

In some applications it is desired to shut down all rails simultaneously with no delay between rails. Set the INSTDWN bit in the SEQ6 register to bypass all delay times and shut-down all rails simultaneously when the power-down sequence is triggered.

A power-down sequence is executed if one of the following events occurs:

- The SEQDWN bit is set.
- The PWR_EN pin is pulled low.
- The push-button is pressed for > 8 s.
- The nRESET pin is pulled low.
- A fault occurs in the IC (OTS, UVLO, PGOOD failure).
- The PWR_EN pin is not asserted (pulled high) within 5 seconds of a power-up event and the OFF bit is set to 1.

When transitioning from ACTIVE to OFF state, any rail not controlled by the sequencer is shut down after the power-down sequencer has finished. When transitioning from ACTIVE to SLEEP state any rail not controlled by the power-down sequencer will maintain state. This allows keeping selected power rails up in SLEEP state.

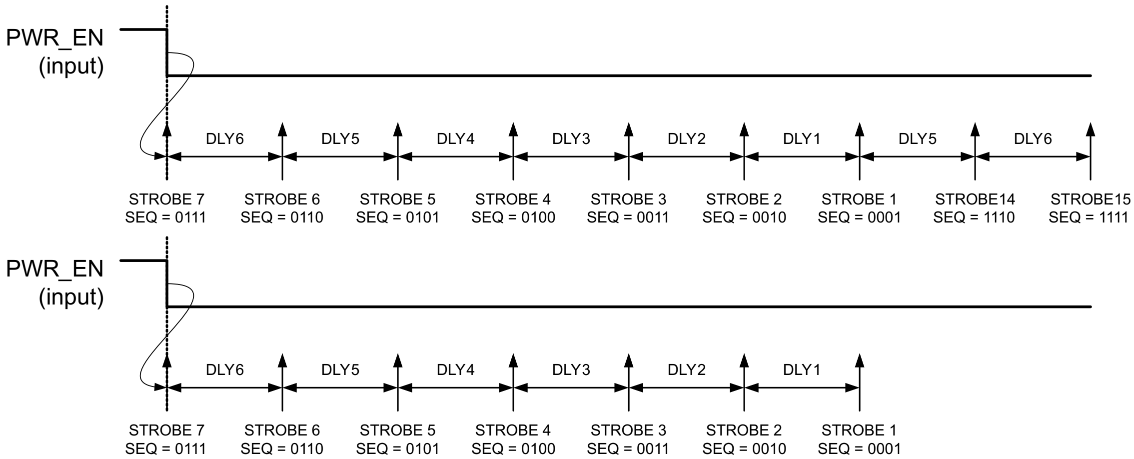


Figure 3. Power-Down Sequence Follows Reverse Power-Up Sequence. TOP: Power-down sequence from ON state to OFF state (all rails are turned OFF). BOTTOM: Power-down sequence from ON state to SLEEP state. STROBE14 and 15 are omitted to allow LDO1/2 to remain ON.

Special Strobes (STROBE 14 and 15)

STROBE 14 and STORBE 15 are not assigned to the main sequencer but used to control rails that are ‘always-on’, i.e. are powered up as soon as the device exits OFF state and remain ON in SLEEP state. STROBE 14/15 options are available only for LDO1 and LDO2 and not for any of the other rails.

STROBE 14 occurs as soon as the push-button is pressed or the USB or AC adaptor is connected to the device. After a delay time of DLY6 STROBE 15 occurs. LDO1 and LDO2 can be assigned to either strobe and therefore can be powered up in any order (contact factory for details - default settings must be factory programmed since all registers are reset in SLEEP mode).

When a power-down sequence is initiated, STOBE 15 and STOBE 14 will occur only if the OFF bit is set. Otherwise both strobes are omitted and LDO1 and LDO2 will maintain state.

POWER GOOD

Power-good is a signal used to indicate if an output rail is in regulation or at fault. Internally, all power-good signals of the enabled rails are monitored at all times and if any of the signals goes low, a fault is declared. All PGOOD signals are internally deglitched. When a fault occurs, all output rails are powered down and the device enters OFF state.

The TPS65217 has two PGOOD outputs, one dedicated to LDO1 and 2 (LDO_PGOOD), and one programmable output (PGOOD). The following rules apply to both outputs:

- The power-up default state for PGOOD/LDO_PGOOD is low. When all rails are disabled, PGOOD and LDO_PGOOD outputs are both low.
- Only enabled rails are monitored. Disabled rails are ignored.
- Power-good monitoring of a particular rail starts 5ms after the rail has been enabled. It is continuously monitored thereafter. This allows the rail to power-up.
- PGOOD and LDO_PGOOD outputs are delayed by the PGDLY (20 ms default) after the sequencer is done.
- If an enabled rail goes down due to a fault (output shorted, OTS, UVLO), PGOOD and/or LDO_PGOOD is declared low, and all rails are shut-down.
- If the user disables a rail (either manually or through sequencer), it has no effect on the PGOOD or LDO_PGOOD pin.
- If the user disables all rails (either manually or through sequencer) PGOOD and/or LDO_PGOOD will be pulled low.

LDO1, LDO2 PGOOD (LDO_PGOOD)

LDO_PGOOD is a push-pull output which is driven to high-level whenever LDO1 and/or LDO2 are enabled and in regulation. It is pulled low when both LDOs are disabled or at least one is enabled but has encountered a fault. A typical fault is an output short or over-current condition. In normal operation LDO_PGOOD is high in ACTIVE and SLEEP state and low in RESET or OFF state.

Main PGOOD (PGOOD)

The main PGOOD pin has similar functionality to the LDO_PGOOD pin except that it monitors DCDC1, DCDC2, DCDC3, and LS1/LDO3, LS2/LDO4 if they are configured as LDOs. If LS1/LDO3 and/or LS2/LDO4 are configured as load switches, their respective PGODD status is ignored. In addition, the user can choose to also monitor LDO1 and LDO2 by setting the LDO1PGM and LDO2PGM bits in the DEFPG register low. By default, LDO1 and LDO2 PGOOD status does not affect the PGOOD pin (mask bits are set to 1 by default). In normal operation PGOOD is high in ACTIVE state but low in SLEEP, RESET or OFF state.

In SLEEP mode and WAIT PWR_EN state, PGOOD pin is forced low. PGOOD is pulled high after entering ACTIVE mode, the power sequencer done, and the PGDLY expired. This function can be disabled by the factory.

Load Switch PGOOD

If either LS1/LDO3 or LS2/LDO4 are configured as load switches their respective PGOOD signal is ignored by the system. An over-current or short condition will not affect the PGOOD pin or any of the power rails unless the power dissipation leads to thermal shut-down.

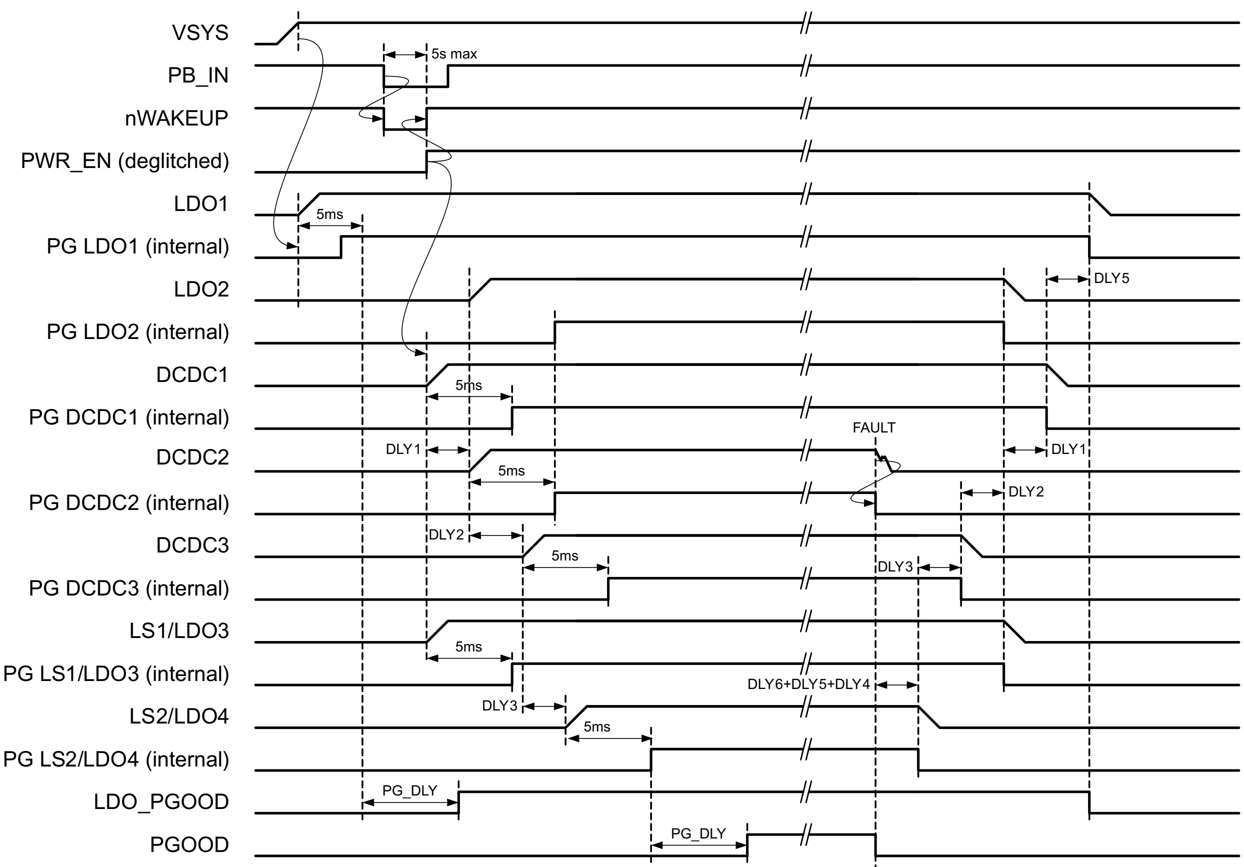


Figure 4. Default Power-Up Sequence. Also shown is the power-down sequence for the case of a short on DCDC2 output.

PUSH BUTTON MONITOR (PB_IN)

The TPS65217 has an active-low push-button input which is typically connected to a momentary switch to ground. The PB_IN input has a 50ms deglitch time and an internal pull-up resistor to an always-on supply. The push button monitor is used to:

- Power-up the device from OFF or SLEEP mode upon detecting a falling edge on PB_IN.
- Power cycle the device when PB_IN is held low for > 8 s.

Both functions are described in the Modes of Operation section. A change in push-button status (PB_IN transitions high to low or low to high) is signaled to the host through the PBI interrupt bit in the INT register. The current status of the interrupt can be checked by reading the PB status bit in the STATUS register. A timing diagram for the push-button monitor is shown in Figure 5.

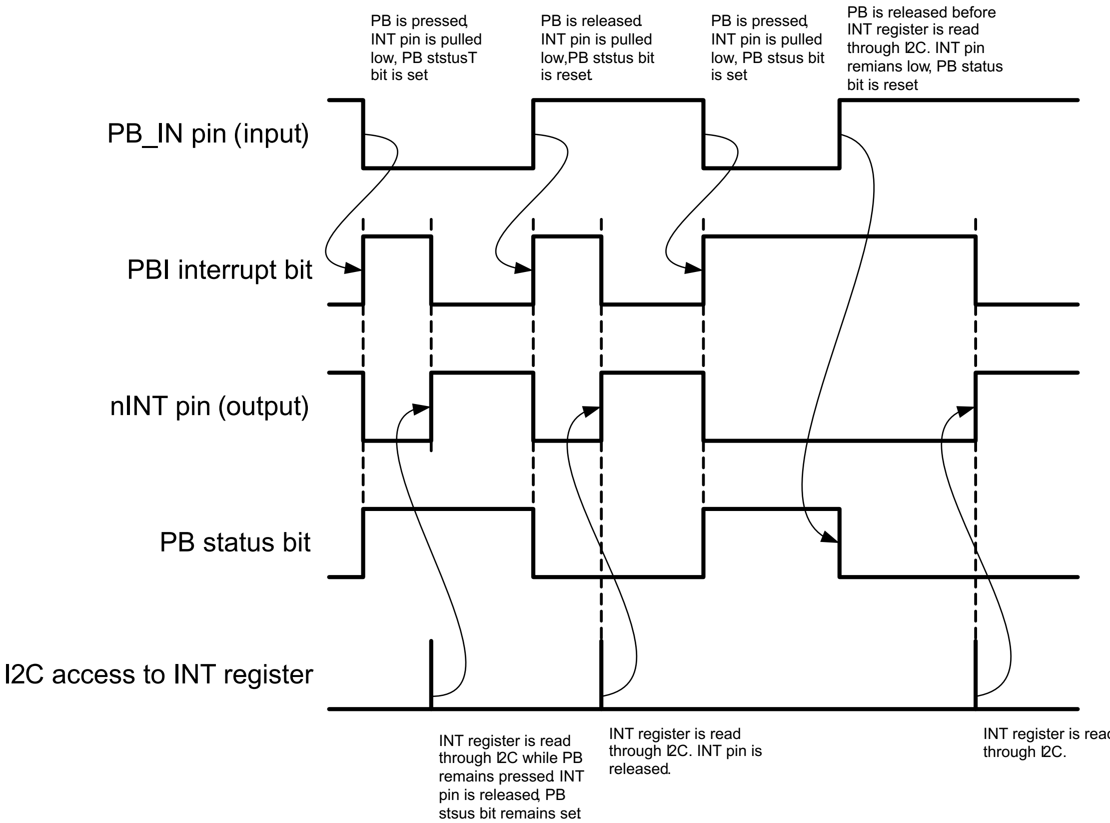


Figure 5. Timing Diagram of the Push-Button Monitor Circuit

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nWAKEUP PIN (nWAKEUP)

The nWAKEUP pin is an open drain, active-low output that is used to signal a wakeup event to the system host. This pin is pulled low whenever the device is in OFF or SLEEP state and detects a wakeup event as described in the Modes of Operation section. The nWAKEUP pin is delayed 50ms over the power-up event and will remain low for 50 ms after the PWR_EN pin has been asserted. If the PWR_EN pin is not asserted within 5 seconds of the power-up event, the device will shut down and enter OFF state. In ACTIVE mode the nWAKEUP pin is always high. The timing diagram for the nWAKEUP pin is shown in Figure 6.

POWER ENABLE PIN (PWR_EN)

The PWR_EN pin is used to keep the unit in ACTIVE mode once it has detected a wakeup event as described in the Modes of Operation section. If the PWR_EN pin is not asserted within 5 seconds of the nWAKEUP pin being pulled low, the device will shut down the power and enter either OFF or SLEEP mode, depending on the OFF bit in the STATUS register. The PWR_EN pin is level sensitive, meaning that it may be pulled high before the wakeup event.

The PWR_EN pin may also be used to toggle between ACTIVE and SLEEP mode. See SLEEP mode description for details.

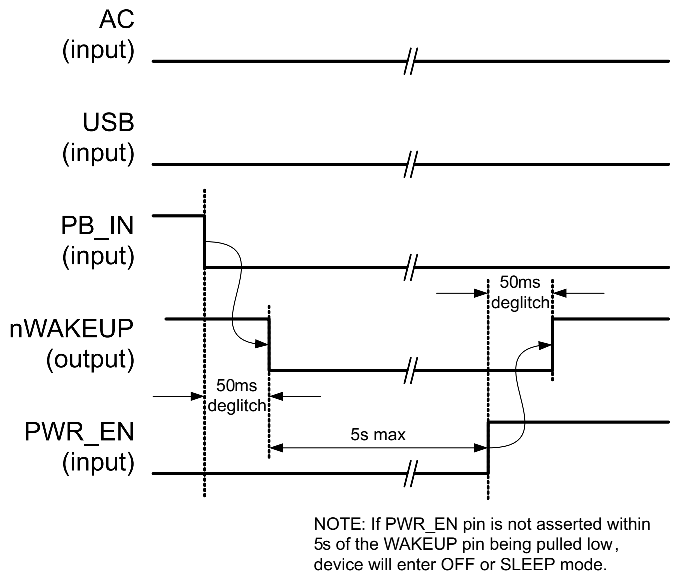

Figure 6. nWAKEUP Timing Diagram. In the example shown the wakeup event is a falling edge on the PB_IN.

RESET PIN (nRESET)

When the nRESET pin is pulled low, all power rails, including LDO1 and LDO2 are powered down and default register settings are restored. The device will remain powered down as long as the nRESET pin is held low but for a minimum of 1 second. Once the nRESET pin is pulled high the device enters ACTIVE mode and the default power-up sequence will execute. See RESET section for more information.

INTERRUPT PIN (nINT)

The interrupt pin is used to signal any event or fault condition to the host processor. Whenever a fault or event occurs in the IC the corresponding interrupt bit is set in the INT register, and the open-drain output is pulled low. The nINT pin is released (returns to HiZ state) and fault bits are cleared when the INT register is read by the host. However, if a failure persists, the corresponding INT bit remains set and the nINT pin is pulled low again after a maximum of 32 µs.

Interrupt events include pushbutton pressed/released, USB and AC voltage status change.

The MASK bits in the INT register are used to mask events from generating interrupts. The MASK settings affect the nINT pin only and have no impact on protection and monitor circuits themselves. Note that persisting event conditions such as ISINK enabled shutdown can cause the nINT pin to be pulled low for an extended period of time which can keep the host in a loop trying to resolve the interrupt. If this behavior is not desired, set the corresponding mask bit after receiving the interrupt and keep polling the INT register to see when the event condition has disappeared. Then unmask the interrupt bit again.

ANALOG MULTIPLEXER

The TPS65217 provides an analog multiplexer that allow access to critical system voltages such as:

- battery voltage (VBAT)
- system voltage (VSYS)
- temperature sense voltage (VTS), and
- VICHARGE, a voltage proportional to the charging current.

In addition one external input is available to monitor an additional system voltage. VBAT and VSYS are divided down by a factor of 1:3 to be compatible with input voltage range of the ADC that resides on the system host side. The output of the MUX is buffered and can drive a maximum of 1-mA load current.

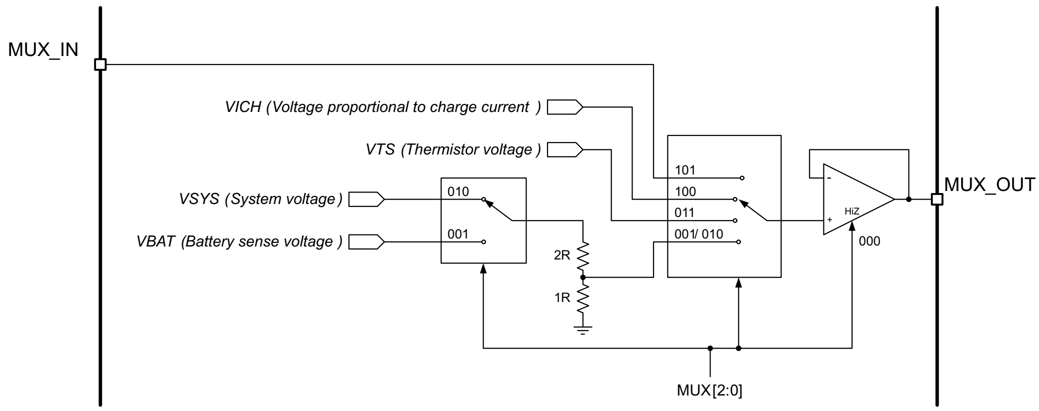

Figure 7. Analog Multiplexer

BATTERY CHARGER AND POWER PATH

TPS65217 provides a linear charger for Li+ batteries and a triple system-power path targeted at space-limited portable applications. The power path allows simultaneous and independent charging of the battery and powering of the system. This feature enables the system to run with a defective or absent battery pack and allows instant system turn-on even with a totally discharged battery. The input power source for charging the battery and running the system can be either an AC adapter or a USB port. The power path prioritizes the AC input over the USB and both over battery input to reduce the number of charge and discharge cycles on the battery. Charging current is automatically reduced when system load increases and if the system load exceeds the maximum current of the USB or AC adapter supply, the battery will supplement, meaning that the battery will be discharged to supply the remaining current. A block diagram of the power path is shown in Figure 8 and an example of the power path management function is shown in Figure 9.

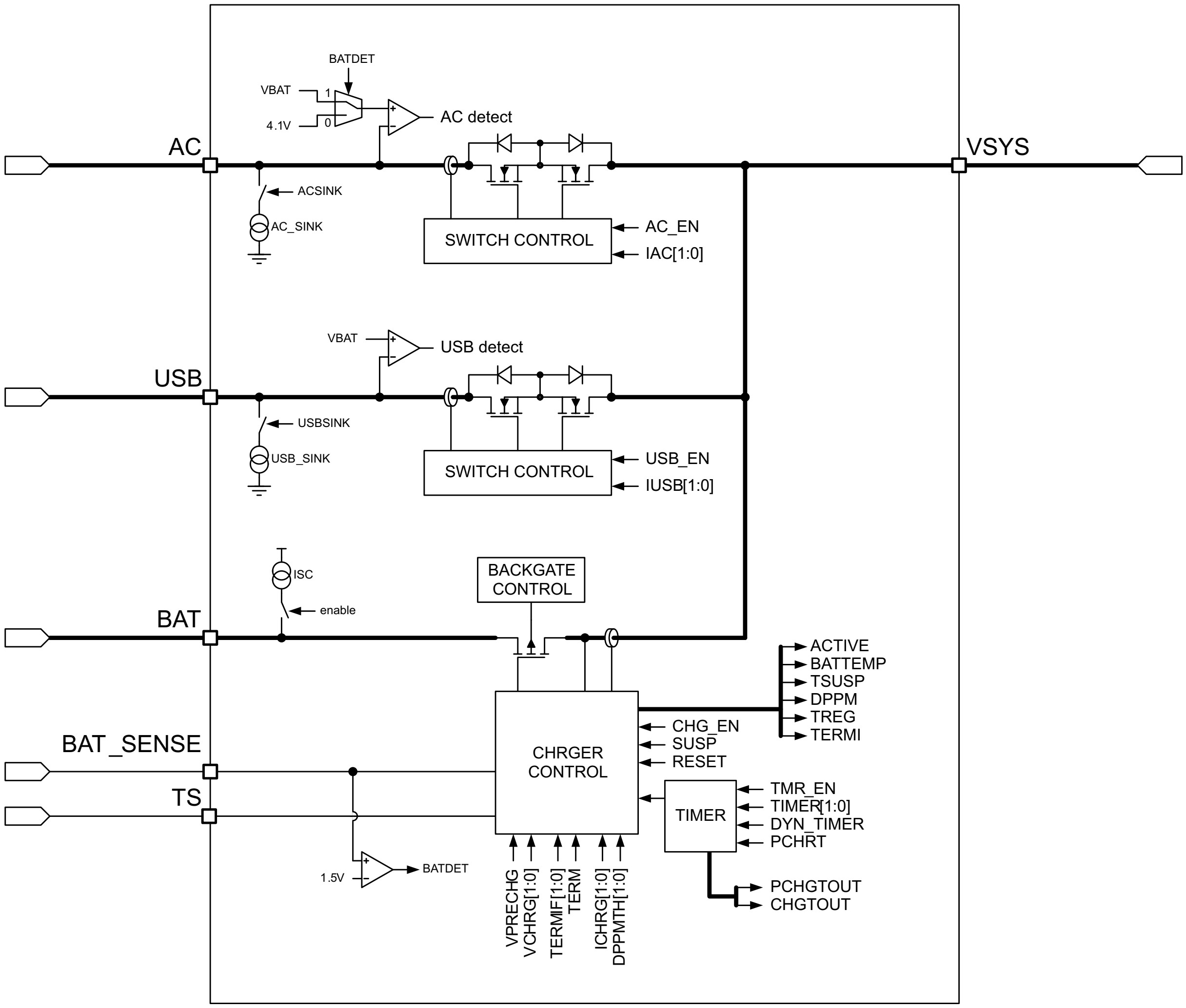

Figure 8. Block Diagram of the Power Path and Battery Charger

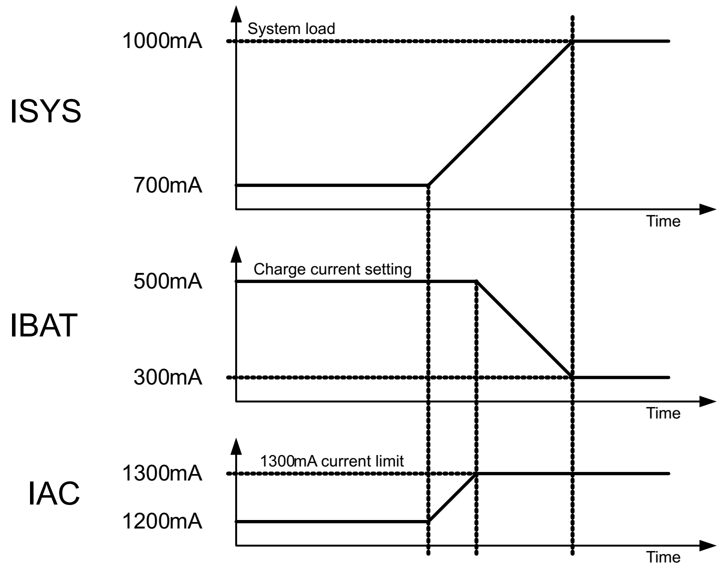

Figure 9. Power Path Management. In this example the AC input current limit is set to 1300 mA, battery charge current is 500 mA and system load is 700 mA. As the system load increases to 1000 mA battery charging current is reduced to 300 mA to maintain AC input current of 1300 mA.

Detection thresholds for AC and USB inputs are a function of the battery voltage and three basic use-cases must be considered:

Shorted or Absent Battery (V_{BAT} < 1.5 V)

AC or USB inputs are valid and the chip powers up if V_{AC} or V_{USB} rises above 4.3 V. Once powered up, the input voltage can drop to the V_{UVLO} + V_{OFFSET} level (e.g. 3.3 V + 200 mV) before the chip powers down.

AC input is prioritized over USB input, i.e. if both inputs are valid, current is pulled from the AC input and not USB. If both, AC and USB supplies are available, the power-path switches to USB input if V_{AC} drops below 4.1 V (fixed threshold).

Note that the rise time of V_{AC} and V_{USB} must be less than 50 ms for the detection circuits to operate properly. If the rise time is longer than 50 ms, the IC may fail to power up.

The linear charger periodically applies a 10-mA current source to the BAT pin to check for the presence of a battery. This will cause the BAT terminal to float up to > 3 V which may interfere with AC removal detection and the ability to switch from AC to USB input. For this reason, it is not recommended to use both AC and USB inputs when the battery is absent.

Dead Battery (1.5 V < V_{BAT} < V_{UVLO})

Functionality is the same as for the shorted battery case. The only difference is that once AC is selected as the input and the power-path does not switch back to USB as V_{AC} falls below 4.1 V.

Good Battery (V_{BAT} > V_{UVLO})

AC and USB supplies are detected when the input is 190 mV above the battery voltage and are considered absent when the voltage difference to the battery is less than 125 mV. This feature ensures that AC and USB supplies are used whenever possible to save battery life. USB and AC inputs are both current limited and controlled through the PPATH register.

In case AC or USB is not present or blocked by the power path control logic (e.g. in OFF state), the battery voltage always supplies the system (SYS pin).

AC and USB Input Discharge

AC and USB inputs have 90-µA internal current sinks which are used to discharge the input pins to avoid false detection of an input source. The AC sink is enabled when USB is a valid supply and V_{AC} is below the detection threshold. Likewise, the USB sink is enabled when AC is a valid supply and V_{USB} is below the detection limit. Both current sinks can be forced OFF by setting the [ACSINK, USBSINK] bits to 11b. Both bits are located in register 0x01 (PPATH).

NOTE

[ACSINK, USBSINK] = 01b and 10b combinations are not recommended as these may lead to unexpected enabling and disabling of the current sinks.

BATTERY CHARGING

When the charger is enabled (CH_EN bit set to 1) it first checks for a short-circuit on the BAT pin by sourcing a small current and monitoring the BAT voltage. If the voltage on the BAT pin rises above $V_{BAT(SC)}$, a battery is present and charging can begin. The battery is charged in three phases: pre-charge, constant current fast charge (current regulation) and a constant voltage charge (voltage regulation). In all charge phases, an internal control loop monitors the IC junction temperature and reduces the charge current if an internal temperature threshold is exceeded. Figure 10 shows a typical charging profile.

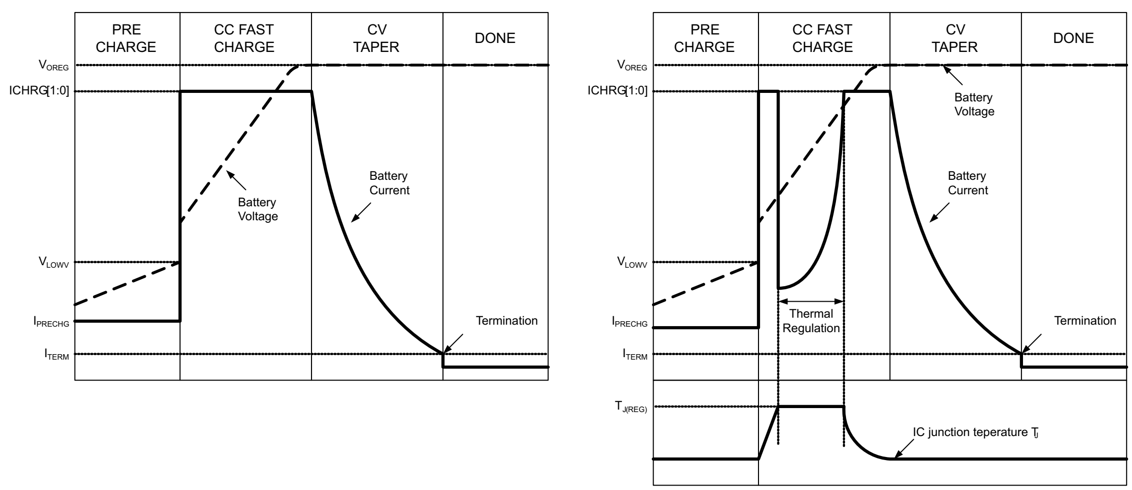

Figure 10. LEFT: Typical charge current profile with termination enabled. RIGHT: Modified charging profile with thermal regulation loop active and termination enabled.

In the pre-charge phase, the battery is charged at a current of IPRECHG which is typically 10% of the fast-charge current rate. The battery voltage starts rising. Once the battery voltage crosses the V_{LOWV} threshold, the battery is charged at a current of I_{CHG}. The battery voltage continues to rise. When the battery voltage reaches V_{OREG}, the battery is held at a constant value of V_{OREG}. The battery current now decreases as the battery approaches full charge. When the battery current reaches I_{TERM}, the TERMI flag in register CHGCONFIG0 is set to 1. To avoid false termination when the DPM or thermal loop kicks in, termination is disabled when either loop is active.

The charge current cannot exceed the input current limit of the power path minus the load current on the SYS pin because the power-path manager will reduce the charge current to support the system load if the input current limit is exceeded. Whenever the nominal charge current is reduced by action of the power path manger, the DPM loop, or the thermal loop the safety timer is clocked with half the nominal frequency to extend the charging time by a factor of 2.

Precharge

The pre-charge current is pre-set to a factor of 10% of the fast-charge current ICHRG[1:0] and cannot be changed by the user.

Charge Termination

When the charging current drops below the termination current threshold, the charger is turned off. The value of the termination current threshold can be set in register CHGCONFIG3 using bits TERMIF[1:0]. The termination current has a default setting of 7.5% of the ICHRG[1:0] setting.

Charge termination is disabled by default and can be enabled by setting the TERM bit or the CHGCONFIG1 register to 1. When termination is disabled, the device goes through the pre-charge, fast-charge and CV phases, then remains in the CV phase. The charger behaves like an LDO with an output voltage equal to V_{OREG}, able to source current up to I_{CHG} or $I_{IN\text{-}MAX}$, whichever is less. Battery detection is not performed.

NOTE

Termination current threshold is not a tightly controlled parameter. Using the lowest setting (2.5% of nominal charge current) is not recommended because the minimum termination current can be very close to 0. Any leakage on the battery-side may cause the termination not to trigger and charging to time-out eventually.

Battery Detection and Recharge

Whenever the battery voltage falls below V_{RCH}, $I_{BAT(DET)}$ is pulled from the battery for a duration t_{DET} to determine if the battery has been removed. If the voltage on the BAT pin remains above V_{LOWV}, it indicates that the battery is still connected. If the charger is enabled (CH_EN = 1), a new battery charging cycle begins.

If the BAT pin voltage falls below V_{LOWV} in the battery detection test, it indicates that the battery has been removed. The device then checks for battery insertion: it turns on the charging path and sources I_{PRECHG} out of the BAT pin for duration t_{DET}. If the voltage does not rise above V_{RCH}, it indicates that a battery has been inserted, and a new charge cycle can begin. If, however, the voltage does rise above V_{RCH}, it is possible that a fully charged battery has been inserted. To check for this, $I_{BAT(DET)}$ is pulled from the battery for t_{DET} and if the voltage falls below V_{LOWV}, no battery is present. The battery detection cycle continues until the device detects a battery or the charger is disabled.

When the battery is removed from the system the charger will also flag a BATTEMP error indicating that the TS input is not connected to a thermistor.

Safety Timer

The TPS65217 hosts internal safety timer for the pre-charge and fast-charge phases to prevent potential damage to either the battery or the system. The default fast-charge time can be changed in register CHGCONFIG1 and the precharge time in CHGCONFIG3. The timer functions can be disabled by resetting the TMR_EN bit of the CHGCONFIG1 register to 0. Note that both timers are disabled when charge termination is disabled (TERM = 0).

Dynamic Timer Function

Under some circumstances the charger current is reduced to react to changes in the system load or junction temperature. The two events that can reduce the charging current are:

- The system load current increases, and the DPM loop reduces the available charging current.
- The device has entered thermal regulation because the IC junction temperature has exceeded $T_{J(REG)}$.

In each of these events, the timer is clocked with half frequency to extend the charger time by a factor of 2 and charger termination is disabled. Normal operation resumes after IC junction temperature has cooled off and/or the system load drops to a level where enough current is available to charge the battery at the desired charge rate. This feature is enabled by default and can be disabled by resetting the DYNTMR bit in the CHGCONFIG2 register to 0. A modified charge cycle with the thermal loop active is shown in Figure 10.

Timer Fault

A timer fault occurs if:

- If the battery voltage does not exceed V_{LOWV} in time t_{PRECHG} during pre-charging.
- If the battery current does not reach I_{TERM} in fast charge before the safetimer expires. Fast-charge time is measured from the beginning of the fast charge cycle.

The fault status is indicated by CHTOUT and PCHTOUT bits in CHGCONFIG0 register. Timeout faults are cleared and a new charge cycle is started when either USB or AC supplies are connected (rising edge of V_{USB} or V_{AC}), the charger RESET bit is set to 1 in the CHGCONFIG1 register, or the battery voltage drops below the recharge threshold V_{RCH}.

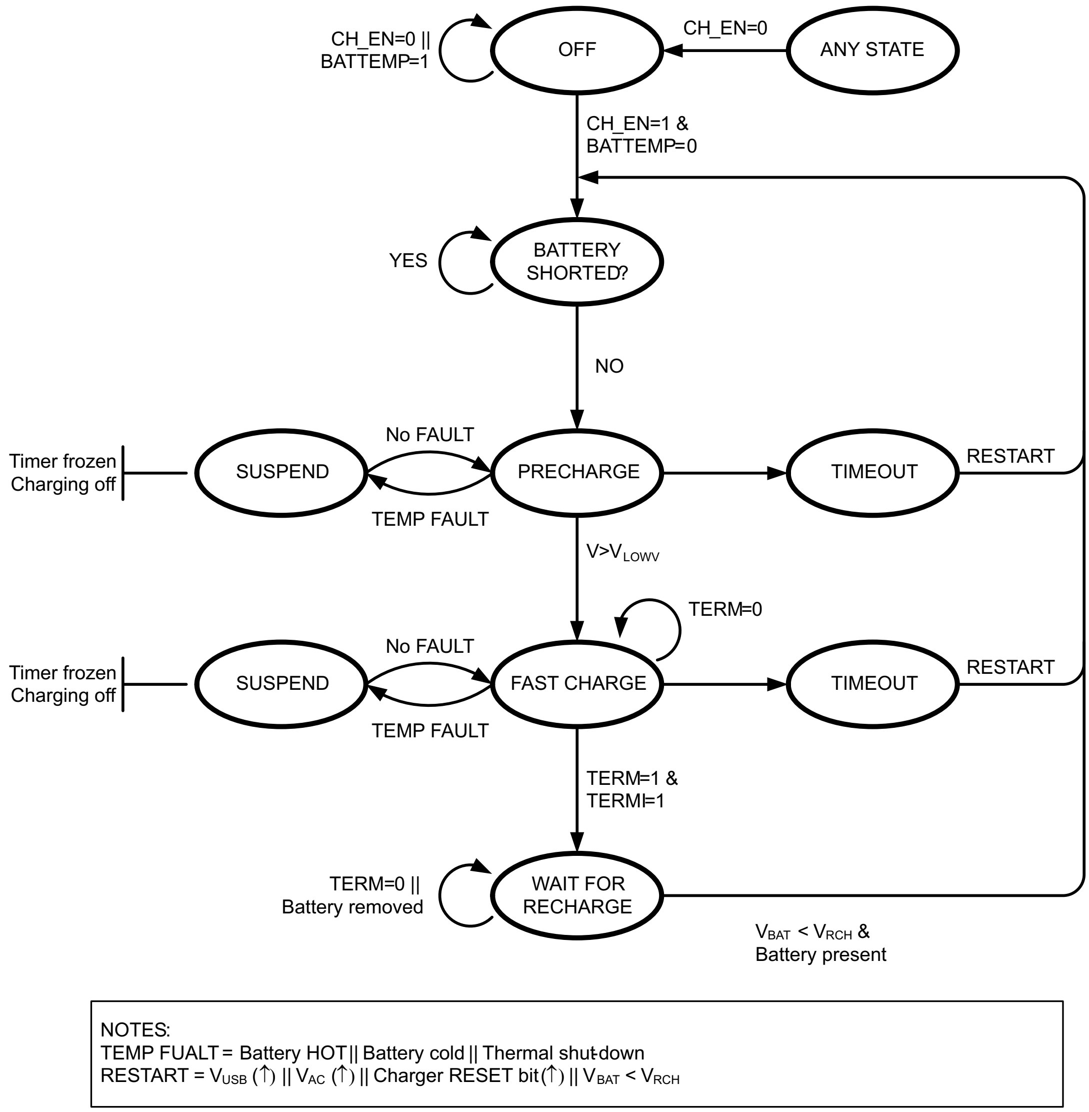

Figure 11. State Diagram of Battery Charger

Battery Pack Temperature Monitoring

The TS pin of the TPS65217 connects to the NTC resistor in the battery pack. During charging, if the resistance of the NTC indicates that the battery is operating outside the limits of safe operation, charging is suspended and the safety timer value is frozen. When the battery pack temperature returns to a safe value, charging resumes with the current timer setting.

By default, the device is setup to support a 10 kΩ the NTC with a B-value of 3480. The NTC is biased through a 7.35-kΩ internal resistor connected to the BYPASS rail (2.25 V) and requires an external 75-kΩ resistor parallel to the NTC to linearize the temperature response curve.

TPS65217 supports two different temperature ranges for charging, 0°C to 45°C and 0°C to 60°C which can be selected through the TRANGE bit in register CHCONFIG3.

NOTE

The device can be configured to support a 100-kΩ NTC (B = 3960) by setting the the NTC_TYPE bit in register CHGCONFIG1 to 1. However it is not recommended to do so. In sleep mode the charger continues charging the battery but all register values are reset to default values, therefore the charger would get wrong temperature information. If 100 kΩ NTC setting is required, please contact the factory.

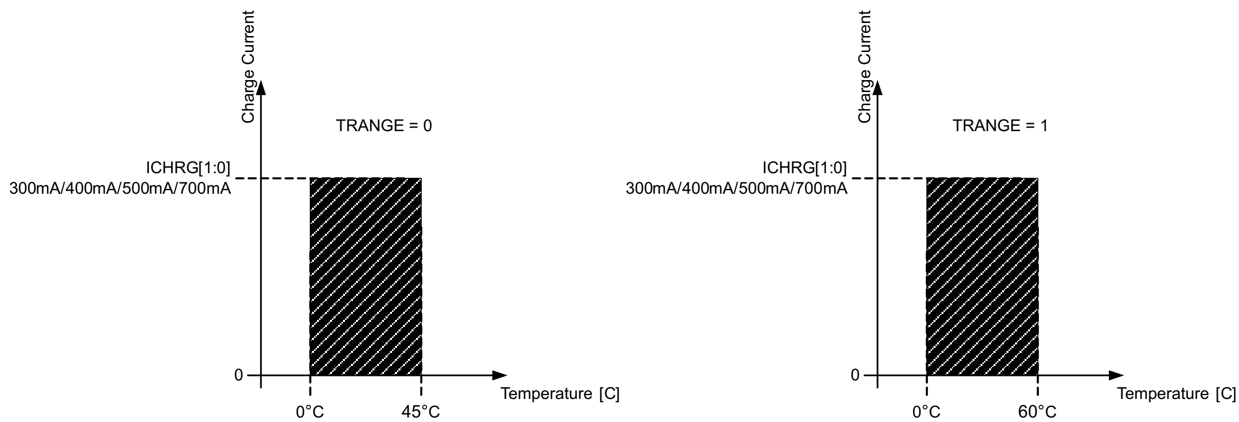

Figure 12. Charge Current as a Function of Battery Temperature

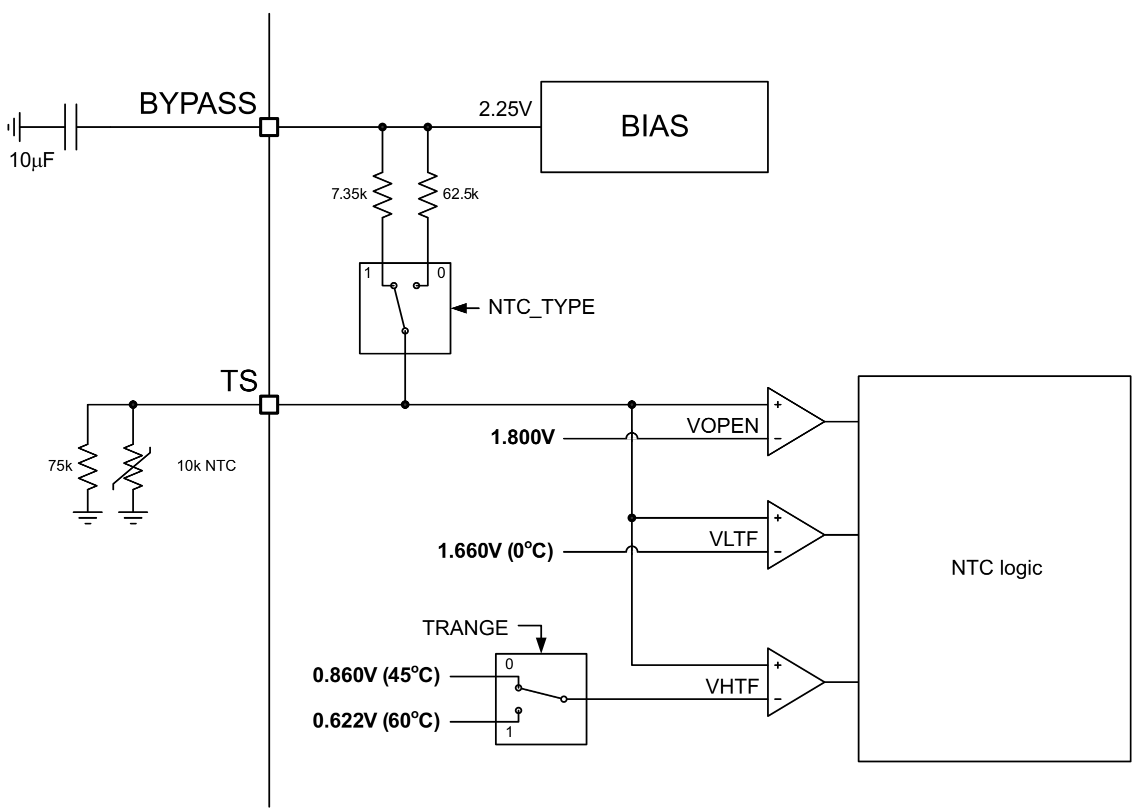

Figure 13. NTC Bias Circuit

DCDC CONVERTERS

Operation

The TPS65217 step down converters typically operate with 2.25-MHz fixed frequency pulse width modulation (PWM) at moderate to heavy load currents. At light load currents the converter automatically enters Power Save Mode and operates in PFM (Pulse Frequency Modulation).

During PWM operation the converter use a unique fast response voltage mode controller scheme with input voltage feed-forward to achieve good line and load regulation allowing the use of small ceramic input and output capacitors. At the beginning of each clock cycle the high-side MOSFET is turned on. The current flows from the input capacitor via the high-side MOSFET through the inductor to the output capacitor and load. During this phase, the current ramps up until the PWM comparator trips and the control logic turns off the switch. The current limit comparator will also turn off the switch in case the current limit of the high-side MOSFET switch is exceeded. After a dead time preventing shoot through current, the low-side MOSFET rectifier is turned on and the inductor current ramps down. The current flows now from the inductor to the output capacitor and to the load. It returns back to the inductor through the low-side MOSFET rectifier.

The next cycle turns off the low-side MOSFET rectifier and turs on the on the high-side MOSFET.

The DC-DC converters operate synchronized to each other, with converter 1 as the master. A 120° phase shift between DCDC1/DCDC2 and DCDC2/DCDC3 decreases the combined input RMS current at the VIN_DCDCx pins. Therefore smaller input capacitors can be used.

Output Voltage Setting

The output voltage of the DCDCs can be set in two different ways:

- As a fixed voltage converter where the voltage is defined in register DEFDCDCx.
- An external resistor network. Set the XADJx bit in register DEFDCDCx register and calculate the output voltage with the following formula:

$$V_{OUT} = V_{REF} \times (1 + \frac{R_1}{R_2}) \tag{1}$$

Where V_{REF} is the feedback voltage of 0.6 V. It is recommended to set the total resistance of R1 + R2 to less than 1 MΩ. Shield the VDCDC1, VDCDC2, and VDCDC3 lines from switching nodes and inductor L1, L2, and L3 to prevent coupling of noise into the feedback pins.

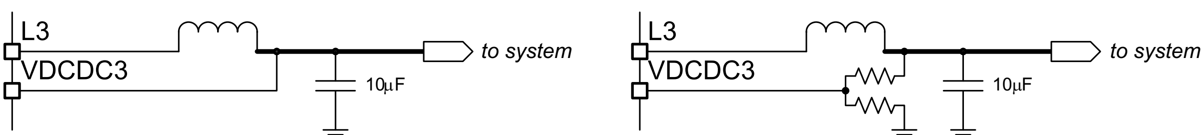

Figure 14. DCDC1, 2, and 3 Offer Two Methods to Adjust the Output Voltage. Example for DCDC3. LEFT: fixed voltage options programmable through I²C (XADJ3 = 0, default). RIGHT: Voltage is set by external feedback resistor network (XADJ3 = 1).

Power Save Mode and Pulse Frequency Modulation (PFM)

By default all three DCDC converter enter Pulse Frequency Modulation (PFM) mode at light loads and fixed-frequency Pulse Width Modulation (PWM) mode at heavy loads. In some applications it is desirable to force PWM operation even at light loads which can be accomplished by setting the PFM_ENx bits in the DEFSLEW registers to 0 (default setting is 1). In PFM mode the converter skips switching cycles and operates with reduced frequency with a minimum quiescent current to maintain high efficiency. The converter will position the output voltage typically +1% above the nominal output voltage. This voltage positioning feature minimizes voltage drops caused by a sudden load step.

The transition from PWM to PFM mode occurs once the inductor current in the low-side MOSFET switch becomes 0.

During the Power Save Mode the output voltage is monitored with a PFM comparator. As the output voltage falls below the PFM comparator threshold of V_{OUT} - 1%, the device starts a PFM current pulse. For this the high-side MOSFET will turn on and the inductor current ramps up. Then it is turned off and the low-side MOSFET switch turns on until the inductor current becomes 0 again.

The converter effectively delivers a current to the output capacitor and the load. If the load is below the delivered current the output voltage will rise. If the output voltage is equal or higher than the PFM comparator threshold, the device stops switching and enters a sleep mode with typically 15-µA current consumption. In case the output voltage is still below the PFM comparator threshold, further PFM current pulses will be generated until the PFM comparator threshold is reached. The converter starts switching again once the output voltage drops below the PFM comparator threshold.

With a single threshold comparator, the output voltage ripple during PFM mode operation can be kept very small. The ripple voltage depends on the PFM comparator delay, the size of the output capacitor and the inductor value. Increasing output capacitor values and/or inductor values will minimize the output ripple.

The PFM mode is left and PWM mode entered in case the output current can no longer be supported in PFM mode or if the output voltage falls below a second threshold, called PFM comparator low threshold. This PFM comparator low threshold is set to -1% below nominal V_{OUT}, and enables a fast transition from Power Save Mode to PWM Mode during a load step.

The Power Save Mode can be disabled through the I^2C interface for each of the step-down converters independent from each other. If Power Save Mode is disabled, the converter will then operate in fixed PWM mode.

Dynamic Voltage Positioning

This feature reduces the voltage under/overshoots at load steps from light to heavy load and vice versa. It is active in Power Save Mode. It provides more headroom for both the voltage drop at a load step, and the voltage increase at a load throw-off. This improves load transient behavior. At light loads, in which the converter operates in PFM mode, the output voltage is regulated typically 1% higher than the nominal value. In case of a load transient from light load to heavy load, the output voltage drops until it reaches the PFM comparator low threshold set to –1% below the nominal value and enters PWM mode. During a load throw off from heavy load to light load, the voltage overshoot is also minimized due to active regulation turning on the low-side MOSFET.

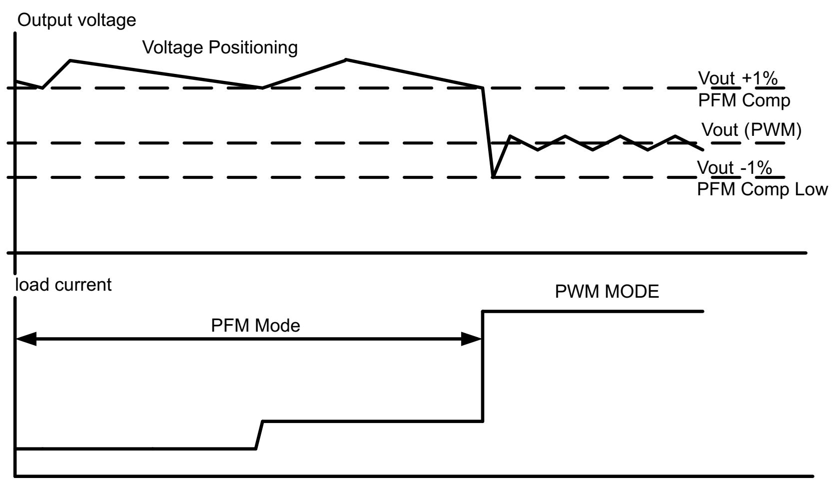

Figure 15. Dynamic Voltage Positioning in Power Save Mode

100% Duty Cycle Low Dropout Operation

The device starts to enter 100% duty cycle Mode once the input voltage comes close the nominal output voltage. In order to maintain the output voltage, the high-side MOSFET is turned on 100% for one or more cycles. As VIN decreases further, the high-side MOSFET is turned on completely. In this case the converter offers a low input-to-output voltage difference. This is particularly useful in battery-powered applications to achieve longest operation time by taking full advantage of the whole battery voltage range.

The minimum input voltage to maintain regulation depends on the load current and output voltage, and can be calculated as:

$$V_{IN,MIN} = V_{OUT,MAX} + I_{OUT,MAX} \cdot \left(R_{DSON,MAX} + R_L\right) \tag{2}$$

where:

$I_{OUT,MAX}$ = Maximum output current plus inductor ripple current
$R_{DSON,MAX}$ = Maximum upper MOSFETt switch R_{DSON}
R_L = DC resistance of the inductor
$V_{OUT,MAX}$ = Nominal output voltage plus maximum output voltage tolerance

Short-Circuit Protection

High-side and low-side MOSFET switches are short-circuit protected. Once the high-side MOSFET switch reaches its current limit, it is turned off and the low-sideMOSFET switch is turned ON. The high-side MOSFET switch can only turn on again, once the current in the low-sideMOSFET switch decreases below its current limit.

Soft Start

The 3 step-down converters in TPS65217 have an internal soft start circuit that controls the ramp up of the output voltage. The output voltage ramps up from 5% to 95% of its nominal value within 750 µs. This limits the inrush current in the converter during start up and prevents possible input voltage drops when a battery or high impedance power source is used. The soft start circuit is enabled after the start up time t_{Start} has expired.

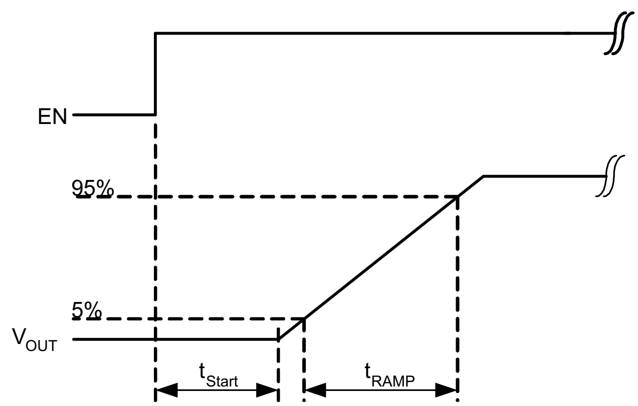

Figure 16. Output of the DCDC Converters is Ramped Up Within 750 µs

Output Filter Design (Inductor and Output Capacitor)

Inductor Selection for Buck Converters

The step-down converters operate typically with 2.2-µH output inductors. Larger or smaller inductor values can be used to optimize the performance of the device for specific operation conditions. The selected inductor has to be rated for its DC resistance and saturation current. The DC resistance of the inductance will influence directly the efficiency of the converter. Therefore an inductor with lowest DC resistance should be selected for highest efficiency.

The following formula can be used to calculate the maximum inductor current under static load conditions. The saturation current of the inductor should be rated higher than the maximum inductor current because during heavy load transient the inductor current will rise above the calculated value.

$$\Delta I_L = Vout \cdot \frac{1 - \frac{Vout}{Vin}}{L \cdot f} \tag{3}$$

$$I_{L\max} = I_{out\max} + \frac{\Delta I_L}{2} \tag{4}$$

where:

f = Switching frequency (2.25 MHz typical)
L = Inductor value
ΔI_L = Peak to peak inductor ripple current
I_{Lmax} = Maximum inductor current

The highest inductor current will occur at maximum V_{IN}. Open core inductors have a soft saturation characteristic and they can usually handle higher inductor currents versus a comparable shielded inductor.

A more conservative approach is to select the inductor current rating just for the maximum switch current of the corresponding converter. It must be considered, that the core material from inductor to inductor differs and will have an impact on the efficiency especially at high switching frequencies. Also the resistance of the windings will greatly affect the converter efficiency at high load. Please refer to Table 1 for recommended inductors.

Table 1. Recommended Inductors for DCDC1, 2, and 3

PART NUMBER	SUPPLIER	VALUE (µH)	R_{DS} (mΩ) MAX	RATED CURRENT (A)	DIMENSIONS (mm)
LQM2HPN2R2MG0L	Murata	2.2	100	1.3	2 x 2.5 x 0.9
VLCF4018T-2R2N1R4-2	TDK	2.2	60	1.44	3.9 x 4.7 x 1.8

Output Capacitor Selection

The advanced Fast Response voltage mode control scheme of the two converters allow the use of small ceramic capacitors with a typical value of 10 µF, without having large output voltage under and overshoots during heavy load transients. Ceramic capacitors having low ESR values result in lowest output voltage ripple and are therefore recommended.

If ceramic output capacitors are used, the capacitor RMS ripple current rating must always meet the application requirements. For completeness the RMS ripple current is calculated as:

$$I_{RMSCout} = Vout \cdot \frac{1 - \frac{Vout}{Vin}}{L \cdot f} \cdot \frac{1}{2 \cdot \sqrt{3}} \tag{5}$$

At nominal load current the inductive converters operate in PWM mode and the overall output voltage ripple is the sum of the voltage spike caused by the output capacitor ESR plus the voltage ripple caused by charging and discharging the output capacitor:

$$\Delta Vout = Vout \cdot \frac{1 - \frac{Vout}{Vin}}{L \cdot f} \cdot \left(\frac{1}{8 \cdot Cout \cdot f} + ESR \right) \tag{6}$$

Where the highest output voltage ripple occurs at the highest input voltage V_{IN}.

At light load currents the converters operate in Power Save Mode and the output voltage ripple is dependent on the output capacitor value. The output voltage ripple is set by the internal comparator delay and the external capacitor. The typical output voltage ripple is less than 1% of the nominal output voltage.

Input Capacitor Selection

Because of the nature of the buck converter having a pulsating input current, a low ESR input capacitor is required for best input voltage filtering and minimizing the interference with other circuits caused by high input voltage spikes. The converters need a ceramic input capacitor of 10 µF. The input capacitor can be increased without any limit for better input voltage filtering. Please refer to Table 2 for recommended ceramic capacitors.

Table 2. Recommended Input Capacitors for DCDC1, 2, and 3

PART NUMBER	SUPPLIER	VALUE (µF)	DIMENSIONS
C2012X5R0J226MT	TDK	22	0805
JMK212BJ226MG	Taiyo Yuden	22	0805
JMK212BJ106M	Taiyo Yuden	10	0805
C2012X5R0J106M	TDK	10	0805

STANDBY LDOS (LDO1, LDO2)

LDO1 and LDO2 support up to 100 mA each, are internally current limited and have a maximum drop-out voltage of 200 mV at rated output current. In SLEEP mode, however, output current is limited to 1 mA each. When disabled, both outputs are discharged to ground through a 430-Ω resistor.

LDO1 supports an output voltage range of 1.0 V - 1.8 V which is controlled through the DEFLDO1 register. LDO2 supports an output voltage range from 0.9 V - 1.5 V and is controlled through the DEFLDO2 register. By default, LDO1 is enabled immediately after a power-up event as described in the Modes of Operation section and remains ON in SLEEP mode to support system standby. Each LDO has low standby-current of < 15 µA typical.

LDO2 can be configured to track the output voltage of DCDC3 (core voltage). When the TRACK bit is set in the DEFLDO2 register, the output is determined by the DCDC3[5:0] bits of the DEFDCDC3 register and the LDO2[5:0] bits of the DEFLDO2 register are ignored.

LDO1 and LDO2 can be controlled through STROBE 1-6, special STROBES 14 and 15, or through the corresponding enable bits in the ENABLE register. By default, LDO1 are controlled through STROBE15 which keeps it alive in SLEEP mode. The STROBE assignments can be changed by the user while in ACTIVE mode but be aware that all register settings are reset to default values in SLEEP or OFF mode. This can cause the LDO to power up automatically when leaving SLEEP mode even tough they have been disabled in SLEEP mode previously by assigning them to a different strobe or resetting the corresponding enable bit. If this is not desired, new default values must be programmed into non-volatile memory by the factory. Contact TI for details.

LOAD SWITCHES/LDOS (LS1/LDO3, LS2/LDO4)

TPS65217 provides two general-purpose load switches that can also be configured as LDOs. As LDOs they support up to 200 mA each, are internally current limited and have a maximum drop-out voltage of 200 mV at rated output current. LDO3 and LDO4 of the TPS65217C and and TPS65217D devices support up to 400-mA of current. In either mode ON/OFF state can be controlled either through the sequencer or the LS1_EN and LS2_EN bits of the ENABLE register. When disabled, both outputs are discharged to ground through a 375-Ω resistor.

As load switches LS1 and LS2 have a max impedance of 650 mΩ. Different from LDO operation, load switches can remain in current limit indefinitely without affecting the internal power-good signal or affecting the other rails. Please note, however, that excessive power dissipation in the switches may cause thermal shutdown of the IC.

Load switch and LDO mode are controlled by LS1LDO3 and LS2LDO4 bits of the DEFLS1 and DEFLS2 registers.

WHITE LED DRIVER

TPS65217 contains a boost converter and two current sinks capable of driving up to 2 x 10 LEDs at 25 mA or a single string at 50 mA of current. The current per current sink is approximated by the following equation:

$$I_{LED} = 1048 \times \frac{1.24V}{R_{SET}} \tag{7}$$

Two different current levels can be programmed using two external R_{SET} resistors. Only one current setting is active at any given time and both current sinks are always regulated to the same current. The active current setting is selected through the ISEL bit of the WLEDCTRL1 register.

Brightness dimming is supported by an internal PWM signal and I^2C control. Both current sources are controlled together and cannot operate independently. By default, the PWM frequency is set to 200 Hz, but can be changed to 100 Hz, 500 Hz, and 1000 Hz. The PWM duty cycle can be adjusted from 1% (default) to 100% in 1% steps through the WLEDCTRL2 register.

When the ISINK_EN bit of WLEDCTRL1 register is set to 1, both current sinks are enabled and the boost output voltage at the FB_WLED pin is regulated to support the same I_{SINK} current through each current sink. The boost output voltage, however, is internally limited to 39 V.

If only a single WLED string is required, short ISINK1 and ISINK2 pins together and connect them to the Cathode of the diode string. Note that the LED current in this case is 2 x I_{SINK}.

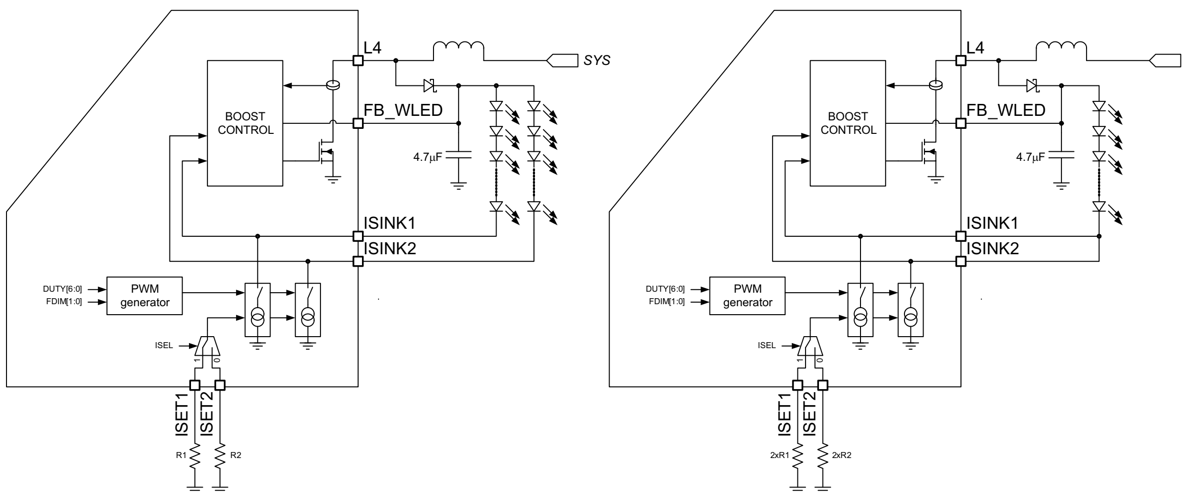

Figure 17. Block Diagram of WLED Driver. LEFT: Dual string operation. RIGHT: Single string operation (same LED current as dual string). Note that for single string operation both ISINK pins are shorted together and RSET values are doubled.

Table 3. Recommended Inductors for WLED Boost Converter

PART NUMBER	SUPPLIER	VALUE (µH)	R_{DS} (mΩ) MAX	RATED CURRENT (A)	DIMENSIONS (mm x mm x mm)
CDRH74NP-180M	Sumida	18	73	1.31	7.5 x 7.5 x 4.5
P1167.183	Pulse	18	37	1.5	7.5 x 7.5 x 4.5

Table 4. Recommended Output Capacitors for WLED Boost Converter

PART NUMBER	SUPPLIER	VOLTAGE RATING (V)	VALUE (µF)	DIMENSIONS	DIELECTRIC
UMK316BJ475ML-T	Taiyo Yuden	50	4.7	1206	X5R

BATTERY-LESS/5-V OPERATION

TPS65217 provides a linear charger for Li+ batteries but the IC can operate without a battery attached. There are three basic use-cases for battery-less operation:

1. The system is designed for battery operation, but the battery is not inserted. The system can be powered by connecting an AC adaptor or USB supply.
2. A non-portable system running off a (regulated) 5-V supply, but the PMIC must provide protection against input over-voltage up to 20 V. Electrically this is the same as the previous case where the IC is powered off an AC adaptor. The battery pins (BAT, BATSENSE, TS) are floating and power is provided through the AC pin. DCDC converters, WLED driver, and LDOs connect to the over-voltage protected SYS pins. Load switches (or LDO3 and LDO4, depending on configuration) typically connect to one of the lower system rails but may also be connected to the SYS pin.
3. A non-portable system running of a regulated 5-V supply that does not require input-over-voltage protection. In this case the 5-V power supply is connected through the BAT pins and the DCDC converter inputs, WLED driver, LDO1, and LDO2 are connected directly to the 5-V supply. A 10-kΩ resistor is connected from TS to ground to simulate the NTC of the battery. Load switches (or LDO3 and LDO4, depending on configuration) typically connect to one of the lower system rails, but may also be connected to the 5-V input supply directly. The main advantage of connecting the supply to the BAT pins is higher power-efficiency because the internal power-path is by-passed and power-loss across the internal switches is avoided.

Figure 18 shows the connection of the input power supply to the IC for 5-V only operation with and without 20-V input over-voltage protection and Table 5 lists the functional differences between both setups.

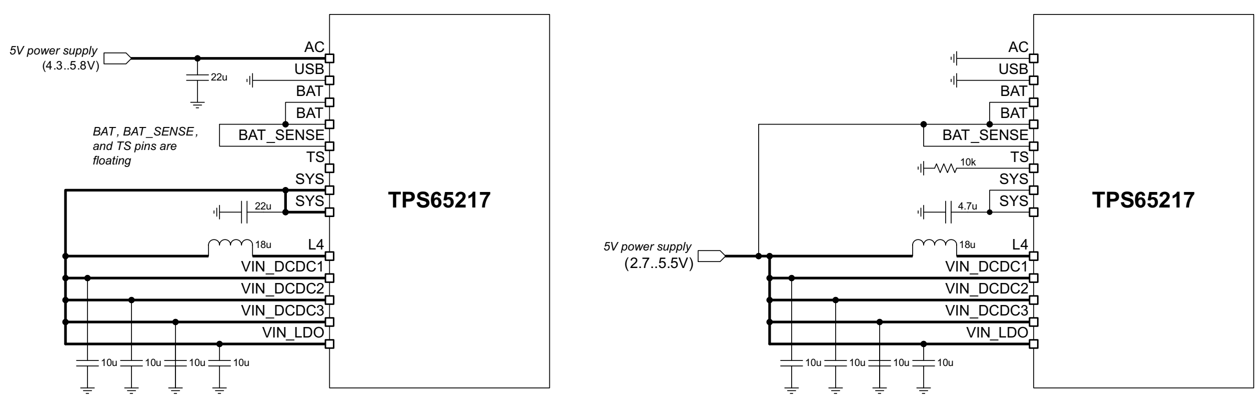

Figure 18. Left: Power-connection for battery-less/5-V only operation. The SYS node and DCDC converters are protected against input over-voltage up to 20 V. Right: Power-connection for 5-V only operation. The DCDC converters are not protected against input over-voltage, but power-efficiency is higher because the internal power-path switches are bypassed.

Table 5. Functional Differences Between Battery-Less/5-V Only Operation With and Without 20-V Input Over-Voltage Protection

	POWER SUPPLIED THROUGH AC PIN (CASE (1) AND (2))	POWER SUPPLIED THROUGH BAT PIN (CASE (3))
Input protection	Max operating input voltage is 5.8 V, but IC is protected against input over-voltage up to 20 V.	Max operating input voltage is 5.5 V.
Power efficiency	DCDC input current passes through AC-SYS power-path switch (approximately 150 mΩ).	Internal power-path is bypassed to minimize IxR losses.
BATTEMP bit	BATTEMP bit (bit 0 in register 0x03h) always reads 1, but has no effect on operation of the part.	BATTEMP bit (bit 0 in register 0x03h) always reads 0.
Output rail status upon initial power connection	LDO1 is automatically powered up when AC pin is connected to 5-V supply and device enters [WAIT PWR_EN] state. IF PWR_EN pin is not asserted within 5s, LDO1 turns OFF.	LDO1 is OFF when BAT is connected to 5-V supply. PB_IN must be pulled low to enter [WAIT PWR_EN] state.

Table 5. Functional Differences Between Battery-Less/5-V Only Operation With and Without 20-V Input Over-Voltage Protection (continued)

	POWER SUPPLIED THROUGH AC PIN (CASE (1) AND (2))	POWER SUPPLIED THROUGH BAT PIN (CASE (3))
Response to input-over-voltage	Device enters OFF mode. NOTE: If a battery is present in the system, TPS65217 automatically switches from AC to BAT supply when AC input exceeds 6.5 V and back to AC when AC input recovers to safe operating voltage range.	N/A.

I²C BUS OPERATION

The TPS65217 hosts a slave I²C interface that supports data rates up to 400 kbit/s and auto-increment addressing and is compliant to I²C standard 3.0.

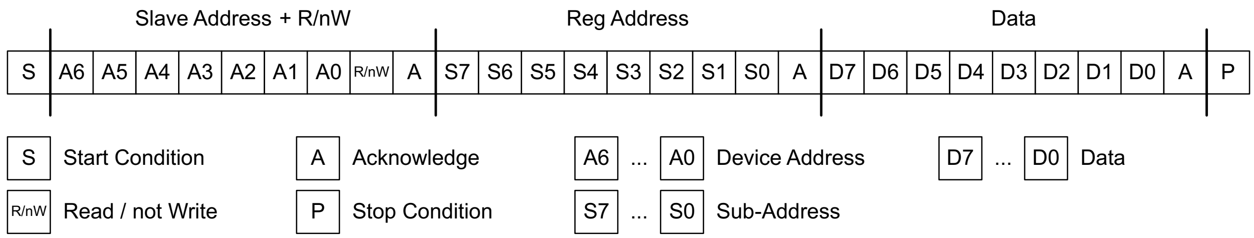

Figure 19. Sub-Address in I²C Transmission

The I²C Bus is a communications link between a controller and a series of slave terminals. The link is established using a two-wired bus consisting of a serial clock signal (SCL) and a serial data signal (SDA). The serial clock is sourced from the controller in all cases where the serial data line is bi-directional for data communication between the controller and the slave terminals. Each device has an open Drain output to transmit data on the serial data line. An external pull-up resistor must be placed on the serial data line to pull the drain output high during data transmission.

Data transmission is initiated with a start bit from the controller as shown in Figure 21. The start condition is recognized when the SDA line transitions from high to low during the high portion of the SCL signal. Upon reception of a start bit, the device will receive serial data on the SDA input and check for valid address and control information. If the appropriate group and address bits are set for the device, then the device will issue an acknowledge pulse and prepare the receive of sub-address data. Sub-address data is decoded and responded to as per the “Register Map” section of this document. Data transmission is completed by either the reception of a stop condition or the reception of the data word sent to the device. A stop condition is recognized as a low to high transition of the SDA input during the high portion of the SCL signal. All other transitions of the SDA line must occur during the low portion of the SCL signal. An acknowledge is issued after the reception of valid address, sub-address and data words. The I²C interfaces will auto-sequence through register addresses, so that multiple data words can be sent for a given I²C transmission. Reference Figure 20 and Figure 21 for detail.

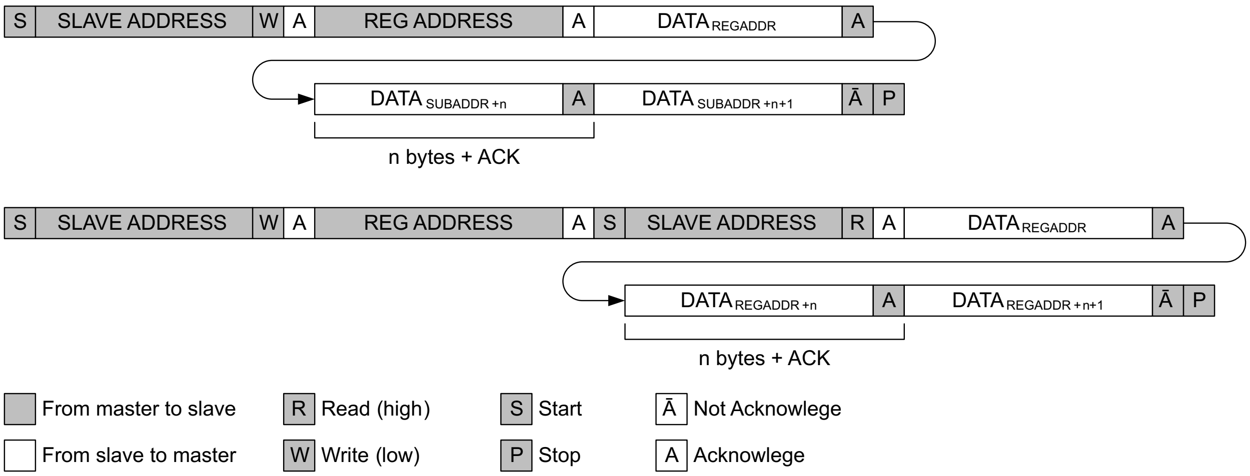

Figure 20. I²C Data Protocol. TOP: Master writes data to slave. BOTTOM: Master reads data from slave.

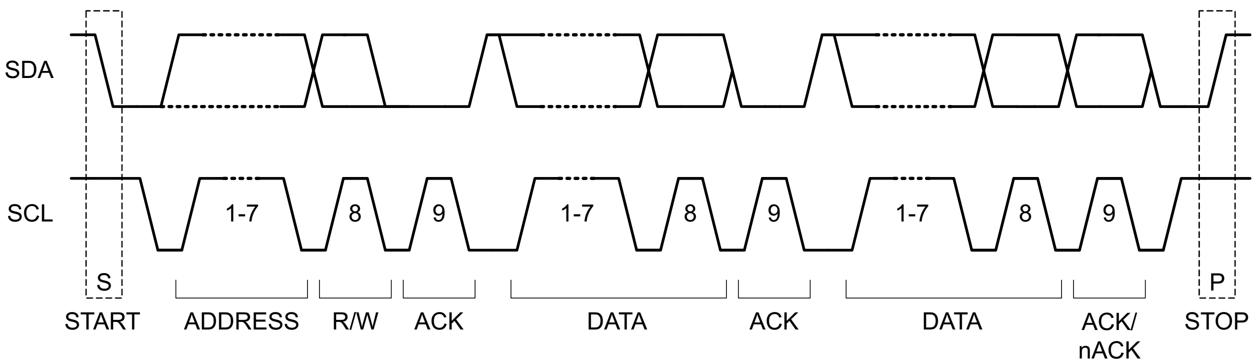

Figure 21. I²C Start/Stop/Acknowledge Protocol

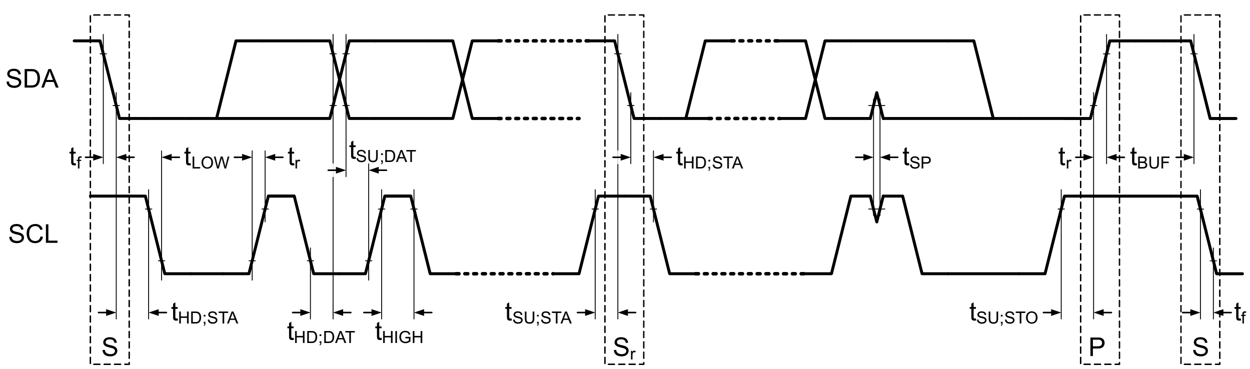

Figure 22. I²C Data Transmission Timing

DATA TRANSMISSION TIMING

V_{BAT} = 3.6 V ±5%, T_A = 25ºC, C_L = 100 pF (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{SCL}	Serial clock frequency		100		400	kHz
$t_{HD;STA}$	Hold time (repeated) START condition. After this period, the first clock pulse is generated	SCL = 100 KHz	4			µs
		SCL = 400 KHz	600			ns
t_{LOW}	LOW period of the SCL clock	SCL = 100 KHz	4.7			µs
		SCL = 400 KHz	1.3			
t_{HIGH}	HIGH period of the SCL clock	SCL = 100 KHz	4			µs
		SCL = 400 KHz	600			ns
$t_{SU;STA}$	Set-up time for a repeated START condition	SCL = 100 KHz	4.7			µs
		SCL = 400 KHz	600			ns
$t_{HD;DAT}$	Data hold time	SCL = 100 KHz	0		3.45	µs
		SCL = 400 KHz	0		900	ns
$t_{SU;DAT}$	Data set-up time	SCL = 100 KHz	250			ns
		SCL = 400 KHz	100			
t_r	Rise time of both SDA and SCL signals	SCL = 100 KHz			1000	ns
		SCL = 400 KHz			300	
t_f	Fall time of both SDA and SCL signals	SCL = 100 KHz			300	ns
		SCL = 400 KHz			300	
$t_{SU;STO}$	Set-up time for STOP condition	SCL = 100 KHz	4			µs
		SCL = 400 KHz	600			ns
t_{BUF}	Bus free time between stop and start condition	SCL = 100 KHz	4.7			µs
		SCL = 400 KHz	1.3			
t_{SP}	Pulse width of spikes which mst be suppressed by the input filter	SCL = 100 KHz	N/A		N/A	
		SCL = 400 KHz	0		50	ns
C_b	Capacitive load for each bus line	SCL = 100 KHz			400	pF
		SCL = 400 KHz			400	

PASSWORD PROTECTION

Registers 0x0B through 0x1F with exception of the password register are protected against accidental write by a 8-bit password. The password needs to be written prior to writing to a protected register and is automatically reset to 0x00h after the following I^2C transaction, regardless of the register that was accessed and regardless of the transaction type (read or write). The password is required for write access only and is not required for read access.

Level1 Protection

To write to a Level1 protected register:

1. Write the address of the destination register, XORed with the protection password (0x7Dh) to the PASSWORD register.
2. Write data to the password protected register.
3. Only if the content of the PASSWORD register XORed with the address send in step 2 matches 0x7Dh, the data will be transferred to the protected register. Otherwise the transaction will be ignored. In any case the PASSWORD register is reset to 0x00 after the transaction.

The cycle needs to be repeated for any other register that is Level1 write protected.

Level2 Protection

To write to a Level2 protected register:

1. Write the address of the destination register, XORed with the protection password (0x7Dh) to the PASSWORD register.
2. Write to the password protected register. The register value will not change at this point but the data will be temporarily stored if the content of the PASSWORD register XORed with the address send in step 2 matches 0x7Dh. In any case, the PASSWORD register is reset to 0x00 after the transaction.
3. Write the address of the destination register, XORed with the protection password (0x7Dh) to the PASSWORD register.
4. Write the same data as in step 2 to the password protected register. Again, the content of the PASSWORD register XORed with the address send in step 4 must match 0x7Dh for the data to be valid.
5. The register will be updated only if both data transfers 2, and 4 were valid, and the transferred data matched.

Note that no other I^2C transaction is allowed between step 2 and 4 and the register will not be updated if any other transaction occurs in-between. The cycle needs to be repeated for any other register that is Level2 write protected.

RESET TO DEFAULT VALUES

All registers are reset to default values when one or more of the following conditions occur:

- The device transitions from ACTIVE state to SLEEP or OFF state.
- VBAT or VUSB is applied from power-less state (Power-On-Reset).
- Push-button input is pulled high for > 8 s.
- nRESET pin is pulled low.
- A fault occurs.

REGISTER ADDRESS MAP

REGISTER	ADDRESS (HEX)	NAME	PROTECTION	DEFAULT VALUE	DESCRIPTION
0	0	CHIPID	None	N/A	Chip ID
1	1	PPATH	None	N/A	Power path control
2	2	INT	None	N/A	Interrupt flags and masks
3	3	CHGCONFIG0	None	N/A	Charger control register 0
4	4	CHGCONFIG1	None	N/A	Charger control register 1
5	5	CHGCONFIG2	None	N/A	Charger control register 2
6	6	CHGCONFIG3	None	N/A	Charger control register 3
7	7	WLEDCTRL1	None	N/A	WLED control register
8	8	WLEDCTRL2	None	N/A	WLED PWM duty cycle
9	9	MUXCTRL	None	N/A	Analog Multiplexer control register
10	0A	STATUS	None	N/A	Status register
11	0B	PASSWORD	None	N/A	Write password
12	0C	PGOOD	None	N/A	Power good (PG) flags
13	0D	DEFPG	Level1	N/A	Power good (PG) delay
14	0E	DEFDCDC1	Level2	N/A	DCDC1 voltage adjustment
15	0F	DEFDCDC2	Level2	N/A	DCDC2 voltage adjustment
16	10	DEFDCDC3	Level2	N/A	DCDC3 voltage adjustment
17	11	DEFSLEW	Level2	N/A	Slew control DCDC1-3/PFM mode enable
18	12	DEFLDO1	Level2	N/A	LDO1 voltage adjustment
19	13	DEFLDO2	Level2	N/A	LDO2 voltage adjustment
20	14	DEFLS1	Level2	N/A	LS1/LDO3 voltage adjustment
21	15	DEFLS2	Level2	N/A	LS2/LDO4 voltage adjustment
22	16	ENABLE	Level1	N/A	Enable register
23	18	DEFUVLO	Level1	N/A	UVLO control register
24	19	SEQ1	Level1	N/A	Power-up STROBE definition
25	1A	SEQ2	Level1	N/A	Power-up STROBE definition
26	1B	SEQ3	Level1	N/A	Power-up STROBE definition
27	1C	SEQ4	Level1	N/A	Power-up STROBE definition
28	1D	SEQ5	Level1	N/A	Power-up delay times
29	1E	SEQ6	Level1	N/A	Power-up delay times

CHIP ID REGISTER (CHIPID)

Address – 0x00h

DATA BIT		D7	D6	D5	D4	D3	D2	D1	D0
FIELD NAME		CHIP[3:0]				REV[3:0]			
READ/WRITE		R	R	R	R	R	R	R	R
RESET VALUE	**TPS65217A**	0	1	1	1	0	0	1	0
	TPS65217B	1	1	1	1	0	0	1	0
	TPS65217C	1	1	1	0	0	0	1	0
	TPS65217D	0	1	1	0	0	0	1	0

FIELD NAME	BIT DEFINITION
CHIP[3:0]	Chip ID 0000 – future use 0001 – future use 0110 – TPS65217D 0111 – TPS65217A 1000 – future use ... 1110 – TPS65217C 1111 – TPS65217B
REV[3:0]	Revision code 0000 – revision 1.0 0001 – revision 1.1 0010 – revision 1.2 ... 1111 – future use

POWER PATH CONTROL REGISTER (PPATH)

Address – 0x01h

DATA BIT	D7	D6	D5	D4	D3	D2	D1	D0
FIELD NAME	ACSINK	USBSINK	AC_EN	USB_EN	IAC[1:0]		IUSB[1:0]	
READ/WRITE	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
RESET VALUE	0	0	1	1	1	1	0	1

FIELD NAME	BIT DEFINITION
ACSINK	AC current sink control 0 – AC sink is enabled when USB is valid supply and V_{AC} is below detection threshold 1 – Set [ACSINK, USBSINK] = 11 to force both (AC and USB) current sinks OFF NOTE: [ACSINK, USBSINK] = 01b and 10b combinations are not recommended as these may lead to unexpected enabling and disabling of the current sinks.
USBSINK	USB current sink control 0 – USB sink is enabled when AC is valid supply and V_{USB} is below detection threshold 1 – Set [ACSINK, USBSINK] = 11 to force both (AC and USB) current sinks OFF NOTE: [ACSINK, USBSINK] = 01b and 10b combinations are not recommended as these may lead to unexpected enabling and disabling of the current sinks.
AC_EN	AC power path enable 0 – AC power input is turned off 1 – AC power input is turned on
USB_EN	USB power path enable 0 – USB power input is turned off (USB suspend mode) 1 – USB power input is turned on
IAC[1:0]	AC input current limit 00 – 100 mA 01 – 500 mA 10 – 1300 mA 11 – 2500 mA
IUSB[1:0]	USB input current limit 00 – 100 mA 01 – 500 mA 10 – 1300 mA 11 – 1800 mA

INTERRUPT REGISTER (INT)

Address – 0x02h

DATA BIT	D7	D6	D5	D4	D3	D2	D1	D0
FIELD NAME	not used	PBM	ACM	USBM	not used	PBI	ACI	USBI
READ/WRITE	R/W	R/W	R/W	R/W	R	R	R	R
RESET VALUE	1	0	0	0	0	0	0	0

FIELD NAME	BIT DEFINITION
not used	N/A
PBM	Pushbutton status change interrupt mask 0 – interrupt is issued when PB status changes 1 – no interrupt is issued when PB status changes
ACM	AC interrupt mask 0 – interrupt is issued when power to AC input is applied or removed 1 – no interrupt is issued when power to AC input is applied or removed
USBM	USB power status change interrupt mask 0 – interrupt is issued when power to USB input is applied or removed 1 – no interrupt is issued when power to USB input is applied or removed
not used	N/A
PBI	Push-button status change interrupt 0 – no change in status 1 – pushbutton status change (PB_IN changed high to low or low to high) NOTE: Status information is available in STATUS register
ACI	AC power status change interrupt 0 – no change in status 1 – AC power status change (power to AC pin has either been applied or removed) NOTE: Status information is available in STATUS register
USBI	USB power status change interrupt 0 – no change in status 1 – USB power status change (power to USB pin has either been applied or removed) NOTE: Status information is available in STATUS register

CHARGER CONFIGURATION REGISTER 0 (CHGCONFIG0)

Address – 0x03h

DATA BIT	D7	D6	D5	D4	D3	D2	D1	D0
FIELD NAME	TREG	DPPM	TSUSP	TERMI	ACTIVE	CHGTOUT	PCHGTOUT	BATTEMP
READ/WRITE	R	R	R	R	R	R	R	R
RESET VALUE	0	0	0	0	0	0	0	0

FIELD NAME	BIT DEFINITION
TREG	Thermal regulation 0 – charger is in normal operation 1 – charge current is reduced due to high chip temperature
DPPM	DPPM active 0 – DPPM loop is not active 1 – DPPM loop is active; charge current is reduced to support the load with the current required
TSUSP	Thermal suspend 0 – charging is allowed 1 – charging is momentarily suspended because battery temperature is out of range
TERMI	Termination current detect 0 – charging, charge termination current threshold has not been crossed 1 – charge termination current threshold has been crossed and charging has been stopped. This can be due to a battery reaching full capacity or to a battery removal condition.
ACTIVE	Charger active bit 0 – charger is not charging 1 – charger is charging (DPPM or thermal regulation may be active)
CHGTOUT	Charge timer time-out 0 – charging, timers did not time out 1 – one of the timers has timed out and charging has been terminated
PCHGTOUT	Pre-charge timer time-out 0 – charging, pre-charge timer did not time out 1 – pre-charge timer has timed out and charging has been terminated
BATTEMP	BAT TEMP/NTC ERROR 0 – battery temperature is in the allowed range for charging 1 – no temperature sensor detected or battery temperature outside valid charging range NOTE: This bit does not indicate that the battery temperature is within the valid range for charging.

CHARGER CONFIGURATION REGISTER 1 (CHGCONFIG1)

Address – 0x04h

DATA BIT	D7	D6	D5	D4	D3	D2	D1	D0
FIELD NAME	TIMER[1:0]		TMR_EN	NTC_TYPE	RESET	TERM	SUSP	CHG_EN
READ/WRITE	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
RESET VALUE	1	0	1	1	0	0	0	1

FIELD NAME	BIT DEFINITION
TIMER[1:0]	Charge safety timer setting (fast charge timer) 00 – 4h 01 – 5h 10 – 6h 11 – 8h
TMR_EN	Safety timer enable 0 – pre-charge timer and fast charge timer are disabled 1 – pre-charge timer and fast charge time are enabled
NTC_TYPE	NTC TYPE (for battery temperature measurement) 0 – 100k (curve 1, B = 3960) 1 – 10k (curve 2, B = 3480)
RESET	Charger reset 0 – inactive 1 – Reset active. This Bit must be set and then reset via the serial interface to restart the charge algorithm.
TERM	Charge termination on/off 0 – charge termination enabled, based on timers and termination current 1 – current-based charge termination will not occur and the charger will always be on
SUSP	Suspend charge 0 – Safety Timer and Pre-Charge timers are not suspended 1 – Safety Timer and Pre-Charge timers are suspended
CHG_EN	Charger enable 0 – charger is disabled 1 – charger is enabled

CHARGER CONFIGURATION REGISTER 2 (CHGCONFIG2)

Address – 0x05h

DATA BIT	D7	D6	D5	D4	D3	D2	D1	D0
FIELD NAME	DYNTMR	VPRECHG	VOREG[1:0]		reserved	reserved	reserved	reserved
READ/WRITE	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
RESET VALUE	1	0	0	0	0	0	0	0

FIELD NAME	BIT DEFINITION
DYNTMR	Dynamic timer function 0 – safety timers run with their nominal clock speed 1 – clock speed is divided by 2 if thermal loop or DPPM loop is active
VPRECHG	Precharge voltage 0 – pre-charge to fast charge transition voltage is 2.9 V 1 – pre-charge to fast charge transition voltage is 2.5 V
VOREG[1:0]	Charge voltage selection 00 – 4.10 V 01 – 4.15 V 10 – 4.20 V 11 – 4.25 V
reserved	This bit should always be set to 0.
reserved	This bit should always be set to 0.
reserved	This bit should always be set to 0.
reserved	This bit should always be set to 0.

CHARGER CONFIGURATION REGISTER 3 (CHGCONFIG3)

Address – 0x06h

DATA BIT	D7	D6	D5	D4	D3	D2	D1	D0
FIELD NAME	ICHRG[1:0]		DPPMTH[1:0]		PCHRGT	TERMIF[1:0]		TRANGE
READ/WRITE	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
RESET VALUE	1	0	1	1	0	0	1	0

FIELD NAME	BIT DEFINITION
ICHRG[1:0]	Charge current setting 00 – 300 mA 01 – 400 mA 10 – 500 mA 11 – 700 mA
DPPMTH[1:0]	Power path DPPM threshold 00 – 3.5 V 01 – 3.75 V 10 – 4.0 V 11 – 4.25 V
PCHRGT	Pre-charge time 0 – 30 min 1 – 60 min
TERMIF[1:0]	Termination current factor 00 – 2.5% 01 – 7.5% 10 – 15% 11 – 18% NOTE: Termination current = TERMIF x ICHRG
TRANGE	Temperature range for charging 0 – 0°C-45°C 1 – 0°C-60°C

WLED CONTROL REGISTER 1 (WLEDCTRL1)

Address – 0x07h

DATA BIT	D7	D6	D5	D4	D3	D2	D1	D0
FIELD NAME	not used	not used	not used	not used	ISINK_EN	ISEL	FDIM[1:0]	
READ/WRITE	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
RESET VALUE	0	0	0	0	0	0	0	1

FIELD NAME	BIT DEFINITION
not used	N/A
not used	N/A
not used	N/A
not used	N/A
ISINK_EN	Current sink enable 0 – current sink is disabled (OFF) 1 – current sink is enabled (ON) NOTE: This bit enables both current sinks
ISEL	ISET selection bit 0 – low-level (define by ISET1 pin) 1 – high-level (defined by ISET2 pin)
FDIM[1:0]	PWM dimming frequency 00 – 100 Hz 01 – 200 Hz 10 – 500 Hz 11 – 1000 Hz

WLED CONTROL REGISTER 2 (WLEDCTRL2)

Address – 0x08h

DATA BIT	D7	D6	D5	D4	D3	D2	D1	D0
FIELD NAME	not used	DUTY[6:0]						
READ/WRITE	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
RESET VALUE	0	0	0	0	0	0	0	0

FIELD NAME	BIT DEFINITION
not used	N/A
DUTY[6:0]	000 0000 – 1% 000 0001 – 2% ... 110 0010 – 99% 110 0011 – 100% 110 0100 – 0% ... 111 1110 – 0% 111 1111 – 0%

MUX CONTROL REGISTER (MUXCTRL)

Address – 0x09h

DATA BIT	D7	D6	D5	D4	D3	D2	D1	D0
FIELD NAME	not used	not used	not used	not used	not used	MUX[2:0]		
READ/WRITE	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
RESET VALUE	0	0	0	0	0	0	0	0

FIELD NAME	BIT DEFINITION
not used	N/A
not used	N/A
not used	N/A
not used	N/A
not used	N/A
MUX[2:0]	Analog multiplexer selection 000 – MUX is disabled, output is HiZ 001 – VBAT 010 – VSYS 011 – VTS 100 – VICHARGE 101 – MUX_IN (external input) 110 – MUX is disabled, output is HiZ 111 – MUX is disabled, output is HiZ

STATUS REGISTER (STATUS)

Address – 0x0Ah

DATA BIT	D7	D6	D5	D4	D3	D2	D1	D0
FIELD NAME	OFF	not used	not used	not used	ACPWR	USBPWR	not used	PB
READ/WRITE	R/W	R/W	R/W	R/W	R	R	R	R
RESET VALUE	0	0	0	0	0	0	0	0

FIELD NAME	BIT DEFINITION
OFF	OFF bit. Set this bit to 1 to enter OFF state when PWR_EN pin is pulled low. Bit is automatically reset to 0.
not used	N/A
not used	N/A
not used	N/A
ACPWR	AC power status bit 0 – AC power is not present and/or not in the range valid for charging 1 – AC source is present and in the range valid for charging
USBPWR	USB power 0 – USB power is not present and/or not in the range valid for charging 1 – USB source is present and in the range valid for charging
not used	N/A
PB	Push Button status bit 0 – Push Button is inactive (PB_IN is pulled high) 1 – Push Button is active (PB_IN is pulled low)

PASSWORD REGISTER (PASSWORD)

Address – 0x0Bh

DATA BIT	D7	D6	D5	D4	D3	D2	D1	D0
FIELD NAME	PWRD[7:0]							
READ/WRITE	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
RESET VALUE	0	0	0	0	0	0	0	0

FIELD NAME	BIT DEFINITION
PWRD[7:0]	0000 0000 – Password protected registers are locked for write access ... 0111 1100 – Password protected registers are locked for write access 0111 1101 – Allows writing to a password protected register in the next write cycle 0111 1110 – Password protected registers are locked for write access ... 1111 1111 – Password protected registers are locked for write access NOTE: Register is automatically reset to 0x00h after following I^2C transaction. See PASSWORD PROTECTION section for details.

POWER GOOD REGISTER (PGOOD)

Address – 0x0Ch

DATA BIT	D7	D6	D5	D4	D3	D2	D1	D0
FIELD NAME	not used	LDO3_PG	LDO4_PG	DC1_PG	DC2_PG	DC3_PG	LDO1_PG	LDO2_PG
READ/WRITE	R/W	R	R	R	R	R	R	R
RESET VALUE	0	0	0	0	0	0	0	0

FIELD NAME	BIT DEFINITION
not used	N/A
LDO3_PG	LDO3 power-good 0 – LDO is either disabled or not in regulation 1 – LDO is in regulation or LS1/LDO3 is configured as switch
LDO4_PG	LDO4 power-good 0 – LDO is either disabled or not in regulation 1 – LDO is in regulation or LS2/LDO4 is configured as switch
DC1_PG	DCDC1 power-good 0 – DCDC is either disabled or not in regulation 1 – DCDC is in regulation
DC2_PG	DCDC2 power-good 0 – DCDC is either disabled or not in regulation 1 – DCDC is in regulation
DC3_PG	DCDC3 power-good 0 – DCDC is either disabled or not in regulation 1 – DCDC is in regulation
LDO1_PG	LDO1 power-good 0 – LDO is either disabled or not in regulation 1 – LDO is in regulation
LDO2_PG	LDO2 power-good 0 – LDO is either disabled or not in regulation 1 – LDO is in regulation

POWER GOOD CONTROL REGISTER (DEFPG)

Address – 0x0Dh (Password Protected)

DATA BIT	D7	D6	D5	D4	D3	D2	D1	D0
FIELD NAME	not used	not used	not used	not used	LDO1PGM	LDO2PGM	PGDLY[1:0]	
READ/WRITE	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
RESET VALUE	0	0	0	0	1	1	0	0

FIELD NAME	BIT DEFINITION
not used	N/A
not used	N/A
not used	N/A
not used	N/A
LDO1PGM	LDO1 power-good masking bit 0 – PGOOD pin is pulled low if LDO1_PG is low 1 – LDO1_PG status does not affect the status of the PGOOD output pin
LDO2PGM	LDO2 power-good masking bit 0 – PGOOD pin is pulled low if LDO2_PG is low 1 – LDO2_PG status does not affect the status of the PGOOD output pin
PGDLY[1:0]	Power Good delay 00 – 20 ms 01 – 100 ms 10 – 200 ms 11 – 400 ms Note: PGDLY applies to PGOOD pin.

DCDC1 CONTROL REGISTER (DEFDCDC1)

Address – 0x0Eh (Password Protected)

DATA BIT		D7	D6	D5	D4	D3	D2	D1	D0
FIELD NAME		XADJ1	not used	DCDC1[5:0]					
READ/WRITE		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
RESET VALUE	TPS65217A	0	0	0	1	1	1	1	0
	TPS65217B	0	0	0	1	1	1	1	0
	TPS65217C	0	0	0	1	1	0	0	0
	TPS65217D	0	0	0	1	0	0	1	0

FIELD NAME	BIT DEFINITION (TPS65217A, TPS65217B)			
XADJ1	DCDC1 voltage adjustment option 0 – Output voltage is adjusted through register setting 1 – Output voltage is externally adjusted			
not used	N/A			
DCDC1[5:0]	DCDC1 output voltage setting			
	00 0000 – 0.900 V	01 0000 – 1.300 V	10 0000 – 1.900 V	11 0000 – 2.700 V
	00 0001 – 0.925 V	01 0001 – 1.325 V	10 0001 – 1.950 V	11 0001 – 2.750 V
	00 0010 – 0.950 V	01 0010 – 1.350 V	10 0010 – 2.000 V	11 0010 – 2.800 V
	00 0011 – 0.975 V	01 0011 – 1.375 V	10 0011 – 2.050 V	11 0011 – 2.850 V
	00 0100 – 1.000 V	01 0100 – 1.400 V	10 0100 – 2.100 V	11 0100 – 2.900 V
	00 0101 – 1.025 V	01 0101 – 1.425 V	10 0101 – 2.150 V	11 0101 – 3.000 V
	00 0110 – 1.050 V	01 0110 – 1.450 V	10 0110 – 2.200 V	11 0110 – 3.100 V
	00 0111 – 1.075 V	01 0111 – 1.475 V	10 0111 – 2.250 V	11 0111 – 3.200 V
	00 1000 – 1.100 V	01 1000 – 1.500 V	10 1000 – 2.300 V	11 1000 – 3.300 V
	00 1001 – 1.125 V	01 1001 – 1.550 V	10 1001 – 2.350 V	11 1001 – 3.300 V
	00 1010 – 1.150 V	01 1010 – 1.600 V	10 1010 – 2.400 V	11 1010 – 3.300 V
	00 1011 – 1.175 V	01 1011 – 1.650 V	10 1011 – 2.450 V	11 1011 – 3.300 V
	00 1100 – 1.200 V	01 1100 – 1.700 V	10 1100 – 2.500 V	11 1100 – 3.300 V
	00 1101 – 1.225 V	01 1101 – 1.750 V	10 1101 – 2.550 V	11 1101 – 3.300 V
	00 1110 – 1.250 V	**01 1110 – 1.800 V**	10 1110 – 2.600 V	11 1110 – 3.300 V
	00 1111 – 1.275 V	01 1111 – 1.850 V	10 1111 – 2.650 V	11 1111 – 3.300 V

FIELD NAME	BIT DEFINITION (TPS65217C)			
XADJ1	DCDC1 voltage adjustment option 0 – Output voltage is adjusted through register setting 1 – Output voltage is externally adjusted			
not used	N/A			
DCDC1[5:0]	DCDC1 output voltage setting			
	00 0000 – 0.900 V	01 0000 – 1.300 V	10 0000 – 1.900 V	11 0000 – 2.700 V
	00 0001 – 0.925 V	01 0001 – 1.325 V	10 0001 – 1.950 V	11 0001 – 2.750 V
	00 0010 – 0.950 V	01 0010 – 1.350 V	10 0010 – 2.000 V	11 0010 – 2.800 V
	00 0011 – 0.975 V	01 0011 – 1.375 V	10 0011 – 2.050 V	11 0011 – 2.850 V
	00 0100 – 1.000 V	01 0100 – 1.400 V	10 0100 – 2.100 V	11 0100 – 2.900 V
	00 0101 – 1.025 V	01 0101 – 1.425 V	10 0101 – 2.150 V	11 0101 – 3.000 V
	00 0110 – 1.050 V	01 0110 – 1.450 V	10 0110 – 2.200 V	11 0110 – 3.100 V
	00 0111 – 1.075 V	01 0111 – 1.475 V	10 0111 – 2.250 V	11 0111 – 3.200 V
	00 1000 – 1.100 V	**01 1000 – 1.500 V**	10 1000 – 2.300 V	11 1000 – 3.300 V
	00 1001 – 1.125 V	01 1001 – 1.550 V	10 1001 – 2.350 V	11 1001 – 3.300 V
	00 1010 – 1.150 V	01 1010 – 1.600 V	10 1010 – 2.400 V	11 1010 – 3.300 V
	00 1011 – 1.175 V	01 1011 – 1.650 V	10 1011 – 2.450 V	11 1011 – 3.300 V
	00 1100 – 1.200 V	01 1100 – 1.700 V	10 1100 – 2.500 V	11 1100 – 3.300 V
	00 1101 – 1.225 V	01 1101 – 1.750 V	10 1101 – 2.550 V	11 1101 – 3.300 V
	00 1110 – 1.250 V	01 1110 – 1.800 V	10 1110 – 2.600 V	11 1110 – 3.300 V
	00 1111 – 1.275 V	01 1111 – 1.850 V	10 1111 – 2.650 V	11 1111 – 3.300 V

FIELD NAME	BIT DEFINITION (TPS65217D)			
XADJ1	DCDC1 voltage adjustment option 0 – Output voltage is adjusted through register setting 1 – Output voltage is externally adjusted			
not used	N/A			
DCDC1[5:0]	DCDC1 output voltage setting			
	00 0000 – 0.900 V	01 0000 – 1.300 V	10 0000 – 1.900 V	11 0000 – 2.700 V
	00 0001 – 0.925 V	01 0001 – 1.325 V	10 0001 – 1.950 V	11 0001 – 2.750 V
	00 0010 – 0.950 V	**01 0010 – 1.350 V**	10 0010 – 2.000 V	11 0010 – 2.800 V
	00 0011 – 0.975 V	01 0011 – 1.375 V	10 0011 – 2.050 V	11 0011 – 2.850 V
	00 0100 – 1.000 V	01 0100 – 1.400 V	10 0100 – 2.100 V	11 0100 – 2.900 V
	00 0101 – 1.025 V	01 0101 – 1.425 V	10 0101 – 2.150 V	11 0101 – 3.000 V
	00 0110 – 1.050 V	01 0110 – 1.450 V	10 0110 – 2.200 V	11 0110 – 3.100 V
	00 0111 – 1.075 V	01 0111 – 1.475 V	10 0111 – 2.250 V	11 0111 – 3.200 V
	00 1000 – 1.100 V	01 1000 – 1.500 V	10 1000 – 2.300 V	11 1000 – 3.300 V
	00 1001 – 1.125 V	01 1001 – 1.550 V	10 1001 – 2.350 V	11 1001 – 3.300 V
	00 1010 – 1.150 V	01 1010 – 1.600 V	10 1010 – 2.400 V	11 1010 – 3.300 V
	00 1011 – 1.175 V	01 1011 – 1.650 V	10 1011 – 2.450 V	11 1011 – 3.300 V
	00 1100 – 1.200 V	01 1100 – 1.700 V	10 1100 – 2.500 V	11 1100 – 3.300 V
	00 1101 – 1.225 V	01 1101 – 1.750 V	10 1101 – 2.550 V	11 1101 – 3.300 V
	00 1110 – 1.250 V	01 1110 – 1.800 V	10 1110 – 2.600 V	11 1110 – 3.300 V
	00 1111 – 1.275 V	01 1111 – 1.850 V	10 1111 – 2.650 V	11 1111 – 3.300 V

DCDC2 CONTROL REGISTER (DEFDCDC2)

Address – 0x0Fh (Password Protected)

DATA BIT		D7	D6	D5	D4	D3	D2	D1	D0
FIELD NAME		XADJ2	not used	DCDC2[5:0]					
READ/WRITE		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
RESET VALUE	TPS65217A	0	0	1	1	1	0	0	0
	TPS65217B	0	0	0	0	1	0	0	0
	TPS65217C	0	0	0	0	1	0	0	0
	TPS65217D	0	0	0	0	1	0	0	0

FIELD NAME	BIT DEFINITION (TPS65217A)			
XADJ2	DCDC2 voltage adjustment option 0 – Output voltage is adjusted through register setting 1 – Output voltage is externally adjusted			
not used	N/A			
DCDC2[5:0]	DCDC2 output voltage setting			
	00 0000 – 0.900 V	01 0000 – 1.300 V	10 0000 – 1.900 V	11 0000 – 2.700 V
	00 0001 – 0.925 V	01 0001 – 1.325 V	10 0001 – 1.950 V	11 0001 – 2.750 V
	00 0010 – 0.950 V	01 0010 – 1.350 V	10 0010 – 2.000 V	11 0010 – 2.800 V
	00 0011 – 0.975 V	01 0011 – 1.375 V	10 0011 – 2.050 V	11 0011 – 2.850 V
	00 0100 – 1.000 V	01 0100 – 1.400 V	10 0100 – 2.100 V	11 0100 – 2.900 V
	00 0101 – 1.025 V	01 0101 – 1.425 V	10 0101 – 2.150 V	11 0101 – 3.000 V
	00 0110 – 1.050 V	01 0110 – 1.450 V	10 0110 – 2.200 V	11 0110 – 3.100 V
	00 0111 – 1.075 V	01 0111 – 1.475 V	10 0111 – 2.250 V	11 0111 – 3.200 V
	00 1000 – 1.100 V	01 1000 – 1.500 V	10 1000 – 2.300 V	**11 1000 – 3.300 V**
	00 1001 – 1.125 V	01 1001 – 1.550 V	10 1001 – 2.350 V	11 1001 – 3.300 V
	00 1010 – 1.150 V	01 1010 – 1.600 V	10 1010 – 2.400 V	11 1010 – 3.300 V
	00 1011 – 1.175 V	01 1011 – 1.650 V	10 1011 – 2.450 V	11 1011 – 3.300 V
	00 1100 – 1.200 V	01 1100 – 1.700 V	10 1100 – 2.500 V	11 1100 – 3.300 V
	00 1101 – 1.225 V	01 1101 – 1.750 V	10 1101 – 2.550 V	11 1101 – 3.300 V
	00 1110 – 1.250 V	01 1110 – 1.800 V	10 1110 – 2.600 V	11 1110 – 3.300 V
	00 1111 – 1.275 V	01 1111 – 1.850 V	10 1111 – 2.650 V	11 1111 – 3.300 V

FIELD NAME	BIT DEFINITION (TPS65217B, TPS65217C, TPS65217D)			
XADJ2	DCDC2 voltage adjustment option 0 – Output voltage is adjusted through register setting 1 – Output voltage is externally adjusted			
not used	N/A			
DCDC2[5:0]	DCDC2 output voltage setting			
	00 0000 – 0.900 V	01 0000 – 1.300 V	10 0000 – 1.900 V	11 0000 – 2.700 V
	00 0001 – 0.925 V	01 0001 – 1.325 V	10 0001 – 1.950 V	11 0001 – 2.750 V
	00 0010 – 0.950 V	01 0010 – 1.350 V	10 0010 – 2.000 V	11 0010 – 2.800 V
	00 0011 – 0.975 V	01 0011 – 1.375 V	10 0011 – 2.050 V	11 0011 – 2.850 V
	00 0100 – 1.000 V	01 0100 – 1.400 V	10 0100 – 2.100 V	11 0100 – 2.900 V
	00 0101 – 1.025 V	01 0101 – 1.425 V	10 0101 – 2.150 V	11 0101 – 3.000 V
	00 0110 – 1.050 V	01 0110 – 1.450 V	10 0110 – 2.200 V	11 0110 – 3.100 V
	00 0111 – 1.075 V	01 0111 – 1.475 V	10 0111 – 2.250 V	11 0111 – 3.200 V
	00 1000 – 1.100 V	01 1000 – 1.500 V	10 1000 – 2.300 V	11 1000 – 3.300 V
	00 1001 – 1.125 V	01 1001 – 1.550 V	10 1001 – 2.350 V	11 1001 – 3.300 V
	00 1010 – 1.150 V	01 1010 – 1.600 V	10 1010 – 2.400 V	11 1010 – 3.300 V
	00 1011 – 1.175 V	01 1011 – 1.650 V	10 1011 – 2.450 V	11 1011 – 3.300 V
	00 1100 – 1.200 V	01 1100 – 1.700 V	10 1100 – 2.500 V	11 1100 – 3.300 V
	00 1101 – 1.225 V	01 1101 – 1.750 V	10 1101 – 2.550 V	11 1101 – 3.300 V
	00 1110 – 1.250 V	01 1110 – 1.800 V	10 1110 – 2.600 V	11 1110 – 3.300 V
	00 1111 – 1.275 V	01 1111 – 1.850 V	10 1111 – 2.650 V	11 1111 – 3.300 V

DCDC3 CONTROL REGISTER (DEFDCDC3)

Address – 0x10h (Password Protected)

DATA BIT	D7	D6	D5	D4	D3	D2	D1	D0
FIELD NAME	XADJ3	not used	DCDC3[5:0]					
READ/WRITE	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
RESET VALUE	0	0	0	0	1	0	0	0

FIELD NAME	BIT DEFINITION			
XADJ3	DCDC3 voltage adjustment option 0 – Output voltage is adjusted through register setting 1 – Output voltage is externally adjusted			
not used	N/A			
DCDC3[5:0]	DCDC3 output voltage setting			
	00 0000 – 0.900 V	01 0000 – 1.300 V	10 0000 – 1.900 V	11 0000 – 2.700 V
	00 0001 – 0.925 V	01 0001 – 1.325 V	10 0001 – 1.950 V	11 0001 – 2.750 V
	00 0010 – 0.950 V	01 0010 – 1.350 V	10 0010 – 2.000 V	11 0010 – 2.800 V
	00 0011 – 0.975 V	01 0011 – 1.375 V	10 0011 – 2.050 V	11 0011 – 2.850 V
	00 0100 – 1.000 V	01 0100 – 1.400 V	10 0100 – 2.100 V	11 0100 – 2.900 V
	00 0101 – 1.025 V	01 0101 – 1.425 V	10 0101 – 2.150 V	11 0101 – 3.000 V
	00 0110 – 1.050 V	01 0110 – 1.450 V	10 0110 – 2.200 V	11 0110 – 3.100 V
	00 0111 – 1.075 V	01 0111 – 1.475 V	10 0111 – 2.250 V	11 0111 – 3.200 V
	00 1000 – 1.100 V	01 1000 – 1.500 V	10 1000 – 2.300 V	11 1000 – 3.300 V
	00 1001 – 1.125 V	01 1001 – 1.550 V	10 1001 – 2.350 V	11 1001 – 3.300 V
	00 1010 – 1.150 V	01 1010 – 1.600 V	10 1010 – 2.400 V	11 1010 – 3.300 V
	00 1011 – 1.175 V	01 1011 – 1.650 V	10 1011 – 2.450 V	11 1011 – 3.300 V
	00 1100 – 1.200 V	01 1100 – 1.700 V	10 1100 – 2.500 V	11 1100 – 3.300 V
	00 1101 – 1.225 V	01 1101 – 1.750 V	10 1101 – 2.550 V	11 1101 – 3.300 V
	00 1110 – 1.250 V	01 1110 – 1.800 V	10 1110 – 2.600 V	11 1110 – 3.300 V
	00 1111 – 1.275 V	01 1111 – 1.850 V	10 1111 – 2.650 V	11 1111 – 3.300 V

SLEW RATE CONTROL REGISTER (DEFSLEW)

Address – 0x11h (Password Protected)

DATA BIT	D7	D6	D5	D4	D3	D2	D1	D0
FIELD NAME	GO	GODSBL	PFM_EN1	PFM_EN2	PFM_EN3	SLEW[2:0]		
READ/WRITE	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
RESET VALUE	0	0	0	0	0	1	1	0

FIELD NAME	BIT DEFINITION (1)
GO	Go bit 0 – no change 1 – Initiates the transition from present state to the output voltage setting currently stored in DEFDCDCx register NOTE: Bit is automatically reset at the end of the voltage transition.
GODSBL	Go disable bit 0 – enabled 1 – disabled; DCDCx output voltage changes whenever set-point is updated in DEFDCDCx register without having to write to the GO bit. SLEW[2:0] setting does apply.
PFM_EN1	PFM enable bit, DCDC1 0 – DCDC converter operates in PWM / PFM mode, depending on load 1 – DCDC converter is forced into fixed frequency PWM mode
PFM_EN2	PFM enable bit, DCDC2 0 – DCDC converter operates in PWM / PFM mode, depending on load 1 – DCDC converter is forced into fixed frequency PWM mode
PFM_EN3	PFM enable bit, DCDC3 0 – DCDC converter operates in PWM / PFM mode, depending on load 1 – DCDC converter is forced into fixed frequency PWM mode
SLEW[2:0]	Output slew rate setting 000 – 224 µs/step (0.11 mV/µs at 25 mV per step) 001 – 112 µs/step (0.22 mV/µs at 25 mV per step) 010 – 56 µs/step (0.45 mV/µs at 25 mV per step) 011 – 28 µs/step (0.90 mV/µs at 25 mV per step) 100 – 14 µs/step (1.80 mV/µs at 25 mV per step) 101 – 7 µs/step (3.60 mV/µs at 25 mV per step) 110 – 3.5 µs/step (7.2 mV/µs at 25 mV per step) 111 – Immediate; Slew rate is only limited by control loop response time Note: The actual slew rate depends on the voltage step per code. Please refer to DCDC1 and DCDC2 register for details.

(1) Slew-rate control applies to all three DCDC converters.

LDO1 CONTROL REGISTER (DEFLDO1)

Address – 0x12h (Password Protected)

DATA BIT	D7	D6	D5	D4	D3	D2	D1	D0
FIELD NAME	not used	not used	not used	not used	LDO1[3:0]			
READ/WRITE	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
RESET VALUE	0	0	0	0	1	0	0	1

FIELD NAME	BIT DEFINITION			
not used	N/A			
not used	N/A			
not used	N/A			
not used	N/A			
LDO1[3:0]	LDO1 output voltage setting			
	0000 – 1.00 V	0100 – 1.30 V	1000 – 1.60 V	1100 – 2.80 V
	0001 – 1.10 V	0101 – 1.35 V	1001 – 1.80 V	1101 – 3.00 V
	0010 – 1.20 V	0110 – 1.40 V	1010 – 2.50 V	1110 – 3.10 V
	0011 – 1.25 V	0111 – 1.50 V	1011 – 2.75 V	1111 – 3.30 V

LDO2 CONTROL REGISTER (DEFLDO2)

Address – 0x13h (Password Protected)

DATA BIT	D7	D6	D5	D4	D3	D2	D1	D0
FIELD NAME	not used	TRACK	LDO2[5:0]					
READ/WRITE	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
RESET VALUE	0	0	1	1	1	0	0	0

FIELD NAME	BIT DEFINITION			
not used	N/A			
TRACK	LDO2 tracking bit 0 – Output voltage is defined by LDO2[5:0] bits 1 – Output voltage follows DCDC3 voltage setting (DEFDCDC3 register)			
LDO2[5:0]	LDO2 output voltage setting			
	00 0000 – 0.900 V	01 0000 – 1.300 V	10 0000 – 1.900 V	11 0000 – 2.700 V
	00 0001 – 0.925 V	01 0001 – 1.325 V	10 0001 – 1.950 V	11 0001 – 2.750 V
	00 0010 – 0.950 V	01 0010 – 1.350 V	10 0010 – 2.000 V	11 0010 – 2.800 V
	00 0011 – 0.975 V	01 0011 – 1.375 V	10 0011 – 2.050 V	11 0011 – 2.850 V
	00 0100 – 1.000 V	01 0100 – 1.400 V	10 0100 – 2.100 V	11 0100 – 2.900 V
	00 0101 – 1.025 V	01 0101 – 1.425 V	10 0101 – 2.150 V	11 0101 – 3.000 V
	00 0110 – 1.050 V	01 0110 – 1.450 V	10 0110 – 2.200 V	11 0110 – 3.100 V
	00 0111 – 1.075 V	01 0111 – 1.475 V	10 0111 – 2.250 V	11 0111 – 3.200 V
	00 1000 – 1.100 V	01 1000 – 1.500 V	10 1000 – 2.300 V	11 1000 – 3.300 V
	00 1001 – 1.125 V	01 1001 – 1.550 V	10 1001 – 2.350 V	11 1001 – 3.300 V
	00 1010 – 1.150 V	01 1010 – 1.600 V	10 1010 – 2.400 V	11 1010 – 3.300 V
	00 1011 – 1.175 V	01 1011 – 1.650 V	10 1011 – 2.450 V	11 1011 – 3.300 V
	00 1100 – 1.200 V	01 1100 – 1.700 V	10 1100 – 2.500 V	11 1100 – 3.300 V
	00 1101 – 1.225 V	01 1101 – 1.750 V	10 1101 – 2.550 V	11 1101 – 3.300 V
	00 1110 – 1.250 V	01 1110 – 1.800 V	10 1110 – 2.600 V	11 1110 – 3.300 V
	00 1111 – 1.275 V	01 1111 – 1.850 V	10 1111 – 2.650 V	11 1111 – 3.300 V

LOAD SWITCH1 / LDO3 CONTROL REGISTER (DEFLS1)

Address – 0x14h (Password Protected)

DATA BIT		D7	D6	D5	D4	D3	D2	D1	D0
FIELD NAME		not used	not used	LS1LDO3	LDO3[4:0]				
READ/WRITE		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
RESET VALUE	TPS65217A	0	0	0	0	0	1	1	0
	TPS65217B	0	0	1	1	1	1	1	1
	TPS65217C	0	0	1	0	0	1	1	0
	TPS65217D	0	0	1	0	0	1	1	0

FIELD NAME	BIT DEFINITION (TPS65217A)			
not used	N/A			
not used	N/A			
LS1LDO3	LS / LDO configuration bit 0 – FET functions as load switch (LS1) 1 – FET is configured as LDO3			
LDO3[4:0]	LDO3 output voltage setting (LS1LDO3 = 1)			
	0 0000 – 1.50 V	0 1000 – 1.90 V	1 0000 – 2.55 V	1 1000 – 2.95 V
	0 0001 – 1.55 V	0 1001 – 2.00 V	1 0001 – 2.60 V	1 1001 – 3.00 V
	0 0010 – 1.60 V	0 1010 – 2.10 V	1 0010 – 2.65 V	1 1010 – 3.05 V
	0 0011 – 1.65 V	0 1011 – 2.20 V	1 0011 – 2.70 V	1 1011 – 3.10 V
	0 0100 – 1.70 V	0 1100 – 2.30 V	1 0100 – 2.75 V	1 1100 – 3.15 V
	0 0101 – 1.75 V	0 1101 – 2.40 V	1 0101 – 2.80 V	1 1101 – 3.20 V
	0 0110 – 1.80 V	0 1110 – 2.45 V	1 0110 – 2.85 V	1 1110 – 3.25 V
	0 0111 – 1.85 V	0 1111 – 2.50 V	1 0111 – 2.90 V	1 1111 – 3.30 V

FIELD NAME	BIT DEFINITION (TPS65217B)			
not used	N/A			
not used	N/A			
LS1LDO3	LS / LDO configuration bit 0 – FET functions as load switch (LS1) 1 – FET is configured as LDO3			
LDO3[4:0]	LDO3 output voltage setting (LS1LDO3 = 1)			
	0 0000 – 1.50 V	0 1000 – 1.90 V	1 0000 – 2.55 V	1 1000 – 2.95 V
	0 0001 – 1.55 V	0 1001 – 2.00 V	1 0001 – 2.60 V	1 1001 – 3.00 V
	0 0010 – 1.60 V	0 1010 – 2.10 V	1 0010 – 2.65 V	1 1010 – 3.05 V
	0 0011 – 1.65 V	0 1011 – 2.20 V	1 0011 – 2.70 V	1 1011 – 3.10 V
	0 0100 – 1.70 V	0 1100 – 2.30 V	1 0100 – 2.75 V	1 1100 – 3.15 V
	0 0101 – 1.75 V	0 1101 – 2.40 V	1 0101 – 2.80 V	1 1101 – 3.20 V
	0 0110 – 1.80 V	0 1110 – 2.45 V	1 0110 – 2.85 V	1 1110 – 3.25 V
	0 0111 – 1.85 V	0 1111 – 2.50 V	1 0111 – 2.90 V	**1 1111 – 3.30 V**

<table>
<tr><th>FIELD NAME</th><th colspan="4">BIT DEFINITION (TPS65217C, TPS65217D)</th></tr>
<tr><td>not used</td><td colspan="4">N/A</td></tr>
<tr><td>not used</td><td colspan="4">N/A</td></tr>
<tr><td>LS1LDO3</td><td colspan="4">LS / LDO configuration bit
0 – FET functions as load switch (LS1)
1 – FET is configured as LDO3</td></tr>
<tr><td rowspan="9">LDO3[4:0]</td><td colspan="4">LDO3 output voltage setting (LS1LDO3 = 1)</td></tr>
<tr><td>0 0000 – 1.50 V</td><td>0 1000 – 1.90 V</td><td>1 0000 – 2.55 V</td><td>1 1000 – 2.95 V</td></tr>
<tr><td>0 0001 – 1.55 V</td><td>0 1001 – 2.00 V</td><td>1 0001 – 2.60 V</td><td>1 1001 – 3.00 V</td></tr>
<tr><td>0 0010 – 1.60 V</td><td>0 1010 – 2.10 V</td><td>1 0010 – 2.65 V</td><td>1 1010 – 3.05 V</td></tr>
<tr><td>0 0011 – 1.65 V</td><td>0 1011 – 2.20 V</td><td>1 0011 – 2.70 V</td><td>1 1011 – 3.10 V</td></tr>
<tr><td>0 0100 – 1.70 V</td><td>0 1100 – 2.30 V</td><td>1 0100 – 2.75 V</td><td>1 1100 – 3.15 V</td></tr>
<tr><td>0 0101 – 1.75 V</td><td>0 1101 – 2.40 V</td><td>1 0101 – 2.80 V</td><td>1 1101 – 3.20 V</td></tr>
<tr><td>0 0110 – 1.80 V</td><td>0 1110 – 2.45 V</td><td>1 0110 – 2.85 V</td><td>1 1110 – 3.25 V</td></tr>
<tr><td>0 0111 – 1.85 V</td><td>0 1111 – 2.50 V</td><td>1 0111 – 2.90 V</td><td>1 1111 – 3.30 V</td></tr>
</table>

LOAD SWITCH2 / LDO4 CONTROL REGISTER (DEFLS2)

Address – 0x15h (Password Protected)

DATA BIT		D7	D6	D5	D4	D3	D2	D1	D0
FIELD NAME		not used	not used	LS2LDO4	LDO4[4:0]				
READ/WRITE		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
RESET VALUE	TPS65217A	0	0	0	1	0	1	0	1
	TPS65217B	0	0	1	1	1	1	1	1
	TPS65217C	0	0	1	1	1	1	1	1
	TPS65217D	0	0	1	1	1	1	1	1

FIELD NAME	BIT DEFINITION (TPS65217A)			
not used	N/A			
not used	N/A			
LS2LDO4	LS / LDO configuration bit 0 – FET functions as load switch (LS2) 1 – FET is configured as LDO4			
LDO4[4:0]	LDO4 output voltage setting (LS2LDO4 = 1)			
	0 0000 – 1.50 V	0 1000 – 1.90 V	1 0000 – 2.55 V	1 1000 – 2.95 V
	0 0001 – 1.55 V	0 1001 – 2.00 V	1 0001 – 2.60 V	1 1001 – 3.00 V
	0 0010 – 1.60 V	0 1010 – 2.10 V	1 0010 – 2.65 V	1 1010 – 3.05 V
	0 0011 – 1.65 V	0 1011 – 2.20 V	1 0011 – 2.70 V	1 1011 – 3.10 V
	0 0100 – 1.70 V	0 1100 – 2.30 V	1 0100 – 2.75 V	1 1100 – 3.15 V
	0 0101 – 1.75 V	0 1101 – 2.40 V	**1 0101 – 2.80 V**	1 1101 – 3.20 V
	0 0110 – 1.80 V	0 1110 – 2.45 V	1 0110 – 2.85 V	1 1110 – 3.25 V
	0 0111 – 1.85 V	0 1111 – 2.50 V	1 0111 – 2.90 V	1 1111 – 3.30 V

FIELD NAME	BIT DEFINITION (TPS65217B, TPS65217C, TPS65217D)			
not used	N/A			
not used	N/A			
LS2LDO4	LS / LDO configuration bit 0 – FET functions as load switch (LS2) 1 – FET is configured as LDO4			
LDO4[4:0]	LDO4 output voltage setting (LS2LDO4 = 1)			
	0 0000 – 1.50 V	0 1000 – 1.90 V	1 0000 – 2.55 V	1 1000 – 2.95 V
	0 0001 – 1.55 V	0 1001 – 2.00 V	1 0001 – 2.60 V	1 1001 – 3.00 V
	0 0010 – 1.60 V	0 1010 – 2.10 V	1 0010 – 2.65 V	1 1010 – 3.05 V
	0 0011 – 1.65 V	0 1011 – 2.20 V	1 0011 – 2.70 V	1 1011 – 3.10 V
	0 0100 – 1.70 V	0 1100 – 2.30 V	1 0100 – 2.75 V	1 1100 – 3.15 V
	0 0101 – 1.75 V	0 1101 – 2.40 V	1 0101 – 2.80 V	1 1101 – 3.20 V
	0 0110 – 1.80 V	0 1110 – 2.45 V	1 0110 – 2.85 V	1 1110 – 3.25 V
	0 0111 – 1.85 V	0 1111 – 2.50 V	1 0111 – 2.90 V	**1 1111 – 3.30 V**

ENABLE REGISTER (ENABLE)

Address – 0x16h (Password Protected)

DATA BIT	D7	D6	D5	D4	D3	D2	D1	D0
FIELD NAME	not used	LS1_EN	LS2_EN	DC1_EN	DC2_EN	DC3_EN	LDO1_EN	LDO2_EN
READ/WRITE	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
RESET VALUE	0	0	0	0	0	0	0	0

FIELD NAME	BIT DEFINITION
not used	N/A
LS1_EN	Load Switch1/LDO3 enable bit 0 – disabled 1 – enabled NOTE: PWR_EN pin must be high to enable LS1/LDO3
LS2_EN	Load Switch2/LDO4 enable bit 0 – disabled 1 – enabled NOTE: PWR_EN pin must be high to enable LS2/LDO4
DC1_EN	DCDC1 enable bit 0 – DCDC1 is disabled 1 – DCDC1 is enabled NOTE: PWR_EN pin must be high to enable DCDC
DC2_EN	DCDC2 enable bit 0 – DCDC2 is disabled 1 – DCDC2 is enabled NOTE: PWR_EN pin must be high to enable DCDC
DC3_EN	DCDC3 enable bit 0 – DCDC3 is disabled 1 – DCDC3 is enabled NOTE: PWR_EN pin must be high to enable DCDC
LDO1_EN	LDO1 enable bit 0 – disabled 1 – enabled
LDO2_EN	LDO2 enable bit 0 – disabled 1 – enabled

UVLO CONTROL REGISTER (DEFUVLO)

Address – 0x18h (Password Protected)

DATA BIT	D7	D6	D5	D4	D3	D2	D1	D0
FIELD NAME	not used	not used	not used	not used	not used	not used	UVLO[1:0]	
READ/WRITE	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
RESET VALUE	0	0	0	0	0	0	1	1

FIELD NAME	BIT DEFINITION
not used	N/A
not used	N/A
not used	N/A
not used	N/A
not used	N/A
not used	N/A
UVLO[1:0]	Under Voltage Lock Out setting 00 – 2.73 V 01 – 2.89 V 10 – 3.18 V 11 – 3.30 V

SEQUENCER REGISTER 1 (SEQ1)

Address – 0x19h (Password Protected)

DATA BIT		D7	D6	D5	D4	D3	D2	D1	D0
FIELD NAME		DC1_SEQ[3:0]				DC2_SEQ[3:0]			
READ/WRITE		R	R/W	R/W	R/W	R	R/W	R/W	R/W
RESET VALUE	TPS65217A	0	0	0	1	0	0	1	0
	TPS65217B	0	0	0	1	0	1	0	1
	TPS65217C	0	0	0	1	0	1	0	1
	TPS65217D	0	0	0	1	0	1	0	1

FIELD NAME	BIT DEFINITION (TPS65217A)
DC1_SEQ[3:0]	DCDC1 enable STROBE 0000 – rail is not controlled by sequencer **0001 – enable at STROBE1** 0010 – enable at STROBE2 0011 – enable at STROBE3 0100 – enable at STROBE4 0101 – enable at STROBE5 0110 – enable at STROBE6 0111 – enable at STROBE7
DC2_SEQ[3:0]	DCDC2 enable state 0000 – rail is not controlled by sequencer 0001 – enable at STROBE1 **0010 – enable at STROBE2** 0011 – enable at STROBE3 0100 – enable at STROBE4 0101 – enable at STROBE5 0110 – enable at STROBE6 0111 – enable at STROBE7

FIELD NAME	BIT DEFINITION (TPS65217B, TPS65217C, TPS65217D)
DC1_SEQ[3:0]	DCDC1 enable STROBE 0000 – rail is not controlled by sequencer **0001 – enable at STROBE1** 0010 – enable at STROBE2 0011 – enable at STROBE3 0100 – enable at STROBE4 0101 – enable at STROBE5 0110 – enable at STROBE6 0111 – enable at STROBE7
DC2_SEQ[3:0]	DCDC2 enable state 0000 – rail is not controlled by sequencer 0001 – enable at STROBE1 0010 – enable at STROBE2 0011 – enable at STROBE3 0100 – enable at STROBE4 **0101 – enable at STROBE5** 0110 – enable at STROBE6 0111 – enable at STROBE7

SEQUENCER REGISTER 2 (SEQ2)

Address – 0x1Ah (Password Protected)

DATA BIT		D7	D6	D5	D4	D3	D2	D1	D0
FIELD NAME		DC3_SEQ[3:0]				LDO1_SEQ[3:0]			
READ/WRITE		R	R/W	R/W	R/W	R/W	R/W	R/W	R/W
RESET VALUE	TPS65217A	0	0	1	1	1	0	1	1
	TPS65217B	0	1	0	1	1	1	1	1
	TPS65217C	0	1	0	1	1	1	1	1
	TPS65217D	0	1	0	1	1	1	1	1

FIELD NAME	BIT DEFINITION (TPS65217A)
DC3_SEQ[3:0]	DCDC3 enable STROBE 0000 – rail is not controlled by sequencer 0001 – enable at STROBE1 0010 – enable at STROBE2 **0011 – enable at STROBE3** 0100 – enable at STROBE4 0101 – enable at STROBE5 0110 – enable at STROBE6 0111 – enable at STROBE7
LDO1_SEQ[3:0]	LDO1 enable state 0000 – rail is not controlled by sequencer 0001 – enable at STROBE1 0010 – enable at STROBE2 0011 – enable at STROBE3 0100 – enable at STROBE4 0101 – enable at STROBE5 0110 – enable at STROBE6 0111 – enable at STROBE7 1000 – rail is not controlled by sequencer 1001 – rail is not controlled by sequencer ... 1110 – enable at STROBE14 **1111 – enabled at STROBE15 (with SYS)**

FIELD NAME	BIT DEFINITION (TPS65217B, TPS65217C, TPS65217D)
DC3_SEQ[3:0]	DCDC3 enable STROBE 0000 – rail is not controlled by sequencer 0001 – enable at STROBE1 0010 – enable at STROBE2 0011 – enable at STROBE3 0100 – enable at STROBE4 **0101 – enable at STROBE5** 0110 – enable at STROBE6 0111 – enable at STROBE7
LDO1_SEQ[3:0]	LDO1 enable state 0000 – rail is not controlled by sequencer 0001 – enable at STROBE1 0010 – enable at STROBE2 0011 – enable at STROBE3 0100 – enable at STROBE4 0101 – enable at STROBE5 0110 – enable at STROBE6 0111 – enable at STROBE7 1000 – rail is not controlled by sequencer 1001 – rail is not controlled by sequencer ... 1110 – enable at STROBE14 **1111 – enabled at STROBE15 (with SYS)**

SEQUENCER REGISTER 3 (SEQ3)

Address – 0x1Bh (Password Protected)

DATA BIT		D7	D6	D5	D4	D3	D2	D1	D0
FIELD NAME		LDO2_SEQ[3:0]				LDO3_SEQ[3:0]			
READ/WRITE		R/WR	R/W	R/W	R/W	R	R/W	R/W	R/W
RESET VALUE	**TPS65217A**	0	0	1	0	0	0	0	1
	TPS65217B	0	0	1	0	0	0	1	1
	TPS65217C	0	0	1	1	0	0	1	0
	TPS65217D	0	0	1	1	0	0	1	0

FIELD NAME	BIT DEFINITION (TPS65217A)
LDO2_SEQ[3:0]	LDO2 enable STROBE 0000 – rail is not controlled by sequencer 0001 – enable at STROBE1 **0010 – enable at STROBE2** 0011 – enable at STROBE3 0100 – enable at STROBE4 0101 – enable at STROBE5 0110 – enable at STROBE6 0111 – enable at STROBE7 1000 – rail is not controlled by sequencer 1001 – rail is not controlled by sequencer ... 1110 – enable at STROBE14 1111 – enabled at STROBE15 (with SYS)
LDO3_SEQ[3:0]	LS1/LDO3 enable state 0000 – rail is not controlled by sequencer **0001 – enable at STROBE1** 0010 – enable at STROBE2 0011 – enable at STROBE3 0100 – enable at STROBE4 0101 – enable at STROBE5 0110 – enable at STROBE6 0111 – enable at STROBE7

FIELD NAME	BIT DEFINITION (TPS65217B)
LDO2_SEQ[3:0]	LDO2 enable STROBE 0000 – rail is not controlled by sequencer 0001 – enable at STROBE1 **0010 – enable at STROBE2** 0011 – enable at STROBE3 0100 – enable at STROBE4 0101 – enable at STROBE5 0110 – enable at STROBE6 0111 – enable at STROBE7 1000 – rail is not controlled by sequencer 1001 – rail is not controlled by sequencer ... 1110 – enable at STROBE14 1111 – enabled at STROBE15 (with SYS)
LDO3_SEQ[3:0]	LS1/LDO3 enable state 0000 – rail is not controlled by sequencer 0001 – enable at STROBE1 0010 – enable at STROBE2 **0011 – enable at STROBE3** 0100 – enable at STROBE4 0101 – enable at STROBE5 0110 – enable at STROBE6 0111 – enable at STROBE7

FIELD NAME	BIT DEFINITION (TPS65217C, TPS65217D)
LDO2_SEQ[3:0]	LDO2 enable STROBE 0000 – rail is not controlled by sequencer 0001 – enable at STROBE1 0010 – enable at STROBE2 **0011 – enable at STROBE3** 0100 – enable at STROBE4 0101 – enable at STROBE5 0110 – enable at STROBE6 0111 – enable at STROBE7 1000 – rail is not controlled by sequencer 1001 – rail is not controlled by sequencer ... 1110 – enable at STROBE14 1111 – enabled at STROBE15 (with SYS)
LDO3_SEQ[3:0]	LS1/LDO3 enable state 0000 – rail is not controlled by sequencer 0001 – enable at STROBE1 **0010 – enable at STROBE2** 0011 – enable at STROBE3 0100 – enable at STROBE4 0101 – enable at STROBE5 0110 – enable at STROBE6 0111 – enable at STROBE7

SEQUENCER REGISTER 4 (SEQ4)

Address – 0x1Ch (Password Protected)

DATA BIT	D7	D6	D5	D4	D3	D2	D1	D0
FIELD NAME	LDO4_SEQ[3:0]				not used	not used	not used	not used
READ/WRITE	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W
RESET VALUE	0	1	0	0	0	0	0	0

FIELD NAME	BIT DEFINITION
LDO4_SEQ[3:0]	LS2/LDO4 enable STROBE 0000 – rail is not controlled by sequencer 0001 – enable at STROBE1 0010 – enable at STROBE2 0011 – enable at STROBE3 0100 – enable at STROBE4 0101 – enable at STROBE5 0110 – enable at STROBE6 0111 – enable at STROBE7
not used	N/A
not used	N/A
not used	N/A
not used	N/A

SEQUENCER REGISTER 5 (SEQ5)

Address – 0x1Dh (Password Protected)

DATA BIT		D7	D6	D5	D4	D3	D2	D1	D0
FIELD NAME		DLY1[1:0]		DLY2[1:0]		DLY3[1:0]		DLY4[1:0]	
READ/WRITE		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
RESET VALUE	TPS65217A	1	0	0	0	0	0	0	0
	TPS65217B	1	0	0	0	0	0	0	0
	TPS65217C	0	0	1	0	0	0	0	0
	TPS65217D	0	0	1	0	0	0	0	0

FIELD NAME	BIT DEFINITION (TPS65217A, TPS65217B)
DLY1[1:0]	Delay1 time 00 – 1 ms 01 – 2 ms **10 – 5 ms** 11 – 10 ms
DLY2[1:0]	Delay2 time **00 – 1 ms** 01 – 2 ms 10 – 5 ms 11 – 10 ms
DLY3[1:0]	Delay3 time **00 – 1 ms** 01 – 2 ms 10 – 5 ms 11 – 10 ms
DLY4[1:0]	Delay4 time **00 – 1 ms** 01 – 2 ms 10 – 5 ms 11 – 10 ms

FIELD NAME	BIT DEFINITION (TPS65217C, TPS65217D)
DLY1[1:0]	Delay1 time **00 – 1 ms** 01 – 2 ms 10 – 5 ms 11 – 10 ms
DLY2[1:0]	Delay2 time 00 – 1 ms 01 – 2 ms **10 – 5 ms** 11 – 10 ms
DLY3[1:0]	Delay3 time **00 – 1 ms** 01 – 2 ms 10 – 5 ms 11 – 10 ms
DLY4[1:0]	Delay4 time **00 – 1 ms** 01 – 2 ms 10 – 5 ms 11 – 10 ms

SEQUENCER REGISTER 6 (SEQ6)

Address – 0x1Eh (Password Protected)

DATA BIT	D7	D6	D5	D4	D3	D2	D1	D0
FIELD NAME	DLY5[1:0]		DLY6[1:0]		not used	SEQUP	SEQDWN	INSTDWN
READ/WRITE	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
RESET VALUE	0	0	0	0	0	0	0	0

FIELD NAME	BIT DEFINITION
DLY5[1:0]	Delay5 time 00 – 1 ms 01 – 2 ms 10 – 5 ms 11 – 10 ms
DLY6[1:0]	Delay6 time 00 – 1 ms 01 – 2 ms 10 – 5 ms 11 – 10 ms
not used	N/A
SEQUP	Set this bit to 1 to trigger a power-up sequence. Bit is automatically reset to 0.
SEQDWN	Set this bit to 1 to trigger a power-down sequence. Bit is automatically reset to 0.
INSTDWN	Instant shut-down bit 0 – shut-down follows reverse power-up sequence 1 – all delays are bypassed and all rails are shut-down simultaneously NOTE: Shut-down occurs when PWR_EN pin is pulled low or SEQDWN bit is set. Only those rails controlled by the sequencer will be shut down.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS65217ARSLR	ACTIVE	VQFN	RSL	48	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 105	TPS 65217A	Samples
TPS65217ARSLT	ACTIVE	VQFN	RSL	48	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 105	TPS 65217A	Samples
TPS65217BRSLR	ACTIVE	VQFN	RSL	48	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 105	TPS 65217B	Samples
TPS65217BRSLT	ACTIVE	VQFN	RSL	48	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 105	TPS 65217B	Samples
TPS65217CRSLR	ACTIVE	VQFN	RSL	48	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 105	TPS 65217C	Samples
TPS65217CRSLT	ACTIVE	VQFN	RSL	48	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 105	TPS 65217C	Samples
TPS65217DRSLR	ACTIVE	VQFN	RSL	48	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 105	TPS 65217D	Samples
TPS65217DRSLT	ACTIVE	VQFN	RSL	48	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 105	TPS 65217D	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

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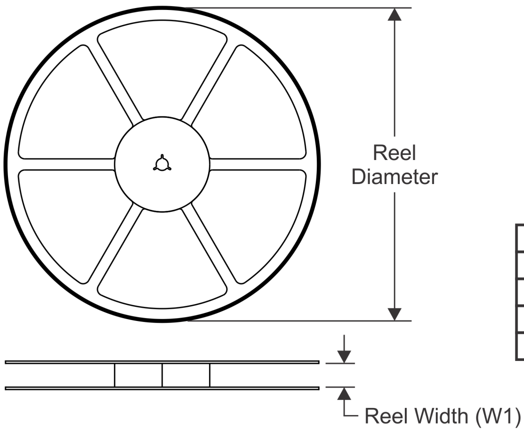
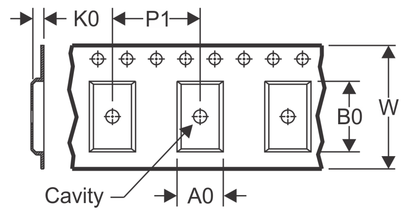
TAPE AND REEL INFORMATION

REEL DIMENSIONS

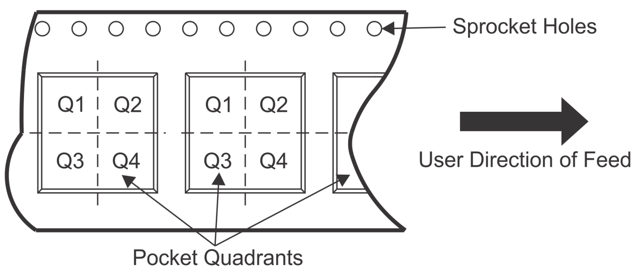


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

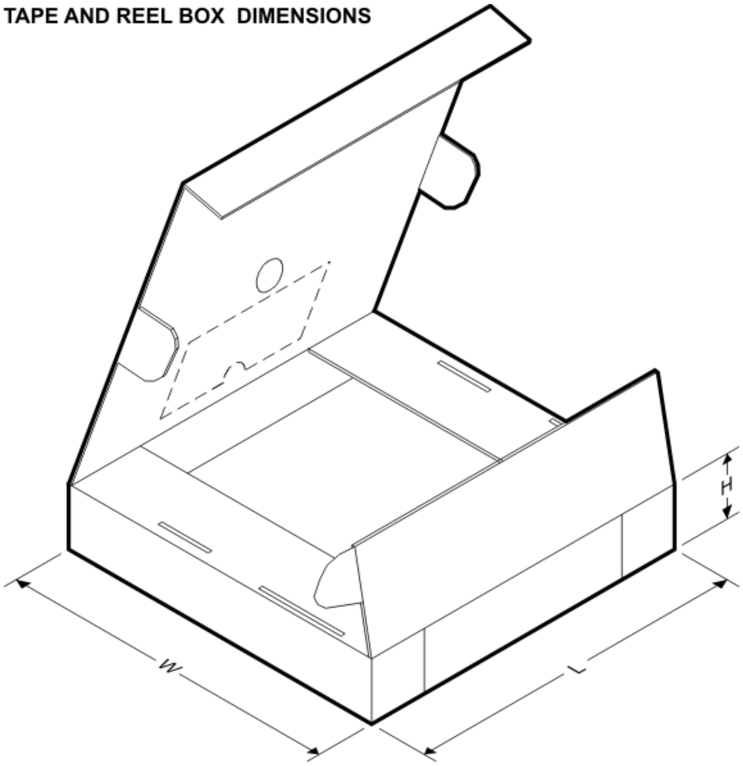
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS65217ARSLR	VQFN	RSL	48	2500	330.0	16.4	6.3	6.3	1.1	12.0	16.0	Q2
TPS65217ARSLT	VQFN	RSL	48	250	180.0	16.4	6.3	6.3	1.1	12.0	16.0	Q2
TPS65217BRSLR	VQFN	RSL	48	2500	330.0	16.4	6.3	6.3	1.1	12.0	16.0	Q2
TPS65217BRSLT	VQFN	RSL	48	250	180.0	16.4	6.3	6.3	1.1	12.0	16.0	Q2
TPS65217CRSLR	VQFN	RSL	48	2500	330.0	16.4	6.3	6.3	1.1	12.0	16.0	Q2
TPS65217CRSLT	VQFN	RSL	48	250	180.0	16.4	6.3	6.3	1.1	12.0	16.0	Q2
TPS65217DRSLR	VQFN	RSL	48	2500	330.0	16.4	6.3	6.3	1.1	12.0	16.0	Q2
TPS65217DRSLT	VQFN	RSL	48	250	180.0	16.4	6.3	6.3	1.1	12.0	16.0	Q2

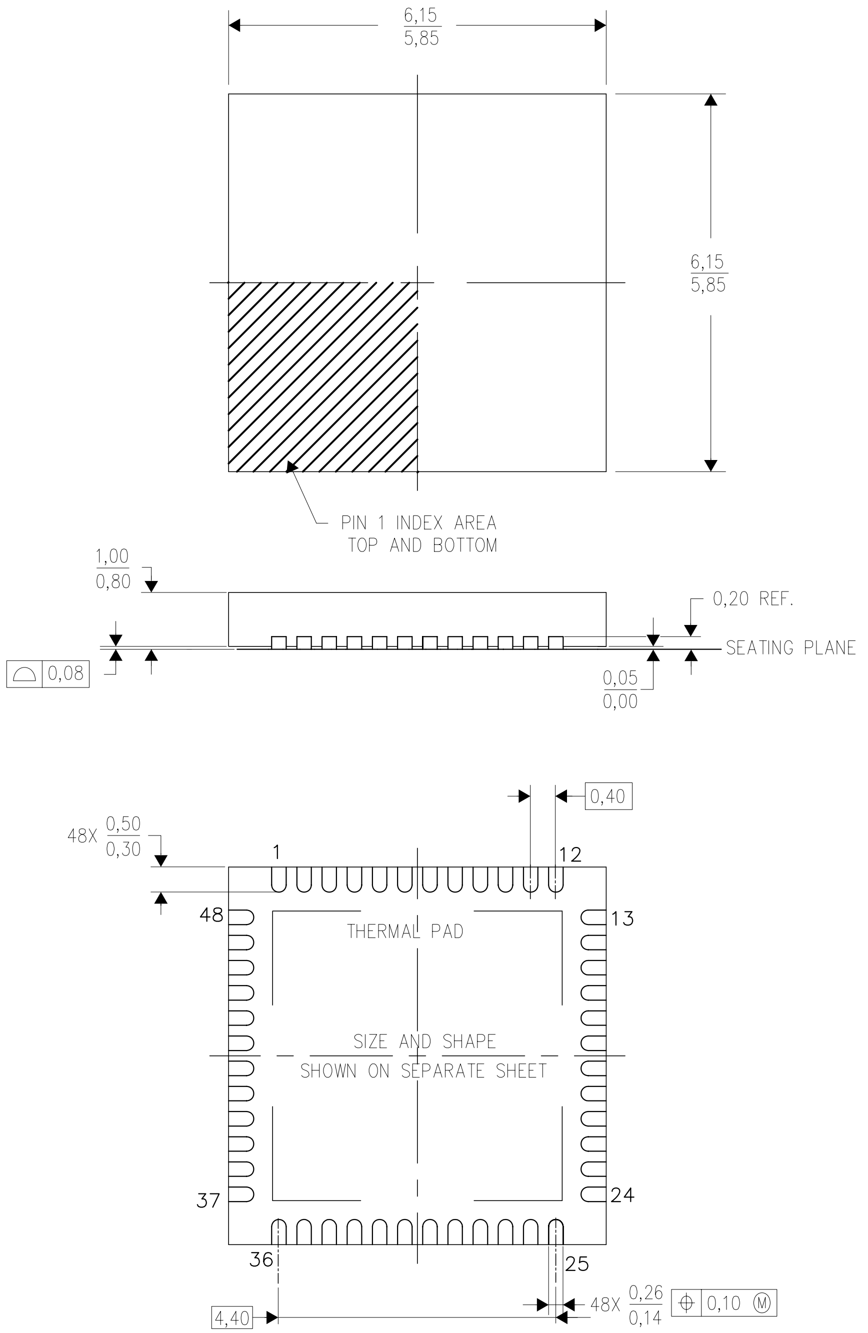
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS65217ARSLR	VQFN	RSL	48	2500	367.0	367.0	38.0
TPS65217ARSLT	VQFN	RSL	48	250	210.0	185.0	35.0
TPS65217BRSLR	VQFN	RSL	48	2500	367.0	367.0	38.0
TPS65217BRSLT	VQFN	RSL	48	250	210.0	185.0	35.0
TPS65217CRSLR	VQFN	RSL	48	2500	367.0	367.0	38.0
TPS65217CRSLT	VQFN	RSL	48	250	210.0	185.0	35.0
TPS65217DRSLR	VQFN	RSL	48	2500	367.0	367.0	38.0
TPS65217DRSLT	VQFN	RSL	48	250	210.0	185.0	35.0

RSL (S–PVQFN–N48) PLASTIC QUAD FLATPACK NO–LEAD



4207548/B 06/11

NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Quad Flatpack, No–leads (QFN) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.

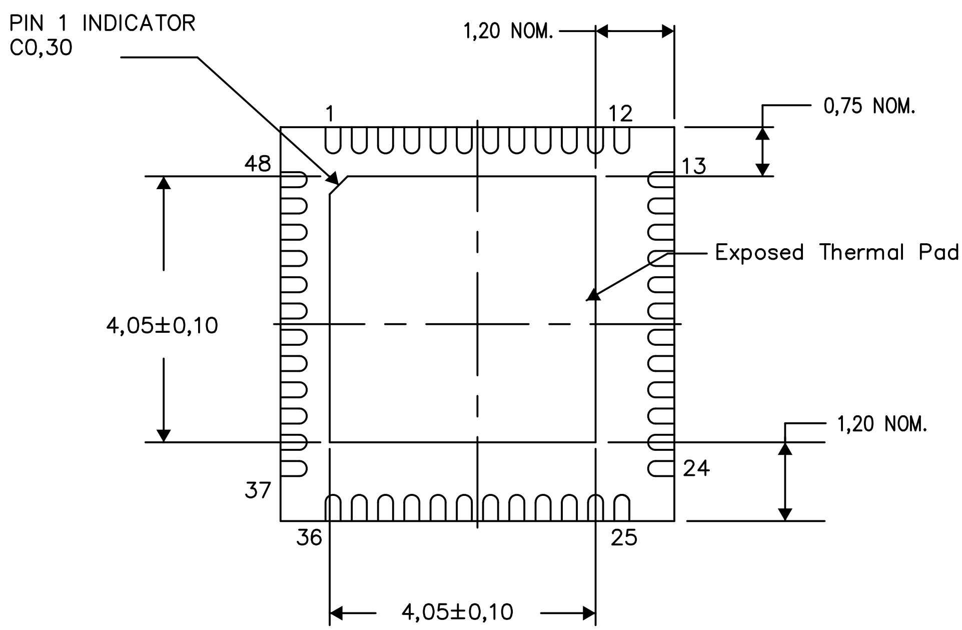
RSL (S–PVQFN–N48) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



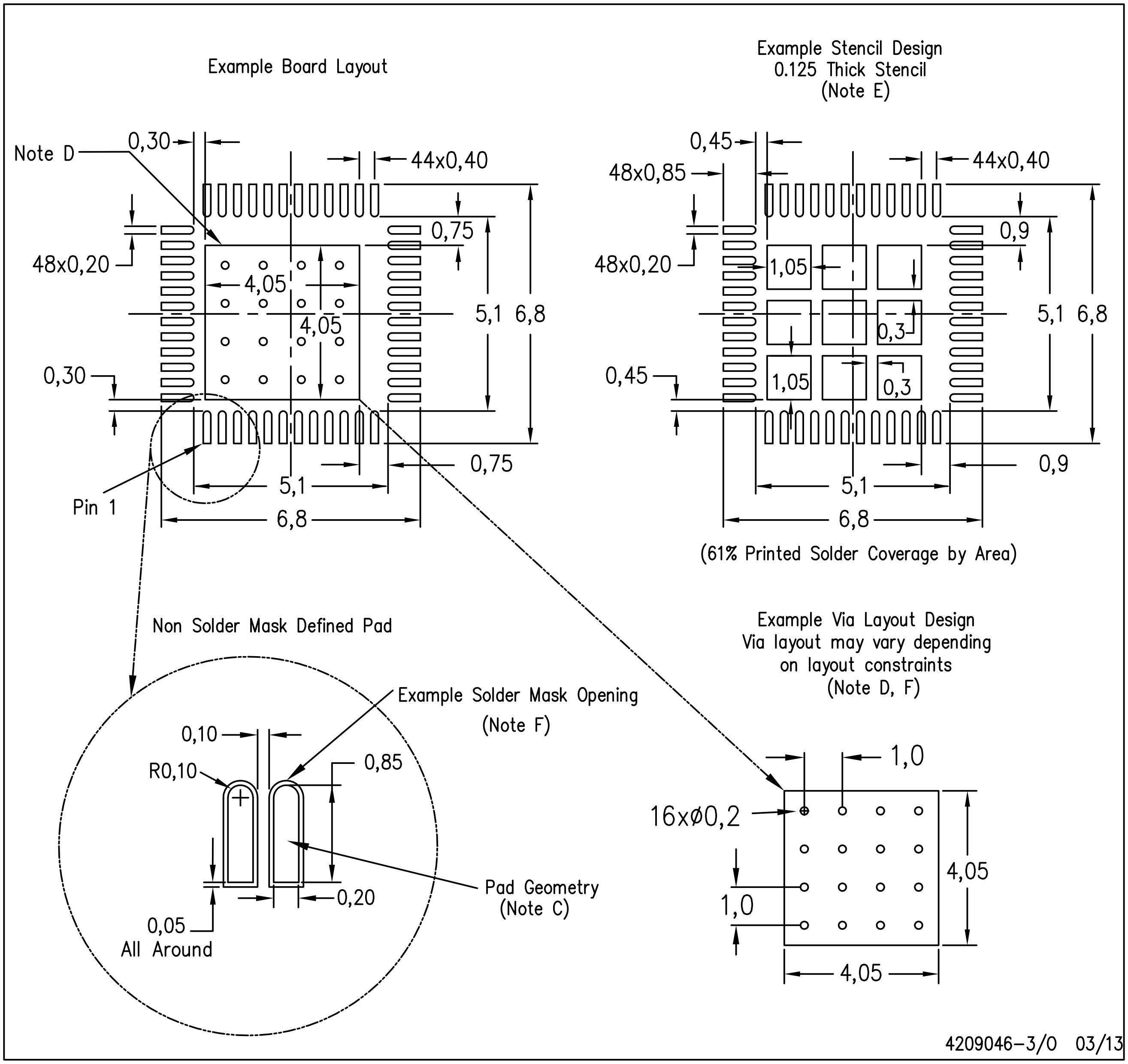
Bottom View

Exposed Thermal Pad Dimensions

4207841-4/P 03/13

NOTE: All linear dimensions are in millimeters

RSL (S–PVQFN–N48) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:

A. All linear dimensions are in millimeters.

B. This drawing is subject to change without notice.

C. Publication IPC–7351 is recommended for alternate designs.

D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http: //www.ti.com>.

E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.

F. Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for vias placed in the thermal pad.

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