NCV47711

5 V to 20 V Adjustable LDO with Adjustable Current Limit and 3.3 V Logic Compatible Enable Input

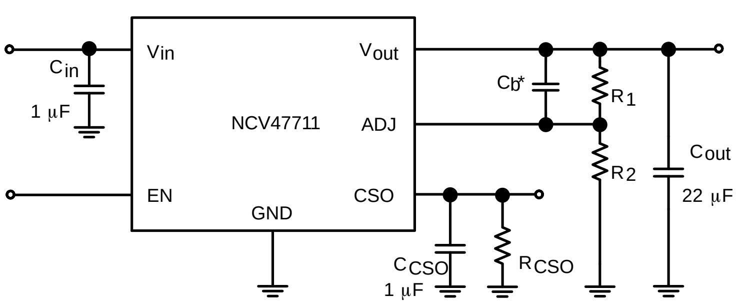
The NCV47711 is a 350 mA output current integrated low dropout regulator designed for use in harsh automotive environments. It includes wide operating temperature and input voltage ranges. The device is offered with adjustable voltage versions available in 3% output voltage accuracy. It has a high peak input voltage tolerance and reverse input voltage protection. It also provides overcurrent protection, overtemperature protection and enable for control of the state of the output voltage. The integrated current sense feature provides diagnosis and system protection functionality. The current limit of the device is adjustable by resistor connected to CSO pin. Voltage on CSO pin is proportional to output current.

Features

- Adjustable Voltage Version (from 5 V to 20 V) ± 3% Output Voltage for ±6% Output Voltage Accuracy see NCV47710 Specification
- Enable Input (3.3 V Logic Compatible Thresholds) for 5 V Logic Compatible Thresholds see NCV47700 or NCV47701 Specification
- Adjustable Current Limit (from 10 mA to 350 mA) with 10% accuracy
- Protection Features:
  - Current Limitation
  - Thermal Shutdown
  - Reverse Input Voltage
- This is a Pb−Free Device

Typical Applications

- Audio and Infotainment System
- Instrument Cluster
- Navigation
- Satellite Radio



*Required if usage of low ESR output capacitor C_{out} is demand, see Regulator Stability Considerations section.

Figure 1. Application Schematic

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MARKING DIAGRAMS

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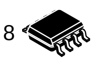

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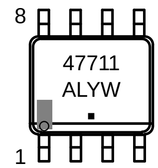
SOIC−8 Exposed Pad PD SUFFIX CASE 751AC



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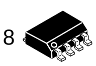

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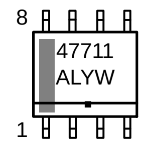
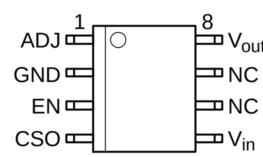
SOIC−8 D SUFFIX CASE 751



A	= Assembly Location
L	= Wafer Lot
Y	= Year
W	= Work Week
▪	= Pb−Free Package

PIN CONNECTIONS



SOIC−8 EP, SOIC−8

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 10 of this data sheet.

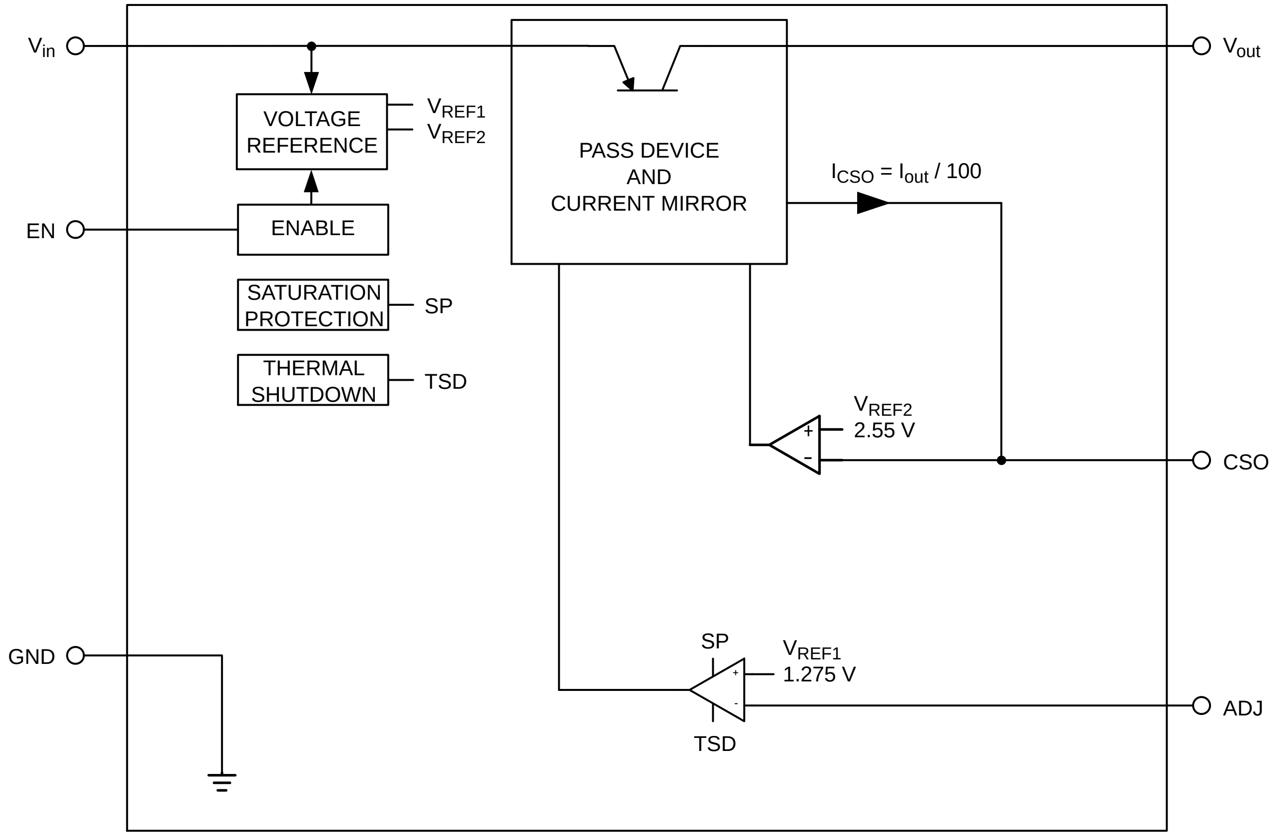


Figure 2. Simplified Block Diagram

PIN FUNCTION DESCRIPTION

Pin No. SOIC−8 EP	Pin No. SOIC−8	Pin Name	Description
1	1	ADJ	Adjustable Voltage Setting Input. See Application Section for more details.
2	2	GND	Power Supply Ground.
3	3	EN	Enable Input; low level disables the IC.
4	4	CSO	Current Sense Output, Current Limit setting and Output Current value information. See Application Section for more details.
5	5	V_{in}	Positive Power Supply Input.
6	6	NC	Not Connected
7	7	NC	Not Connected
8	8	V_{out}	Regulated Output Voltage.
EPAD	−	EPAD	Connect to ground potential or leave unconnected.

ABSOLUTE MAXIMUM RATINGS (Note 1)

Rating	Symbol	Min	Max	Unit
Input Voltage	V_{in}	−42	45	V
Enable Input Voltage	V_{EN}	−0.3	7.0	V
Adjustable Input Voltage	V_{ADJ}	−0.3	10	V
CSO Voltage	V_{CSO}	−0.3	7.0	V
Output Voltage	V_{out}	−1	40	V
Junction Temperature	T_J	−40	150	°C
Storage Temperature	T_{STG}	−55	150	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Refer to ELECTRICAL CHARACTERISTICS and APPLICATION INFORMATION for Safe Operating Area.

ESD CAPABILITY (Note 2)

Rating	Symbol	Min	Max	Unit
ESD Capability, Human Body Model	ESD_{HBM}	−2	2	kV
ESD Capability, Machine Model	ESD_{MM}	−200	200	V

2. This device series incorporates ESD protection and is tested by the following methods:
   ESD Human Body Model tested per AEC−Q100−002 (JS−001−2010)
   ESD Machine Model tested per AEC−Q100−003 (EIA/JESD22−A115)
   Field Induced Charge Device Model ESD characterization is not performed on plastic molded packages with body sizes < 50mm^2 due to the inability of a small package body to acquire and retain enough charge to meet the minimum CDM discharge current waveform characteristic defined in JEDEC JS−002−2014.

LEAD SOLDERING TEMPERATURE AND MSL (Note 3)

Rating		Symbol	Min	Max	Unit
Moisture Sensitivity Level	SOIC−8 EP SOIC−8	MSL	2 1		−

3. For more information, please refer to our Soldering and Mounting Techniques Reference Manual, SOLDERRM/D

THERMAL CHARACTERISTICS

Rating	Symbol	Value	Unit
Thermal Characteristics, SOIC−8 EP (single layer PCB) Thermal Resistance, Junction−to−Air (Note 4) Thermal Reference, Junction−to−Lead (Note 4)	 $R_{\theta JA}$ $R_{\psi JL}$	 70 19	°C/W
Thermal Characteristics, SOIC−8 EP (4 layers PCB) Thermal Resistance, Junction−to−Air (Note 4) Thermal Reference, Junction−to−Lead (Note 4)	 $R_{\theta JA}$ $R_{\psi JL}$	 29 12	°C/W
Thermal Characteristics, SOIC−8 (single layer PCB) Thermal Resistance, Junction−to−Air (Note 4) Thermal Reference, Junction−to−Lead (Note 4)	 $R_{\theta JA}$ $R_{\psi JL}$	 121 42	°C/W
Thermal Characteristics, SOIC−8 (4 layers PCB) Thermal Resistance, Junction−to−Air (Note 4) Thermal Reference, Junction−to−Lead (Note 4)	 $R_{\theta JA}$ $R_{\psi JL}$	 77 52	°C/W

4. Values based on copper area of 645 mm^2 (or 1 in^2) of 1 oz copper thickness and FR4 PCB substrate. Single layer − according to JEDEC51.3, 4 layers − according to JEDEC51.7.

RECOMMENDED OPERATING RANGES

Rating	Symbol	Min	Max	Unit
Input Voltage (Note 5)	V_{in}	5.5	40	V
Output Current Limit (Note 6)	I_{LIM}	10	350	mA
Junction Temperature	T_J	−40	150	°C
Nominal Output Voltage	V_{out_nom}	5.0	20	V
Current Sense Output (CSO) Capacitor	C_{CSO}	1.0	4.7	μF

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

5. Minimum V_{in} = 5.5 V or (V_{out_nom} + 0.5 V), whichever is higher.
6. Corresponding R_{CSO} is in range from 25 kΩ down to 728 Ω.

ELECTRICAL CHARACTERISTICS V_{in} = 13.5 V, V_{EN} = 3.3 V, R_{CSO} = 0 Ω, C_{CSO} = 1 μF, C_{in} = 1 μF, C_{out} = 22 μF, ESR = 1.5 Ω, Min and Max values are valid for temperature range −40°C ≤ T_J ≤ 150°C unless otherwise noted and are guaranteed by test design or statistical correlation. Typical values are referenced to T_J = 25°C.

Parameter	Test Conditions	Symbol	Min	Typ	Max	Unit
REGULATOR OUTPUT						
Output Voltage (Accuracy %)	V_{in} = (V_{out_nom} + 1 V) to 40 V, I_{out} = 5 mA to 350 mA	V_{out}	−3	–	3	%
Line Regulation	V_{in} = (V_{out_nom} + 1 V) to (V_{out_nom} + 20V), I_{out} = 5mA	Reg_{line}	–	0.1	1.0	%
Load Regulation	I_{out} = 5 mA to 350 mA	Reg_{load}	–	0.14	1.4	%
Dropout Voltage (Note 7)	I_{out} = 150 mA, V_{DO} = V_{in} − V_{out}	V_{DO}	–	250	500	mV
DISABLE AND QUIESCENT CURRENTS						
Disable Current	V_{EN} = 0 V V_{EN} = 0 V, T_J = 25°C	I_{DIS}	– –	– 85	10 –	μA nA
Quiescent Current, I_q = I_{in} − I_{out}	I_{out} = 1 mA, V_{in} = (V_{out_nom} + 8.5 V)	I_q	–	150	230	μA
Quiescent Current, I_q = I_{in} − I_{out}	I_{out} = 350 mA, V_{in} = (V_{out_nom} + 8.5 V)	I_q	–	23	50	mA
CURRENT LIMIT PROTECTION						
Current Limit	V_{out} = 0.9 x V_{out_nom}, V_{in} = (V_{out_nom} + 8.5 V)	I_{LIM}	400	–	–	mA
PSRR & NOISE						
Power Supply Ripple Rejection	f = 100 Hz, 0.5 V_{p-p}, I_{out} = 5 mA, C_{in} = none	PSRR	–	70	–	dB
Output Noise Voltage	f = 10 Hz to 100 kHz, C_b = 10 nF, I_{out} = 5 mA	V_n	–	100	–	μV_{rms}
ENABLE						
Enable Input Threshold Voltage Logic Low (OFF) Logic High (ON)	 V_{out} ≤ 0.1 V V_{out} ≥ 0.9 x V_{out_nom}	$V_{th(EN)}$	 0.99 –	 1.85 1.9	 – 2.31	V
Enable Input Current	V_{EN} = 3.3 V	I_{EN}	2.0	9.0	20	μA
Turn On Time from Enable ON to 90% of V_{out_nom}	I_{out} = 100 mA, C_b = 10 nF, R_1 = 82 kΩ, R_2 = 27 kΩ	t_{on}	–	1.6	–	ms
OUTPUT CURRENT SENSE						
CSO Voltage Level at Current Limit	V_{out} = 0.9 x V_{out_nom}, (V_{out_nom} = 5 V) R_{CSO} = 1 kΩ	V_{CSO_Ilim}	2.346 (−8 %)	2.55	2.754 (+8 %)	V
CSO Transient Voltage Level	C_{CSO} = 4.7 μF, R_{CSO} = 1 kΩ, I_{out} pulse from 10 mA to 350 mA, t_r = 1 μs	V_{CSO}	–	–	3.0	V
CSO Current to Output Current Ratio (Note 8)	V_{CSO} = 2 V, I_{out} = 10 mA to 350 mA, (V_{out_nom} = 5V)	I_{CSO}/I_{out}	– (−10%)	(1/100)	– (+10%)	–
CSO Current at No Load Current	V_{CSO} = 0 V, I_{out} = 0 mA, (V_{out_nom} = 5 V)	I_{CSO_off}	–	–	10	μA
REVERSE CURRENT						
Reverse Current (Note 9)	V_{in} = 12 V, V_{out} = 14 V	I_{out_rev}	−40	−25	–	mA
THERMAL SHUTDOWN						
Thermal Shutdown Temperature	I_{out} = 5 mA	T_{SD}	150	–	195	°C

7. Measured when the output voltage V_{out} has dropped −2% from the nominal value obtained at V_{in} = V_{out_nom} + 8.5 V.
8. Not guaranteed in dropout.
9. Values based on design and/or characterization.

TYPICAL CHARACTERISTICS

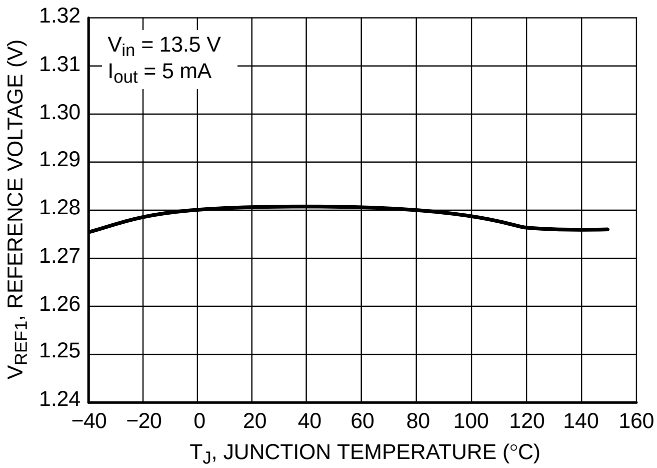


Figure 3. Reference Voltage vs. Temperature

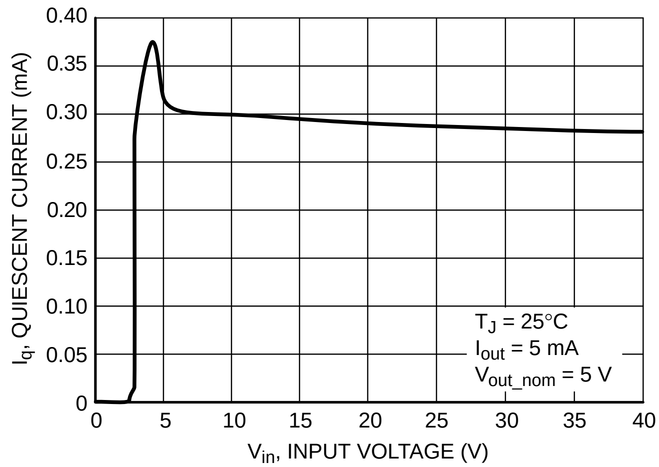


Figure 4. Quiescent Current vs. Input Voltage

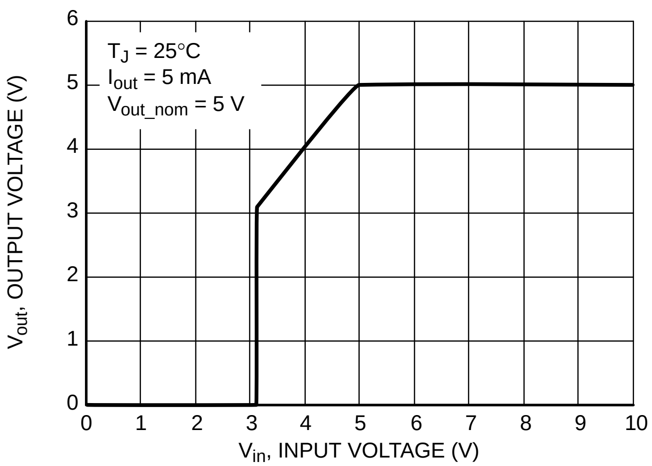


Figure 5. Output Voltage vs. Input Voltage

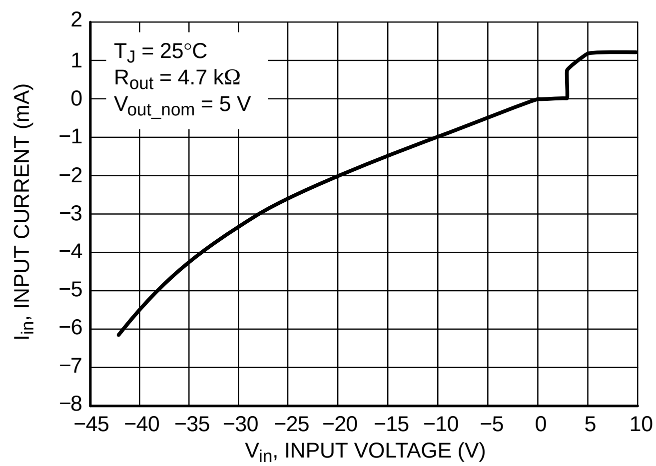


Figure 6. Input Current vs. Input Voltage (Reverse Input Voltage)

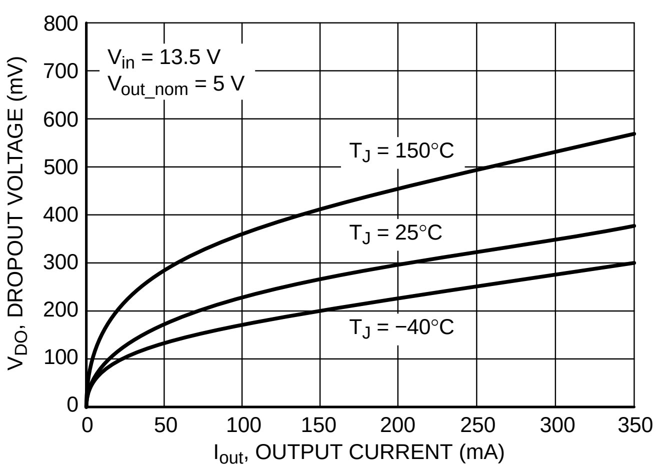


Figure 7. Dropout vs. Output Current

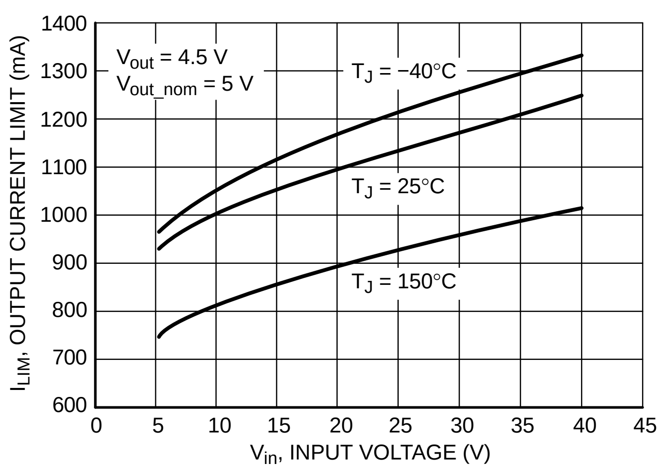


Figure 8. Output Current Limit vs. Input Voltage

TYPICAL CHARACTERISTICS

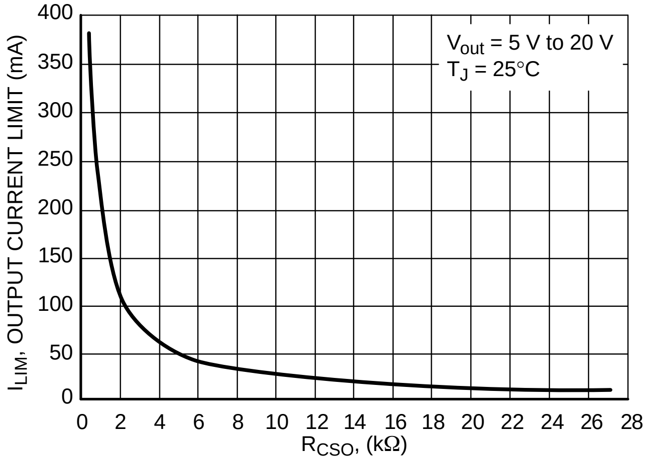


Figure 9. Output Current Limit vs. R_{CSO}

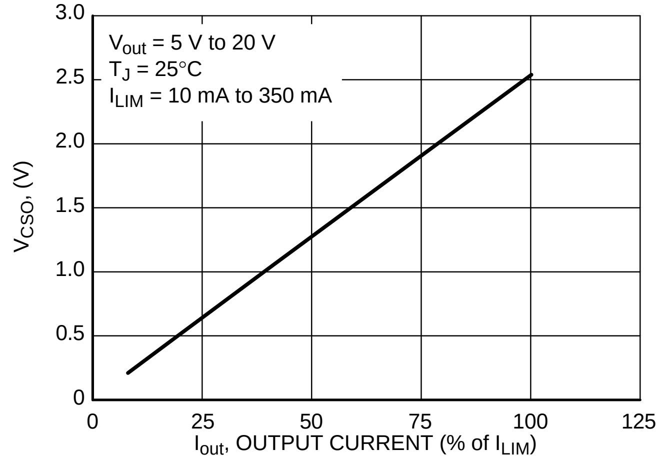


Figure 10. Output Current (% of I_{LIM}) vs. CSO Voltage

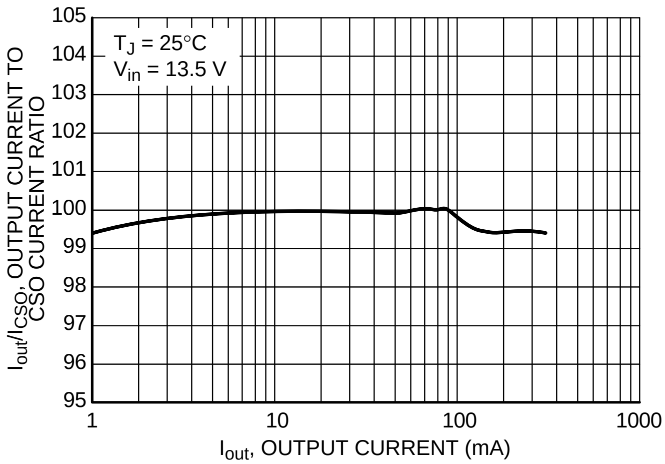


Figure 11. Output Current to CSO Current Ratio vs. Output Current

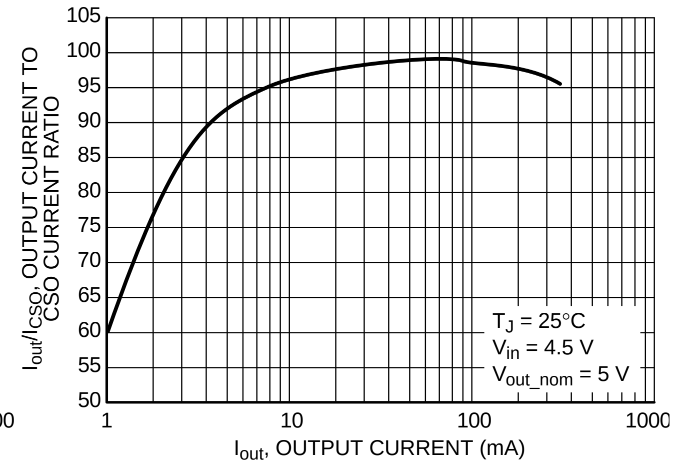


Figure 12. Output Current to CSO Current Ratio vs. Output Current in Dropout

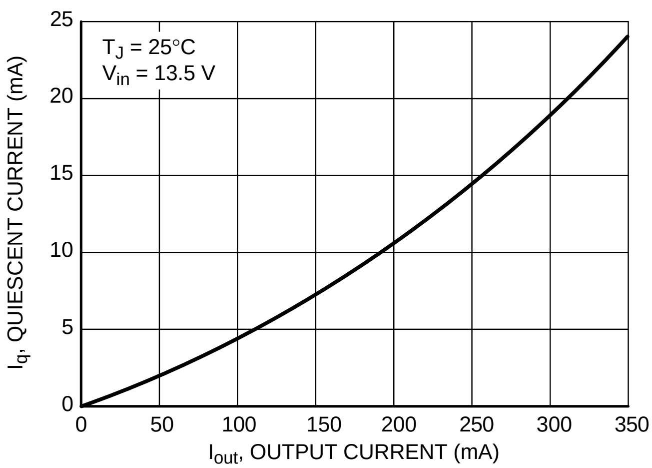


Figure 13. Quiescent Current vs. Output Current (High Load)

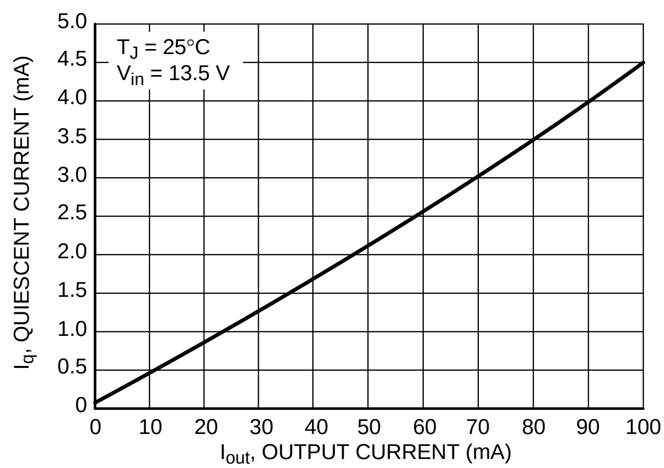


Figure 14. Quiescent Current vs. Output Current (Low Load)

TYPICAL CHARACTERISTICS

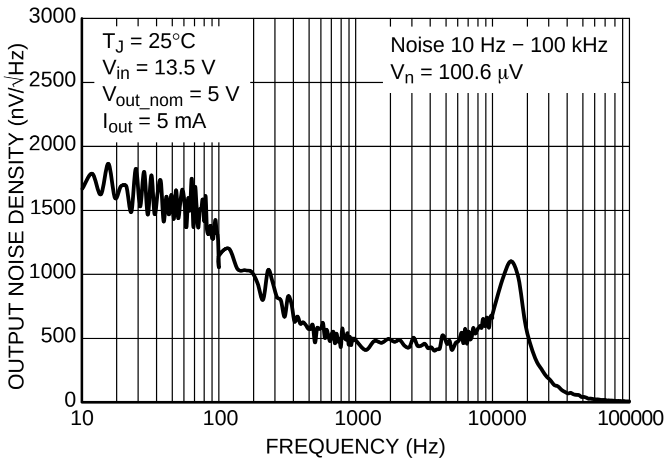


Figure 15. Output Noise Density vs. Frequency

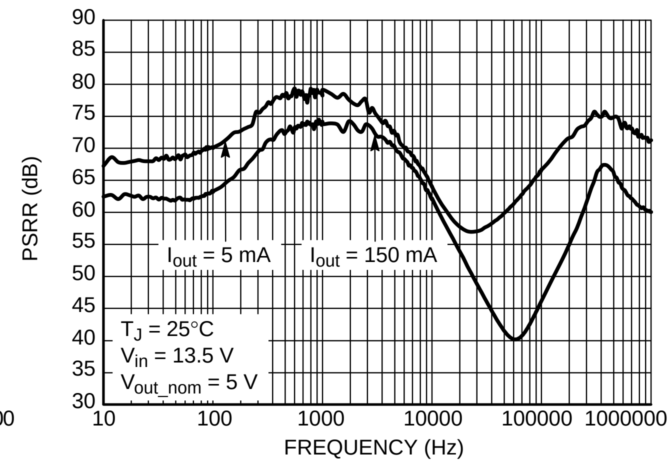


Figure 16. PSRR vs. Frequency

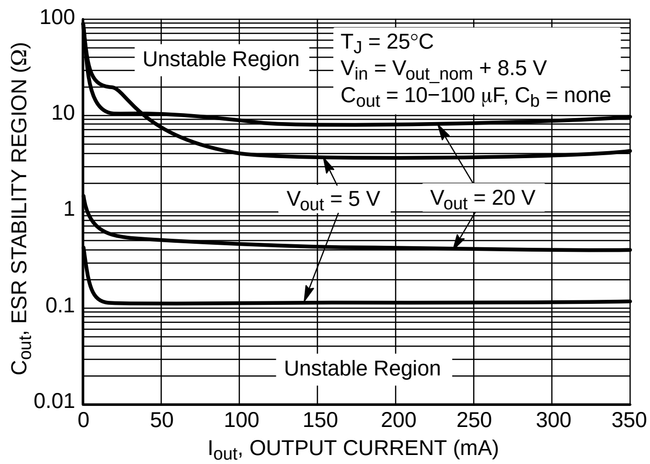


Figure 17. C_{out} ESR Stability Region vs. Output Current

DEFINITIONS

General

All measurements are performed using short pulse low duty cycle techniques to maintain junction temperature as close as possible to ambient temperature.

Output Voltage

The output voltage parameter is defined for specific temperature, input voltage and output current values or specified over Line, Load and Temperature ranges.

Line Regulation

The change in output voltage for a change in input voltage measured for specific output current over operating ambient temperature range.

Load Regulation

The change in output voltage for a change in output current measured for specific input voltage over operating ambient temperature range.

Dropout Voltage

The input to output differential at which the regulator output no longer maintains regulation against further reductions in input voltage. It is measured when the output voltage V_{out} has dropped −2% from the nominal value obtained at $V_{in} = V_{out\_nom} + 8.5$ V. The junction temperature, load current, and minimum input supply requirements affect the dropout level.

Quiescent and Disable Currents

Quiescent Current (I_q) is the difference between the input current (measured through the LDO input pin) and the output load current. If Enable pin is set to LOW the regulator reduces its internal bias and shuts off the output, this term is called the disable current (I_{DIS}).

Current Limit

Current Limit is value of output current by which output voltage drops below 90% of its nominal value.

PSRR

Power Supply Rejection Ratio is defined as ratio of output voltage and input voltage ripple. It is measured in decibels (dB).

Line Transient Response

Typical output voltage overshoot and undershoot response when the input voltage is excited with a given slope.

Load Transient Response

Typical output voltage overshoot and undershoot response when the output current is excited with a given slope between low−load and high−load conditions.

Thermal Protection

Internal thermal shutdown circuitry is provided to protect the integrated circuit in the event that the maximum junction temperature is exceeded. When activated at typically 175°C, the regulator turns off. This feature is provided to prevent failures from accidental overheating.

Maximum Package Power Dissipation

The power dissipation level is maximum allowed power dissipation for particular package or power dissipation at which the junction temperature reaches its maximum operating value, whichever is lower.

APPLICATIONS INFORMATION

Circuit Description

The NCV47711 is an integrated low dropout regulator that provides a regulated voltage at 350 mA to the output. It is enabled with an input to the enable pin. The regulator voltage is provided by a PNP pass transistor controlled by an error amplifier with a bandgap reference, which gives it the lowest possible dropout voltage. The output current capability is 350 mA, and the base drive quiescent current is controlled to prevent oversaturation when the input voltage is low or when the output is overloaded. The integrated current sense feature provides diagnosis and system protection functionality. The current limit of the device is adjustable by resistor connected to CSO pin. Voltage on CSO pin is proportional to output current. The regulator is protected by both current limit and thermal shutdown. Thermal shutdown occurs above 150°C to protect the IC during overloads and extreme ambient temperatures.

Regulator

The error amplifier compares the reference voltage to a sample of the output voltage (V_{out}) and drives the base of a PNP series pass transistor via a buffer. The reference is a bandgap design to give it a temperature−stable output. Saturation control of the PNP is a function of the load current and input voltage. Oversaturation of the output power device is prevented, and quiescent current in the ground pin is minimized.

Regulator Stability Considerations

The input capacitor (C_{in}) is necessary to stabilize the input impedance to avoid voltage line influences. The output capacitor (C_{out}) helps determine three main characteristics of a linear regulator: startup delay, load transient response and loop stability. The capacitor value and type should be based on cost, availability, size and temperature constraints. The aluminum electrolytic capacitor is the least expensive solution, but, if the circuit operates at low temperatures (−25°C to −40°C), both the value and ESR of the capacitor will vary considerably. The capacitor manufacturer's data sheet usually provides this information. The value for the output capacitor C_{out}, shown in Figure 1 should work for most applications; see also Figure 17 for output stability at various load and Output Capacitor ESR conditions. Stable region of ESR in Figure 17 shows ESR values at which the LDO output voltage does not have any permanent oscillations at any dynamic changes of output load current. Marginal ESR is the value at which the output voltage waving is fully damped during four periods after the load change and no oscillation is further observable.

ESR characteristics were measured with ceramic capacitors and additional series resistors to emulate ESR. Low duty cycle pulse load current technique has been used to maintain junction temperature close to ambient temperature.

Calculating Bypass Capacitor

If usage of low ESR ceramic capacitors is demanded, connect the bypass capacitor C_b between Adjustable Input pin and V_{out} pin according to Applications circuit at Figure 1. Parallel combination of bypass capacitor C_b with the feedback resistor R_1 contributes in the device transfer function as an additional zero and affects the device loop stability, therefore its value must be optimized. Attention to the Output Capacitor value and its ESR must be paid. See also Stability in High Speed Linear LDO Regulators Application Note, AND8037/D for more information. Optimal value of bypass capacitor is given by following expression:

$$C_b = \frac{1}{2 \times \pi \times f_z \times R_1} \qquad \text{(eq. 1)}$$

where

R_1 − the upper feedback resistor

f_z − the frequency of the zero added into the device transfer function by R_1 and C_b external components.

Set the R_1 resistor according to output voltage requirement. Chose the f_z with regard on the output capacitance C_{out}, refer to the table below.

C_{out} (μF)	10	22	47	100
f_Z range (kHz)	3.3−48.2	1.5−33	1.5−33	2.2−22

Ceramic capacitors and its part numbers listed bellow have been used as low ESR output capacitors C_{out} from the table above to define the frequency ranges of additional zero required for stability:

GRM31CR71C106KAC7 (10 μF, 16 V, X7R, 1206)
GRM32ER71C226KE18 (22 μF, 16 V, X7R, 1210)
GRM32ER61C476ME15 (47 μF, 16 V, X5R, 1210)
GRM32ER60J107ME20 (100 μF, 6.3 V, X5R, 1210)

Enable Input

The enable pin is used to turn the regulator on or off. By holding the pin down to a voltage less than 0.99 V, the output of the regulator will be turned off. When the voltage on the enable pin is greater than 2.31 V, the output of the regulator will be enabled to power its output to the regulated output voltage.

Setting the Output Voltage

The output voltage range can be set between 5 V and 20 V. This is accomplished with an external resistor divider feeding back the voltage to the IC back to the error amplifier by the voltage adjust pin ADJ. The internal reference voltage is set to a temperature stable reference (V_{REF1}) of 1.275 V. The output voltage is calculated from the following formula. Ignoring the bias current into the ADJ pin:

$$V_{out} = V_{REF1}\left(1 + \frac{R_1}{R_2}\right) \quad \text{(eq. 2)}$$

Use $R_2 < 50\ k\Omega$ to avoid significant voltage output errors due to ADJ bias current.

Designers should consider the tolerance of R_1 and R_2 during the design phase.

Setting the Output Current Limit

The output current limit can be set between 10 mA and 350 mA by external resistor R_{CSO} (see Figure 1). Capacitor C_{CSO} of 1 μF in parallel with R_{CSO} is required for stability of current limit control circuitry (see Figure 1).

$$V_{CSO} = I_{out}\left(R_{CSO} \times \frac{1}{100}\right) \quad \text{(eq. 3)}$$

$$I_{LIM} = \frac{100}{1} \times \frac{2.55}{R_{CSO}} \quad \text{(eq. 4)}$$

$$R_{CSO} = \frac{100}{1} \times \frac{2.55}{I_{LIM}} \quad \text{(eq. 5)}$$

Where

R_{CSO} − current limit setting resistor
V_{CSO} − voltage at CSO pin proportional to I_{out}
I_{LIM} − current limit value
I_{out} − output current actual value

CSO pin provides information about output current actual value. The CSO voltage is proportional to output current according to Equation 3.

Once output current reaches its limit value (I_{LIM}) set by external resistor R_{CSO} than voltage at CSO pin is typically 2.55 V. Calculations of I_{LIM} or R_{CSO} values can be done using equations Equation 4 and Equation 5, respectively.

Thermal Considerations

As power in the NCV47711 increases, it might become necessary to provide some thermal relief. The maximum power dissipation supported by the device is dependent upon board design and layout. Mounting pad configuration on the PCB, the board material, and the ambient temperature affect the rate of junction temperature rise for the part. When the NCV47711 has good thermal conductivity through the PCB, the junction temperature will be relatively low with high power applications. The maximum dissipation the NCV47711 can handle is given by:

$$P_{D(MAX)} = \frac{\left[T_{J(MAX)} - T_A\right]}{R_{\theta JA}} \quad \text{(eq. 6)}$$

Since T_J is not recommended to exceed 150°C, then the NCV47711 soldered on 645 mm^2, 1 oz copper area, FR4 can dissipate up to 1.8 W (SOIC−8 EP) or 1 W (SOIC−8) and up to 4.3 W (SOIC−8 EP) or 1.6 W (SOIC−8) for 4 layers PCB (all layers are 1 oz) when the ambient temperature (T_A) is 25°C. See Figure 18 for R_{thJA} versus PCB area. The power dissipated by the NCV47711 can be calculated from the following equations:

$$P_D = V_{in}\left(I_q@I_{out}\right) + I_{out}\left(V_{in} - V_{out}\right) \quad \text{(eq. 7)}$$

or

$$V_{in(MAX)} \approx \frac{P_{D(MAX)} + \left(V_{out} \times I_{out}\right)}{I_{out} + I_q} \quad \text{(eq. 8)}$$

Hints

V_{in} and GND printed circuit board traces should be as wide as possible. When the impedance of these traces is high, there is a chance to pick up noise or cause the regulator to malfunction. Place external components, especially the output capacitor, as close as possible to the NCV47711 and make traces as short as possible.

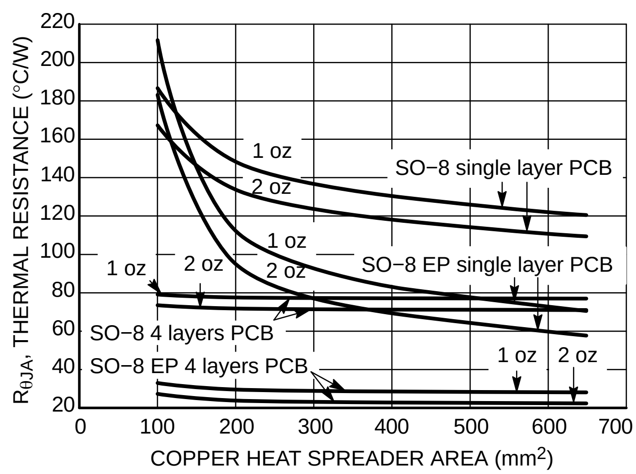


Figure 18. Thermal Resistance vs. PCB Copper Area

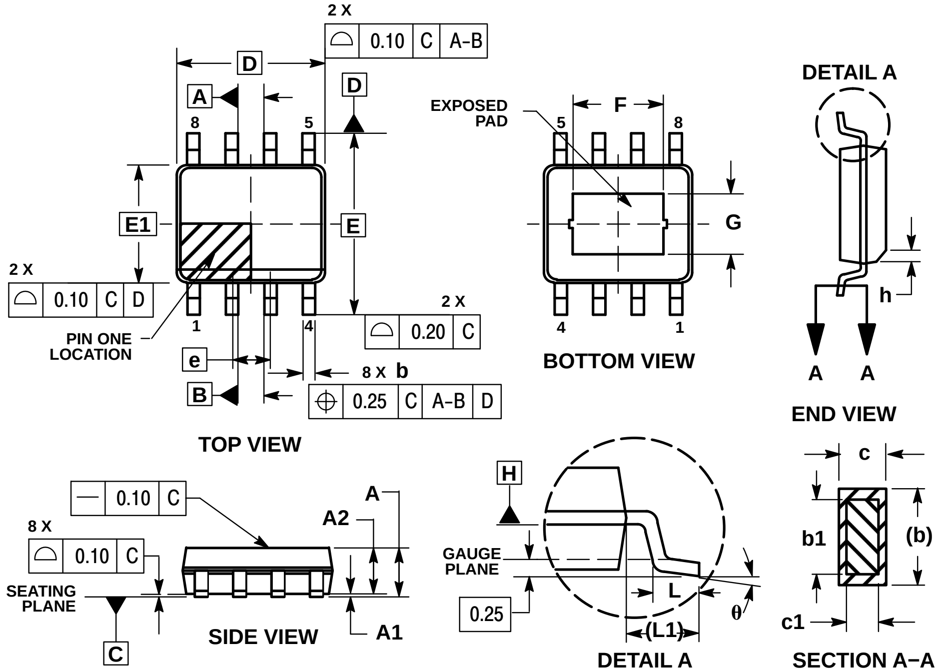
ORDERING INFORMATION

Device	Output Voltage	Marking	Package	Shipping†
NCV47711PDAJR2G	Adjustable	47711	SOIC−8 EP (Pb−Free)	2500 / Tape & Reel
NCV47711DAJR2G	Adjustable	47711	SOIC−8 (Pb−Free)	2500 / Tape & Reel

†For information on tape and reel specifications,including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

PACKAGE DIMENSIONS

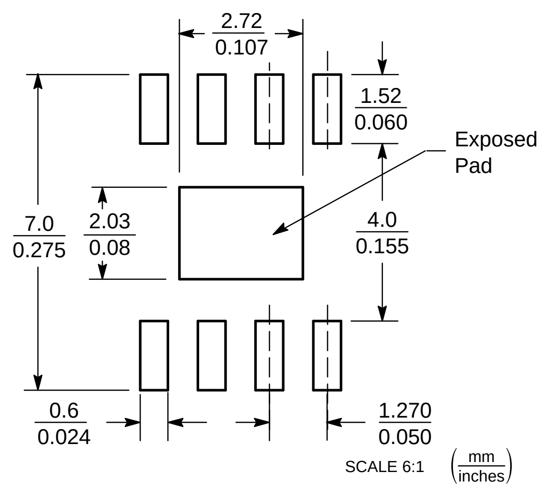
SOIC−8 EP
CASE 751AC
ISSUE B



NOTES:
1. DIMENSIONS AND TOLERANCING PER ASME Y14.5M, 1994.
2. DIMENSIONS IN MILLIMETERS (ANGLES IN DEGREES).
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 MM TOTAL IN EXCESS OF THE “b” DIMENSION AT MAXIMUM MATERIAL CONDITION.
4. DATUMS A AND B TO BE DETERMINED AT DATUM PLANE H.

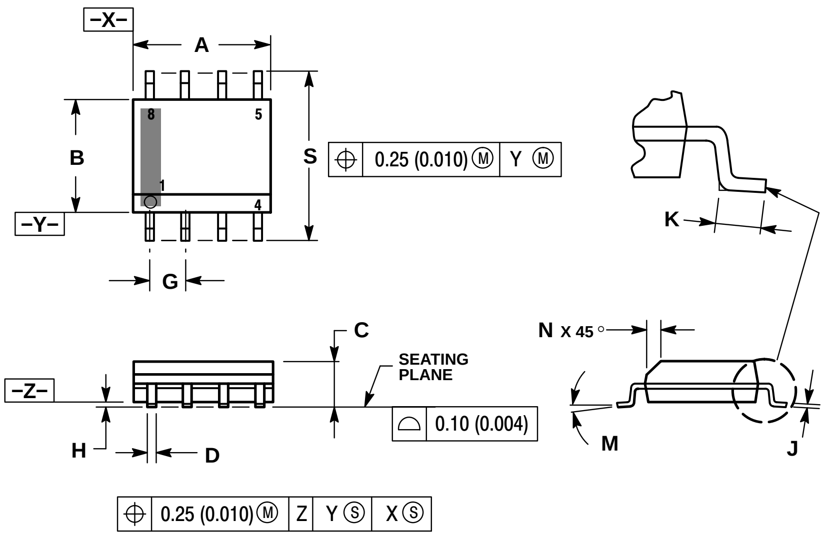
	MILLIMETERS	
DIM	MIN	MAX
A	1.35	1.75
A1	0.00	0.10
A2	1.35	1.65
b	0.31	0.51
b1	0.28	0.48
c	0.17	0.25
c1	0.17	0.23
D	4.90 BSC	
E	6.00 BSC	
E1	3.90 BSC	
e	1.27 BSC	
L	0.40	1.27
L1	1.04 REF	
F	2.24	3.20
G	1.55	2.51
h	0.25	0.50
θ	0 °	8 °

SOLDERING FOOTPRINT



PACKAGE DIMENSIONS

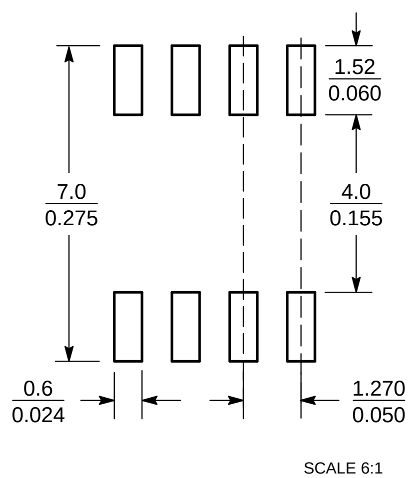
SOIC−8
CASE 751−07
ISSUE AK



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. 751−01 THRU 751−06 ARE OBSOLETE. NEW STANDARD IS 751−07.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.197
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.053	0.069
D	0.33	0.51	0.013	0.020
G	1.27 BSC		0.050 BSC	
H	0.10	0.25	0.004	0.010
J	0.19	0.25	0.007	0.010
K	0.40	1.27	0.016	0.050
M	0 °	8 °	0 °	8 °
N	0.25	0.50	0.010	0.020
S	5.80	6.20	0.228	0.244

SOLDERING FOOTPRINT*



*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

PUBLICATION ORDERING INFORMATION

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