具有高精度可调电流限值和过压钳位的 TPS25200 5V 电子保险丝

1 特性

- 2.5V 至 6.5V 工作电压
- 输入可耐受电压高达 20V
- 7.6V 输入过压关断
- 5.25V 至 5.55V 固定过压钳位
- 0.6µs 过压锁定响应
- 3.5µs 短路响应
- 集成型 60mΩ 高侧金属氧化物半导体场效应晶体管 (MOSFET)
- 高达 2.5A 持续负载电流
- 2.9A 电流下 ±6% 电流限制精度
- 禁用时，反向电流阻断
- 内置软启动
- 与 TPS2553 引脚到引脚兼容
- 经 UL 2367 认证
  - 文件编号169910
  - R_{ILIM} ≥ 33kΩ（最大电流为 3.12A）

2 应用范围

- USB 电源开关
- USB 受控器件
- 手机/智能电话
- 3G，4G 无线数据卡
- 固态硬盘 (SSD)
- 3V 或 5V 适配器供电器件

3 说明

TPS25200 是一款具有高精度电流限值和过压钳位的 5V 电子保险丝。此器件可在过压和过流事件发生期间为负载和电源提供可靠保护。

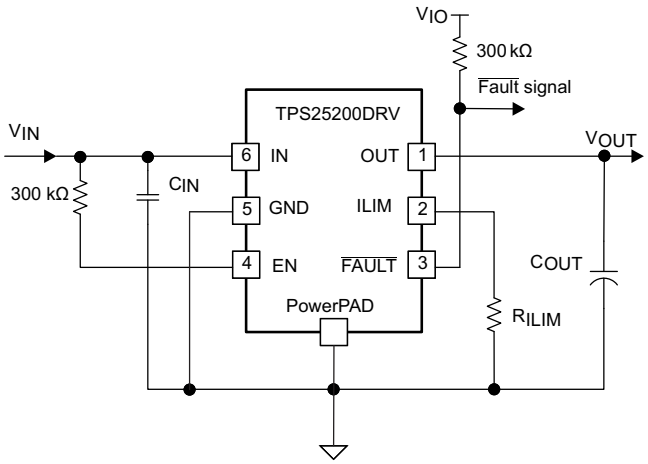
TPS25200 是一款用于保护负载的智能开关，可耐受 20V 的输入电压。如果在输入端施加了错误电压，输出端可将电压限制在 5.4V，以保护负载。如果输入端的电压超过 7.6V，此器件将断开负载，以防止对器件和/或负载造成损坏。

TPS25200 具有 60mΩ 的内部电源开关，可用于在多种异常情况下保护电源、器件和负载。此器件提供高达 2.5A 的持续负载电流。通过一个连接到地的电阻，可对限流值在85mA到2.9A范围内进行设置。当发生过载时，输出电流被限制在由 R_{ILIM} 设定的电流值上如果出现持续过载，TPS25200 将最终进入热关断模式，从而避免自身发生损坏。

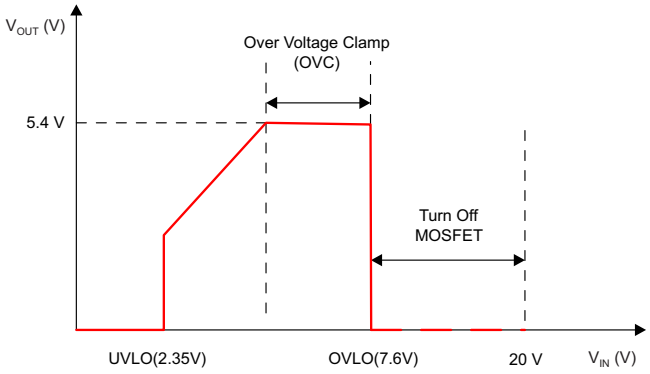
器件信息

订货编号	封装	封装尺寸
TPS25200	SON (6)	2.00mm x 2.00mm

简化电路原理图



V_{OUT} 与 V_{IN} 之间的关系



目录

4 修订历史记录

Changes from Revision A (March 2014) to Revision B **Page**

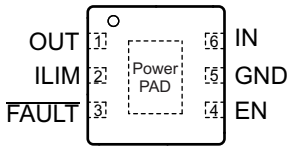
- 已添加 将 UL 认证状态添加到*特性*部分 ... 1

Changes from Original (March 2014) to Revision A **Page**

- Changed the t_{off} TYP value From: 0.24 ms To: 0.22 ms ... 6
- Added condition: V_{EN} = V_{IN} = 0 V to Figure 3 ... 7
- Changed Figure 8 graph title From: Discharge Resistance To: V_{IN} ... 7
- Changed Equation 4 From = 2470 mA to = 2479 mA ... 15

5 Pin Configuration and Functions

DRV Package
6-Pin SOT
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
EN	4	I	Logic-level control input. When is driven high, the power switch is enabled. When it is driven low, turn power switch off. This pin cannot be left floating and it must be limited below the absolute maximum rating if tied to V_{IN}
$\overline{\text{FAULT}}$	3	O	Active-low open-drain output, asserted during overcurrent, overvoltage or overtemperature. Connect a pull up resistor to the logic I/O voltage
GND	5	—	Ground connection; connect externally to PowerPAD
ILIM	2	O	External resistor used to set current-limit threshold; Recommended 33 kΩ ≤ R_{ILIM} ≤ 1100 kΩ
IN	6	I	Input voltage; connect a 0.1-μF or greater ceramic capacitor from IN to GND as close to the IC as possible
OUT	1	O	Protected power switch V_{OUT}
PowerPAD™	PAD	—	Internally connected to GND; used to heat-sink the part to the circuit board traces. Connect PowerPAD to GND terminal externally

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range, voltage are referenced to GND (unless otherwise noted) (1)

		MIN	MAX	UNIT
	Voltage on IN	–0.3	20	V
	Voltage on OUT, EN, ILIM, $\overline{\text{FAULT}}$	–0.3	7	V
	Voltage from IN to OUT	–7	20	V
I_O	Continuous output current	Thermally Limited		
	Continuous $\overline{\text{FAULT}}$ output sink current		25	mA
	Continuous ILIM output source current		150	µA
T_J	Operating junction temperature	Internally limited		
T_{stg}	Storage temperature	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolutemaximum- rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101 (2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range, voltage are referenced to GND (unless otherwise noted)

		MIN	MAX	UNIT
V_{IN}	Input voltage of IN	2.5	6.5	V
V_{EN}	Enable terminal voltage	0	6.5	V
$I_{\overline{\text{FAULT}}}$	Continuous $\overline{\text{FAULT}}$ sink current	0	10	mA
I_{OUT}	Continuous output current of OUT		2.5	A
R_{ILIM}	Current-limit set resistors	33	1100	kΩ
T_J	Operating junction temperature	–40	125	°C

6.4 Thermal Information

THERMAL METRIC (1)		TPS25200 DRV (SOT) 6 PINS	UNIT
θ_{JA}	Junction-to-ambient thermal resistance	66.5	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance	83.4	°C/W
θ_{JB}	Junction-to-board thermal resistance	36.1	°C/W
ψ_{JT}	Junction-to-top characterization parameter	1.6	°C/W
ψ_{JB}	Junction-to-board characterization parameter	36.5	°C/W
θ_{JCbot}	Junction-to-case (bottom) thermal resistance	7.6	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Electrical Characteristics

Conditions are –40°C ≤ T_J ≤ +125°C and 2.5 V ≤ V_{IN} ≤ 6.5 V. V_{EN} = V_{IN}, R_{ILIM} = 33 kΩ. Positive current into terminals. Typical value is at 25°C. All voltages are with respect to GND (unless otherwise noted).

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
POWER SWITCH							
$r_{DS(on)}$	IN–OUT resistance (1)	2.5 V ≤ V_{IN} ≤ 5 V, I_{OUT} = 2.5 A	T_J = 25°C		60	70	mΩ
			–40°C ≤ T_J ≤ +85°C		60	90	
			–40°C ≤ T_J ≤ +125°C		60	99	
ENABLE INPUT EN							
	EN terminal turnon threshold	Input rising				1.9	V
	EN terminal turnoff threshold	Input falling		0.6			V
	Hyesteresis				330 (2)		mV
I_{EN}	Leakage current	V_{EN} = 0 V or 5.5 V		–2		2	µA
DISCHARGE							
R_{DCHG}	OUT discharge resistance	V_{OUT} = 5 V, V_{EN} = 0 V			480	625	Ω
CURRENT LIMIT							
I_{OS}	Current - limit, See Figure 12	R_{ILIM} = 33 kΩ		2773	2952	3127	mA
		R_{ILIM} = 40.2 kΩ		2270	2423	2570	
		R_{ILIM} = 56 kΩ		1620	1740	1860	
		R_{ILIM} = 80.6 kΩ		1110	1206	1300	
		R_{ILIM} = 150 kΩ		590	647	710	
		R_{ILIM} = 1100 kΩ		40	83	130	
OVERVOLTAGE LOCKOUT, IN							
$V_{(OVLO)}$	IN rising OVLO threshold voltage	IN rising		6.8	7.6	8.45	V
	Hysteresis				70 (2)		mV
VOLTAGE CLAMP, OUT							
$V_{(OVC)}$	OUT clamp voltage threshold	C_L = 1 µF, R_L = 100 Ω, V_{IN} = 6.5 V		5.25	5.4	5.55	V
SUPPLY CURRENT							
$I_{IN(off)}$	Supply current, low-level output	V_{EN} = 0 V, V_{IN} = 5 V			0.8	5	µA
		V_{EN} = 0 or 5 V, V_{IN} = 20 V			1000	1700	
$I_{IN(on)}$	Supply current, high-level output	V_{IN} = 5 V, No load on OUT	R_{ILIM} = 33 kΩ		143	200	µA
			R_{ILIM} = 150 kΩ		134	190	
I_{REV}	Reverse leakage current	V_{OUT} = 6.5V, V_{IN} = V_{EN} = 0 V, T_J = 25°C, measure I_{OUT}			3	5	µA
UNDERVOLTAGE LOCKOUT, IN							
V_{UVLO}	IN rising UVLO threshold voltage	IN rising			2.35	2.45	V
	Hysteresis				30 (2)		mV
$\overline{\text{FAULT}}$ FLAG							
V_{OL}	Output low voltage, $\overline{\text{FAULT}}$	$I_{\overline{FAULT}}$ = 1 mA			50	180	mV
	Off-state leakage	$V_{\overline{FAULT}}$ = 6.5 V				1	µA
THERMAL SHUTDOWN							
	Thermal shutdown threshold, OTSD2			155			°C
	Thermal shutdown threshold only in current-limit, OTSD1			135			
	Hysteresis				20 (2)		

(1) Pulse-testing techniques maintain junction temperature close to ambient temperature. Thermal effects must be taken into account separately.
(2) These parameters are provided for reference only and does not constitute part of TI's published device specifications for purposes of TI's product warranty.

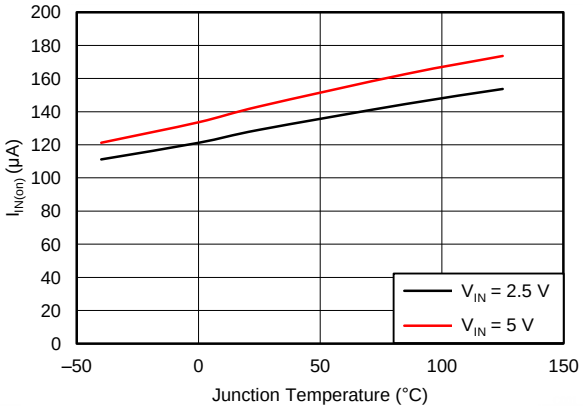
6.6 Timing Requirements

Conditions are –40°C ≤ T_J ≤ +125°C and 2.5 V ≤ V_{IN} ≤ 6.5 V. V_{EN} = V_{IN}, R_{ILIM} = 33 kΩ. Positive current are into terminals. Typical value is at 25°C. All voltages are with respect to GND (unless otherwise noted)

		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER SWITCH						
t_r	OUT voltage rise time	C_L = 1 µF, R_L = 100 Ω, (see Figure 10)		2.05	3.2	ms
t_f	OUT voltage fall time			0.18	0.2	ms
ENABLE INPUT EN						
t_{on}	Turnon time	2.5 V ≤ V_{IN} ≤ 5 V, C_L = 1 µF, R_L = 100 Ω, (see Figure 10)		5.12	7.3	ms
t_{off}	Turnoff time			0.22	0.3	ms
CURRENT LIMIT						
$t_{(IOS)}$	Short-circuit response time	V_{IN} = 5 V (see Figure 12)		3.5 (1)		µs
OVERVOLTAGE LOCKOUT, IN						
$t_{(OVLO\_off\_delay)}$	Turnoff delay for OVLO	V_{IN} 5 V to 10 V with 1-V/µs ramp up rate, V_{OUT} with 100-Ω load		0.6 (1)		µs
$\overline{\text{FAULT}}$ FLAG						
	$\overline{\text{FAULT}}$ deglitch	$\overline{\text{FAULT}}$ assertion or de-assertion due to overcurrent condition	5	8	12	ms

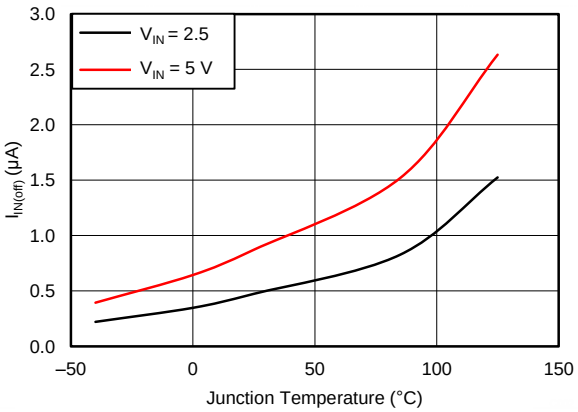
(1) This parameter is provided for reference only and does not constitute part of TI's published device specifications for purposes of TI's product warranty.

6.7 Typical Characteristics



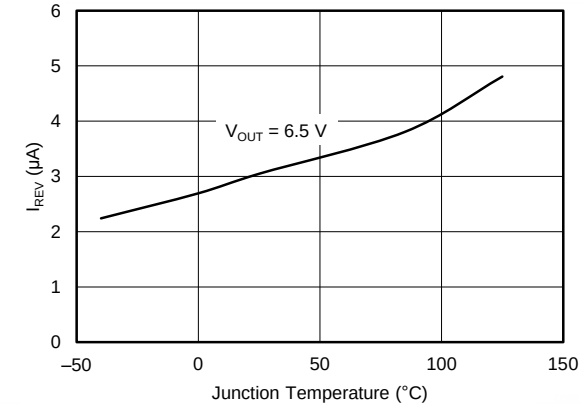
R_{ILIM} = 33 KΩ

Figure 1. $I_{IN(on)}$ vs Junction Temperature



R_{ILIM} = 33 KΩ

Figure 2. $I_{IN(off)}$ vs Junction Temperature



V_{EN} = V_{IN} = 0 V

Figure 3. I_{REV} vs Junction Temperature

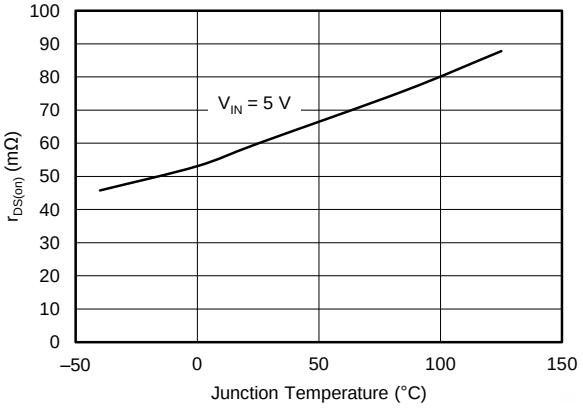
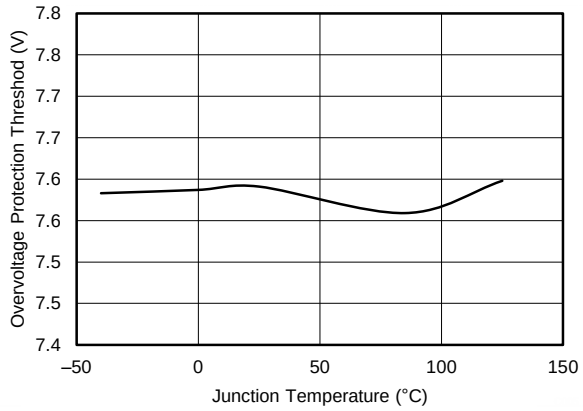
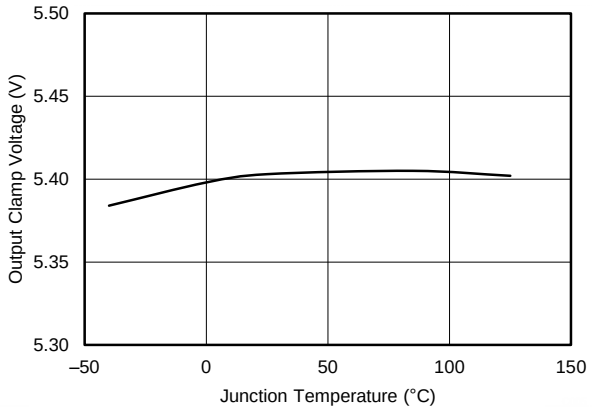


Figure 4. $r_{DS(ON)}$ vs Junction Temperature



V_{EN} = V_{IN} = 0 V

Figure 5. $V_{(OVLO)}$ vs Junction Temperature



C_L = 1 µF R_L = 100 Ω V_{IN} = 6.5 V

Figure 6. $V_{O(VC)}$ vs Junction Temperature

Typical Characteristics (continued)

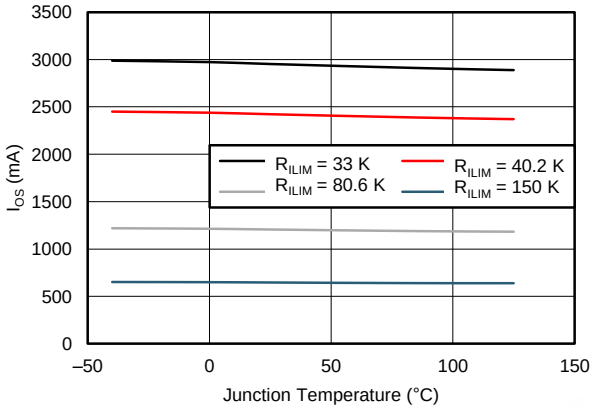


Figure 7. I_{OS} vs Junction Temperature

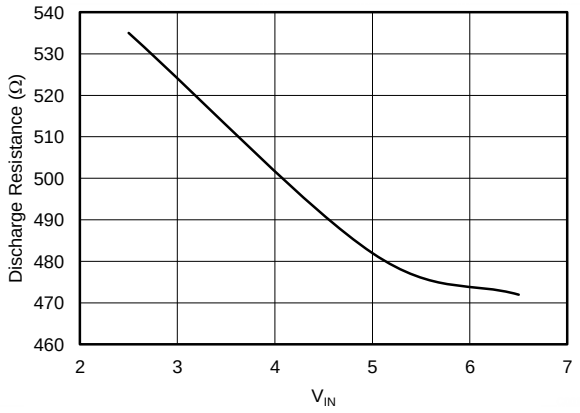


Figure 8. Discharge Resistance vs V_{IN}

7 Parameter Measurement Information

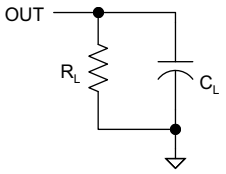


Figure 9. Output Rise-Fall Test Load

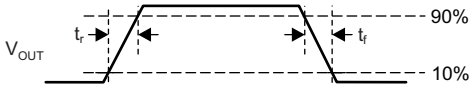


Figure 10. Power-On and Off Timing

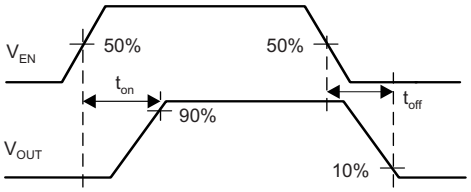


Figure 11. Enable Timing, Active High Enable

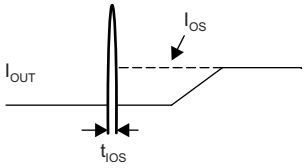


Figure 12. Output Short Circuit Parameters

8 Detailed Description

8.1 Overview

The TPS25200 is an intelligent low voltage switch or e-Fuse with robust overcurrent and overvoltage protection which are suitable for a variety of applications.

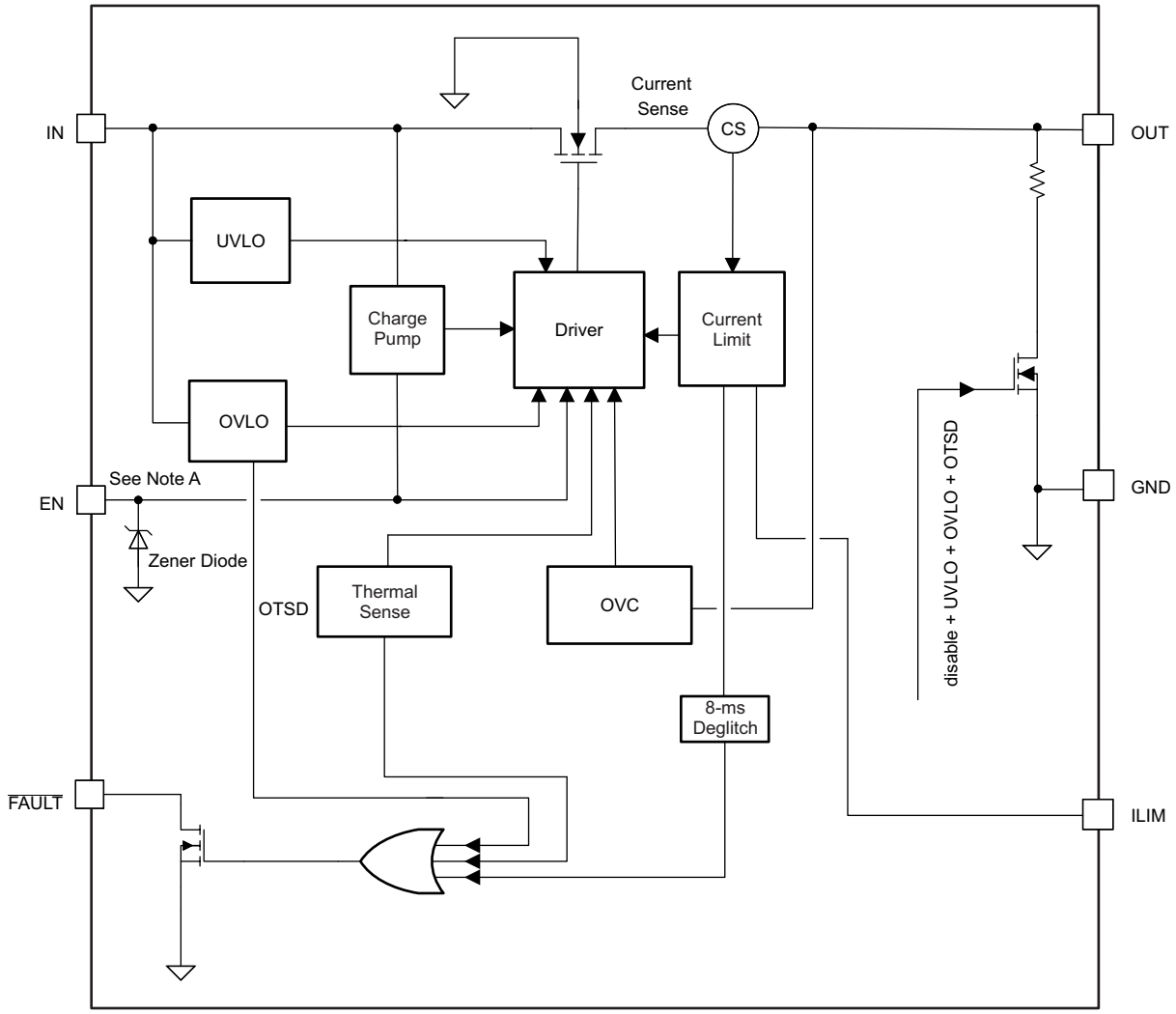
The TPS25200 current limited power switch uses N-channel MOSFETs in applications requiring up to 2.5 A of continuous load current. The device allows the user to program the current-limit threshold between 85 mA and 2.9 A (typical) via an external resistor. The device enters constant-current mode when the load exceeds the current-limit threshold.

The TPS25200 Input can withstand 20-V DC voltage, but clamps V_{OUT} to a precision regulated 5.4 V and shuts down in the event V_{IN} exceeds 7.6 V. The device also integrates overcurrent and short circuit protection. The precision overcurrent limit helps to minimize over design of the input power supply while the fast response short circuit protection isolates the load when a short circuit is detected.

The additional features include:

- Enable the device can be put into a sleep mode for portable applications.
- Overtemperature protection to safely shutdown in the event of an overcurrent event or a slight overvoltage event where the V_{OUT} clamp is engaged over and extended period of time.
- Deglitched fault reporting to filter the Fault signal to ensure the TPS25200 do not provide false fault alerts.
- Output discharge pull-down to help ensue a load is in fact off and not in some undefined operational state.
- Reverse blocking when disabled to prevent back-drive from an active load inadvertently causing undetermined behavior in the application.

8.2 Functional Block Diagram



A. 6.4-V Typical Clamp Voltage

8.3 Feature Description

8.3.1 Enable

This logic enable input controls the power switch and device supply current. A logic high input on EN enables the driver, control circuits, and power switch. The enable input is compatible with both TTL and CMOS logic levels.

EN can be tied to V_{IN} with a pull up resistor, and is protected with an integrated zener diode. Use a sufficiently large (300-kΩ) pull up resistor to ensure that the $V_{(EN)}$ is limited below the absolute maximum rating.

8.3.2 Thermal Sense

The TPS25200 self protects by using two independent thermal sensing circuits that monitor the operating temperature of the power switch and disable operation if the temperature exceeds recommended operating conditions. The TPS25200 device operates in constant-current mode during an overcurrent condition, which increases the voltage drop across power switch. The power dissipation in the package is proportional to the voltage drop across the power switch, which increases the junction temperature during an overcurrent condition. The first thermal sensor (OTSD1) turns off the power switch when the die temperature exceeds 135°C (minimum) and the part is in current limit. Hysteresis is built into the thermal sensor, and the switch turns on after the device has cooled approximately 20°C.

Feature Description (continued)

The TPS25200 also has a second ambient thermal sensor (OTSD2). The ambient thermal sensor turns off the power switch when the die temperature exceeds 155°C (minimum) regardless of whether the power switch is in current limit and turns on the power switch after the device has cooled approximately 20°C. The TPS25200 continues to cycle off and on until the fault is removed.

8.3.3 Overcurrent Protection

The TPS25200 thermally protects itself by thermal cycling during an extended overcurrent condition. The device turns off when the junction temperature exceeds 135°C (typical) while in current limit. The device remains off until the junction temperature cools 20°C (typical) and then restarts. The TPS25200 cycles on/off until the overload is removed (see Figure 26 and Figure 29).

The TPS25200 responds to an overcurrent condition by limiting their output current to the I_{OS} levels shown in Figure 12. When an overcurrent condition is detected, the device maintains a constant output current and the output voltage is reduced accordingly. During an over current event, two possible overload conditions can occur.

The first condition is when a short circuit or partial short circuit is present when the device is powered-up or enabled. The output voltage is held near zero potential with respect to ground and the TPS25200 ramps the output current to I_{OS}. The TPS25200 devices limit the current to I_{OS} until the overload condition is removed or the device begins to thermal cycle.

The second condition is when a short circuit, partial short circuit, or transient overload occurs while the device is enabled and powered on. The device responds to the overcurrent condition within time t_{IOS} (see Figure 12). The current-sense amplifier is overdriven during this time and momentarily disables the internal current-limit MOSFET. The current-sense amplifier recovers and limits the output current to I_{OS}. Similar to the previous case, the TPS25200 limits the current to I_{OS} until the overload condition is removed or the device begins to thermal cycle.

8.3.4 $\overline{\text{FAULT}}$ Response

The $\overline{\text{FAULT}}$ open-drain output is asserted (active low) during an overcurrent, overtemperature or overvoltage condition. The TPS25200 asserts the $\overline{\text{FAULT}}$ signal until the fault condition is removed and the device resumes normal operation. The TPS25200 is designed to eliminate false $\overline{\text{FAULT}}$ reporting by using an internal delay "deglitch" circuit for overcurrent (8-ms typical) conditions without the need for external circuitry. This ensures that $\overline{\text{FAULT}}$ is not accidentally asserted due to normal operation such as starting into a heavy capacitive load. The deglitch circuitry delays entering and leaving current-limit induced fault conditions.

The $\overline{\text{FAULT}}$ signal is not deglitched when the MOSFET is disabled due to an overtemperature condition but is deglitched after the device has cooled and begins to turnon. This unidirectional deglitch prevents $\overline{\text{FAULT}}$ oscillation during an overtemperature event.

The $\overline{\text{FAULT}}$ signal is not deglitched when the MOSFET is disabled into OVLO or out of OVLO. The TPS25200 does not assert the $\overline{\text{FAULT}}$ during output voltage clamp mode.

Connect $\overline{\text{FAULT}}$ with a pull up resistor to a low voltage I/O rail.

8.3.5 Output Discharge

A 480-Ω (typical) output discharge dissipates stored charge and leakage current on OUT when the TPS25200 is in UVLO, disabled or OVLO. The pull down capability decreases as V_{IN} decreases (Figure 8).

8.4 Device Functional Modes

The TPS25200 V_{IN} can withstand up to 20 V. Within 0 V to 20 V range, it can be divided to four modes as shown in Figure 13.

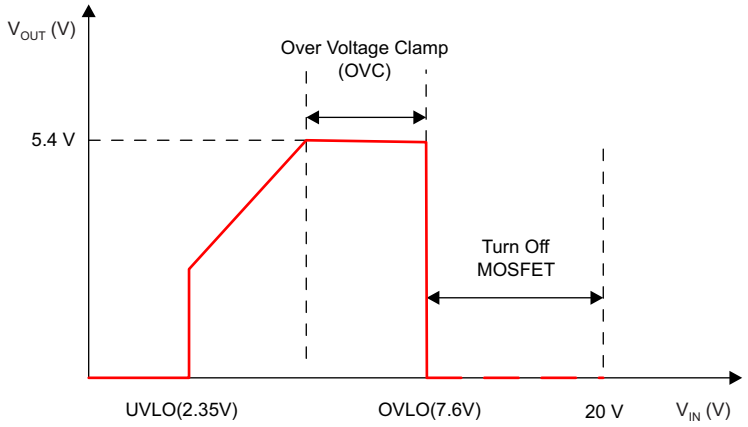


Figure 13. Output vs Input Voltage

8.4.1 Undervoltage Lockout (UVLO)

The undervoltage lockout (UVLO) circuit disables the power switch until the input voltage reaches the UVLO turnon threshold. Built-in hysteresis prevents unwanted on and off cycling due to input voltage droop during turnon.

8.4.2 Overcurrent Protection (OCP)

When 2.35 V < V_{IN} < 5.4 V, the TPS25200 is a traditional power switch, providing overcurrent protection.

8.4.3 Overvoltage Clamp (OVC)

When 5.4 V < V_{IN} < 7.6 V, the overvoltage clamp (OVC) circuit clamps the output voltage to 5.4 V. Within this V_{IN} range, the overcurrent protection remains active.

8.4.4 Overvoltage Lockout (OVLO)

When V_{IN} exceeds 7.6 V, the overvoltage lockout (OVLO) circuit turns off the protected power switch.

9 Application and Implementation

9.1 Application Information

The TPS25200 is a 5-V eFuse with precision current limit and over-voltage clamp. When a slave device such as a mobile data-card device is hot plugged into a USB port as shown in Figure 14, an input transient voltage could damage the slave device due to the cable inductance. Placing the TPS25200 at the input of mobile device as over-voltage and overcurrent protector can safeguard these slave devices. Input transients also occur when the current through the cable parasitic inductance changes abruptly. This can occur when the TPS25200 turns off the internal MOSFET in response to an overvoltage or overcurrent event. The TPS25200 can withstand the transient without a bypass bulk capacitor, or other external overvoltage protection components at input side. The TPS25200 also can be used at host side as a traditional power switch pin-to-pin compatible with the TPS2553.

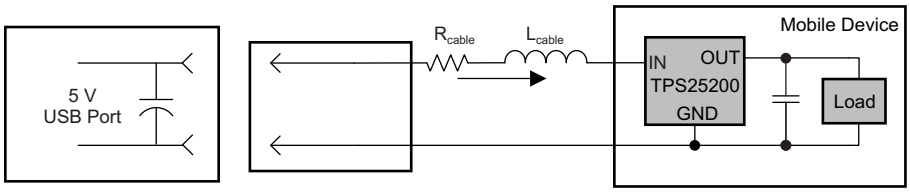


Figure 14. Hot Plug Into 5V USB port with Parasitic Cable Resistance and Inductance

9.2 Typical Application

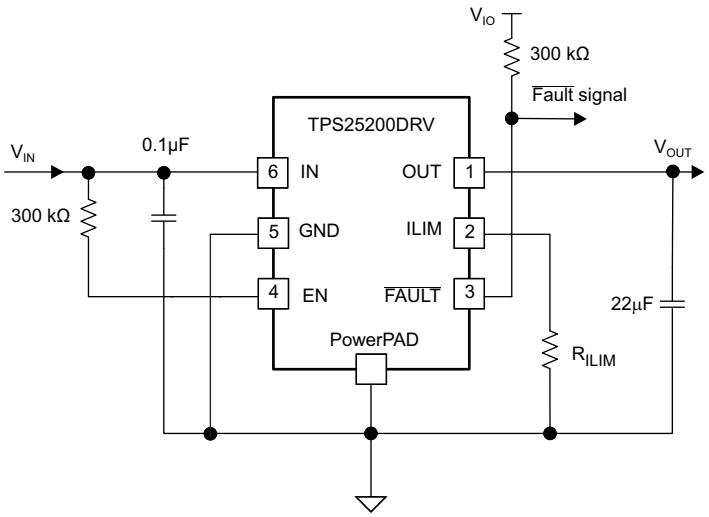


Figure 15. Overvoltage and Overcurrent Protector—Typical Application Schematic

Use the I_{OS} in the *Electrical Characteristics* table or I_{OS} in Equation 1 to select the R_{ILIM}.

9.2.1 Design Requirements

For this design example, use the desgin parameters in Table 1 as the input parameters.

Table 1. Design Parameters

DESIGN PARAMETERS	EXAMPLE VALUE
Normal input operation voltage	5 V
Output transient voltage	6.5 V
Minimum current limit	2.1 A
Maximum currnt limit	2.9 A

9.2.2 Detailed Design Procedure

9.2.2.1 Step by Step Design Produce

To begin the design process a few parameters must be decided upon. The designer needs to know the following:

- Normal Input Operation Voltage
- Output transient voltage
- Minimum Current Limit
- Maximum Current Limit

9.2.2.2 Input and Output Capacitance

Input and output capacitance improves the performance of the device; the actual capacitance must be optimized for the particular application. For all applications, a 0.1-µF or greater ceramic bypass capacitor between IN and GND is recommended as close to the device as possible for local noise decoupling.

When V_{IN} ramp up exceed 7.6 V, V_{OUT} follows V_{IN} until the TPS25200 turns off the internal MOSFET after $t_{(OVLO\_off\_delay)}$. Since $t_{(OVLO\_off\_delay)}$ largely depends on the V_{IN} ramp rate, V_{OUT} sees some peak voltage. Increasing the output capacitance can lower the output peak voltage as shown in Figure 16.

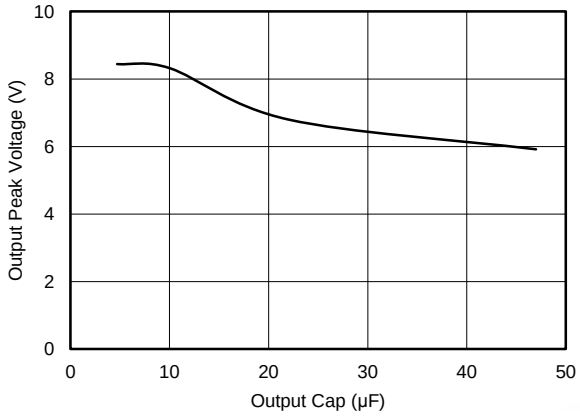


Figure 16. V_{OUT} Peak Voltage vs C_{OUT} (V_{IN} Step From 5 V to 15 V with 1-V/µs Ramp Up Rate)

9.2.2.3 Programming the Current-Limit Threshold

The overcurrent threshold is user programmable via an external resistor. The TPS25200 uses an internal regulation loop to provide a regulated voltage on the ILIM terminal. The current-limit threshold is proportional to the current sourced out of ILIM. The recommended 1% resistor range for R_{ILIM} is 33 kΩ ≤ R_{ILIM} ≤ 1100 kΩ to ensure stability of the internal regulation loop. Many applications require that the minimum current limit is above a certain current level or that the maximum current limit is below a certain current level, so it is important to consider the tolerance of the overcurrent threshold when selecting a value for R_{ILIM}. The current-limit threshold equations (IOS) in Equation 1 approximate the resulting overcurrent threshold for a given external resistor value R_{ILIM}. See the *Electrical Characteristics* table for specific current limit settings. The traces routing the R_{ILIM} resistor to the TPS25200 must be as short as possible to reduce parasitic effects on the current-limit accuracy.

R_{ILIM} can be selected to provide a current-limit threshold that occurs 1) above a minimum load current or 2) below a maximum load current.

To design above a minimum current-limit threshold, find the intersection of R_{ILIM} and the maximum desired load current on the $I_{OS(min)}$ curve and choose a value of R_{ILIM} below this value. Programming the current limit above a minimum threshold is important to ensure start up into full load or heavy capacitive loads. The resulting maximum current-limit threshold is the intersection of the selected value of R_{ILIM} and the $I_{OS(max)}$ curve.

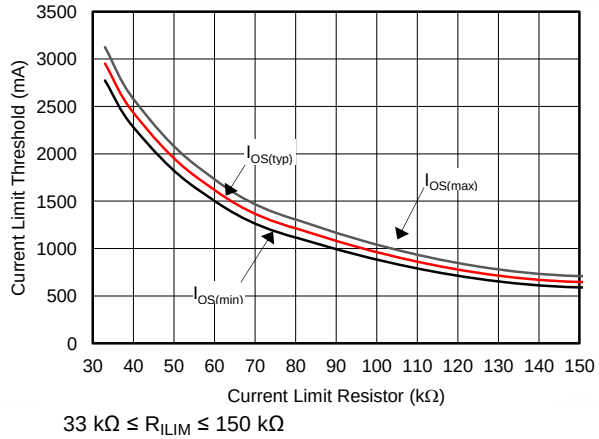
To design below a maximum current-limit threshold, find the intersection of R_{ILIM} and the maximum desired load current on the $I_{OS(max)}$ curve and choose a value of R_{ILIM} above this value. Programming the current limit below a maximum threshold is important to avoid current limiting upstream power supplies causing the input voltage bus to droop. The resulting minimum current-limit threshold is the intersection of the selected value of R_{ILIM} and the $I_{OS(min)}$ curve. See Figure 17 and Figure 18.

$$I_{OS\,max}(mA) = \frac{96754V}{R_{ILIM}^{0.985}k\Omega} + 30$$

$$I_{OS\,nom}(mA) = \frac{98322V}{R_{ILIM}^{1.003}k\Omega}$$

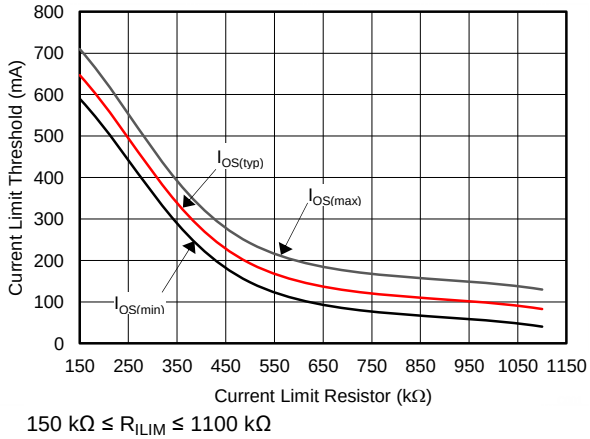
$$I_{OS\,min}(mA) = \frac{97399}{R_{ILIM}^{1.015}k\Omega} - 30 \quad (1)$$

Where 33 kΩ ≤ R_{ILIM} ≤ 1100 kΩ.



33 kΩ ≤ R_{ILIM} ≤ 150 kΩ

Figure 17. Current-Limit Threshold vs R_{ILIM} I



150 kΩ ≤ R_{ILIM} ≤ 1100 kΩ

Figure 18. Current-Limit Threshold vs R_{ILIM} II

9.2.2.4 Design Above a Minimum Current Limit

Some applications require that current limiting cannot occur below a certain threshold. For this example, assume that 2.1 A must be delivered to the load so that the minimum desired current-limit threshold is 2100 mA. Use the I_{OS} equations (Equation 1) and Figure 17 to select R_{ILIM} as shown in Equation 2.

$$I_{OS\,min}(mA) = 2100\ mA$$

$$I_{OS\,min}(mA) = \frac{97399V}{R_{ILIM}^{1.015}k\Omega} - 30$$

$$R_{ILIM}(k\Omega) = \left(\frac{97399}{I_{OS(min)} + 30}\right)^{\frac{1}{1.015}} = \left(\frac{97399}{2100 + 30}\right)^{\frac{1}{1.015}} = 43.22\ k\Omega \quad (2)$$

Select the closest 1% resistor less than the calculated value: R_{ILIM} = 42.2 kΩ. This sets the minimum current-limit threshold at 2130 mA as shown in Equation 3.

$$I_{OS\,min}(mA) = \frac{97399V}{R_{ILIM}^{1.015}k\Omega} - 30 = \frac{97399}{(42.2\ x\ 1.01)^{1.015}} - 30 = 2130mA \quad (3)$$

Use the I_{OS} equations (Equation 1), Figure 17, and the previously calculated value for R_{ILIM} to calculate the maximum resulting current-limit threshold as shown in Equation 4.

$$I_{OS\,max}(mA) = \frac{96754}{R_{ILIM}{}^{0.985}} + 30$$

$$I_{OS\,max}(mA) = \frac{96754}{(42.2 \times 0.99)^{0.985}} + 30 = 2479\ mA \tag{4}$$

The resulting current-limit threshold minimum is 2130 mA and maximum is 2479 mA with R_{ILIM} = 42.2kΩ ± 1%.

9.2.2.5 Design Below a Maximum Current Limit

Some applications require that current limiting must occur below a certain threshold. For this example, assume that 2.9 A must be delivered to the load so that the minimum desired current-limit threshold is 2900 mA. Use the I_{OS} equations (Equation 1) and Figure 18 to select R_{ILIM} as shown in Equation 5.

$$I_{OS\,max}(mA) = 2900mA$$

$$I_{OS\,max}(mA) = \frac{96754}{R_{ILIM}{}^{0.985}k\Omega} + 30$$

$$R_{ILIM}(k\Omega) = \left(\frac{96754}{I_{OS(max)} - 30}\right)^{\frac{1}{0.985}} = \left(\frac{96754}{2900 - 30}\right)^{\frac{1}{0.985}} = 35.57\ k\Omega \tag{5}$$

Select the closest 1% resistor greater than the calculated value: R_{ILIM} = 36 kΩ. This sets the maximum current-limit threshold at 2894 mA as shown in Equation 6.

$$I_{OS\,max}(mA) = \frac{96754V}{R_{ILIM}{}^{0.985}k\Omega} + 30 = \frac{96754}{(36\ x\ 0.99)^{0.985}} + 30 = 2894mA \tag{6}$$

Use the I_{OS} equations, Figure 18, and the previously calculated value for R_{ILIM} to calculate the minimum resulting current-limit threshold as shown in Equation 7.

$$I_{OS\,min}(mA) = \frac{97399}{R_{ILIM}{}^{1.015}} - 30$$

$$I_{OS\,min}(mA) = \frac{97399}{(36 \times 1.01)^{1.015}} - 30 = 2508mA \tag{7}$$

The resulting minimum current-limit threshold minimum is 2592 mA and maximum is 2894 mA with R_{ILIM} = 36 kΩ ± 1%.

9.2.2.6 Power Dissipation and Junction Temperature

The low on-resistance of the internal N-channel MOSFET allows small surface-mount packages to pass large currents. It is good design practice to estimate power dissipation and junction temperature. The below analysis gives an approximation for calculating junction temperature based on the power dissipation in the package. However, it is important to note that thermal analysis is strongly dependent on additional system level factors. Such factors include air flow, board layout, copper thickness and surface area, and proximity to other devices dissipating power. Good thermal design practice must include all system level factors in addition to individual component analysis. Begin by determining the $r_{DS(on)}$ of the N-channel MOSFET relative to the input voltage and operating temperature. As an initial estimate, use the highest operating ambient temperature of interest and read $r_{DS(on)}$ from the typical characteristics graph. When V_{IN} is lower than $V_{(OVC)}$, the TPS2500 is an traditional power switch. Using this value, the power dissipation can be calculated by usnig Equation 8.

$$P_D = r_{DS(on)} \times I_{OUT}^2 \quad (8)$$

When V_{IN} exceed $V_{(OVC)}$, but lower than $V_{(OVLO)}$, the TPS25200 clamp output to fixed $V_{(OVC)}$, the power dissipation can be calculated by using Equation 9.

$$P_D = (V_{IN} - V_{(OVC)}) \times I_{OUT} \quad (9)$$

where

- P_D = Total power dissipation (W)
- $r_{DS(on)}$ = Power switch on-resistance (Ω)
- $V_{(OVC)}$ = Overvoltage clamp voltage (V)
- I_{OUT} = Maximum current-limit threshold (A)

This step calculates the total power dissipation of the N-channel MOSFET.

Finally, calculate the junction temperature using Equation 10.

$$T_J = P_D \times \theta_{JA} + T_A \quad (10)$$

where

- T_A = Ambient temperature (°C)
- θ_{JA} = Thermal resistance (°C /W)
- P_D = Total power dissipation (W)

Compare the calculated junction temperature with the initial estimate. If they are not within a few degrees, repeat the calculation using the "refined" $r_{DS(on)}$ from the previous calculation as the new estimate. Two or three iterations are generally sufficient to achieve the desired result. The final junction temperature is highly dependent on thermal resistance θ_{JA}, and thermal resistance is highly dependent on the individual package and board layout.

9.2.3 Application Curves

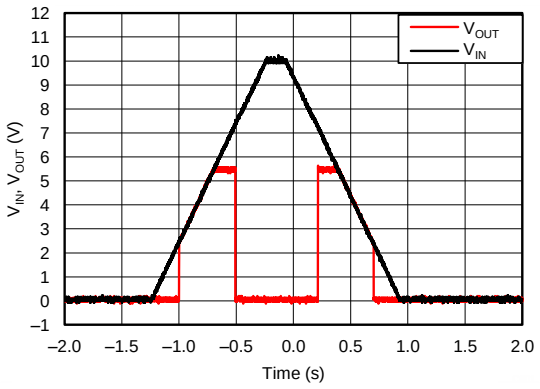


Figure 19. V_{OUT} vs V_{IN} (0 V to 10 V)

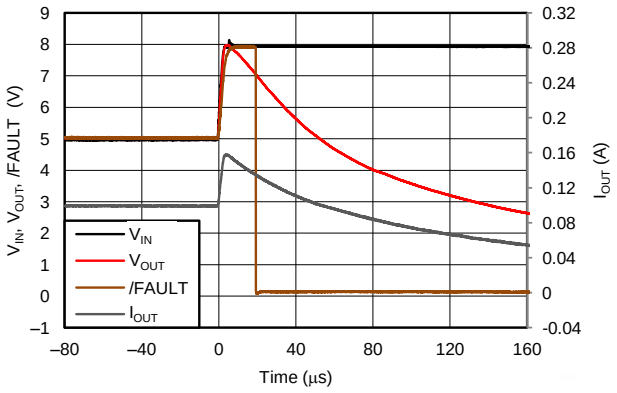


Figure 20. V_{IN} Step 5 V to 8 V With 4.7 µF // 100 Ω

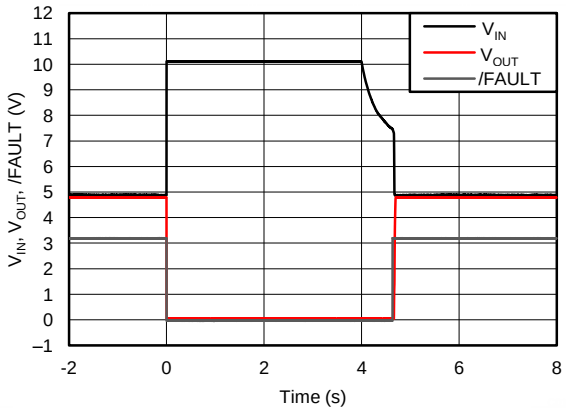


Figure 21. Pulse Overvoltage With 100 Ω

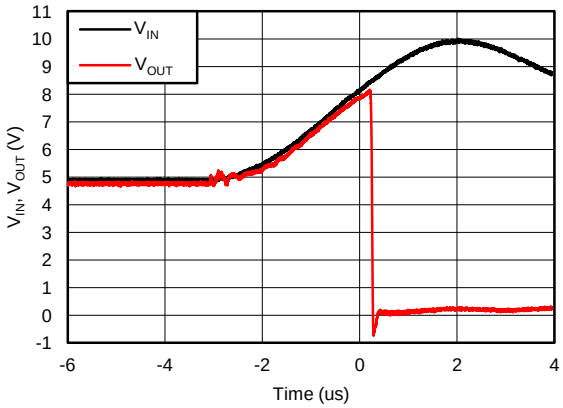


Figure 22. 5 V to 10 V OVLO Response Time

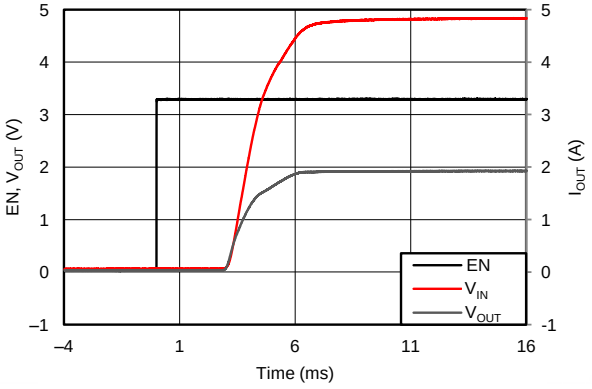


Figure 23. Turnon Delay and Rise Time 150 µF || 2.5 Ω

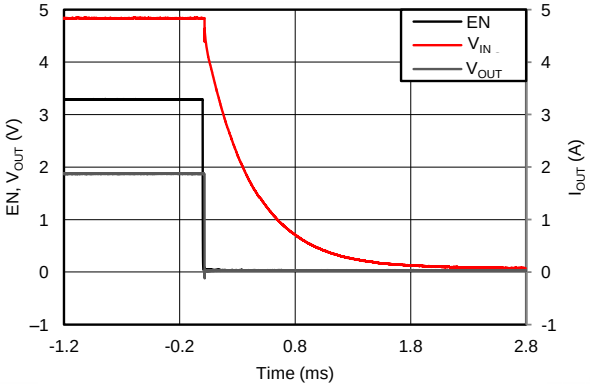


Figure 24. Turnoff Delay and Fall Time 150 µF || 2.5 Ω

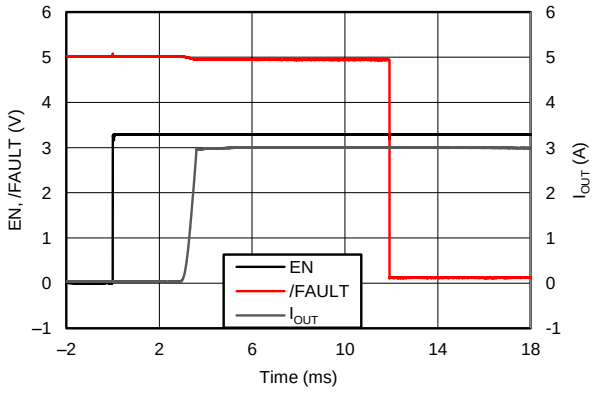


Figure 25. Enable into Output Short

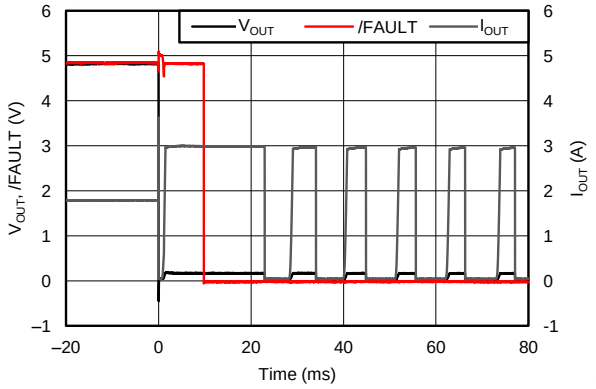


Figure 26. 2.5 Ω to Output Short Transient Response

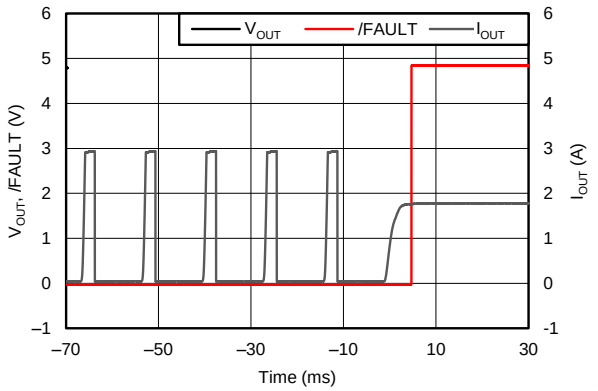


Figure 27. Output Short to 2.5-Ω Load Recovery Response

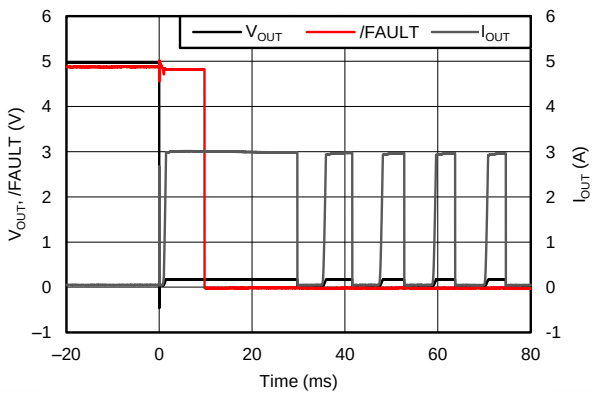


Figure 28. No Load to Output Short Transient Response

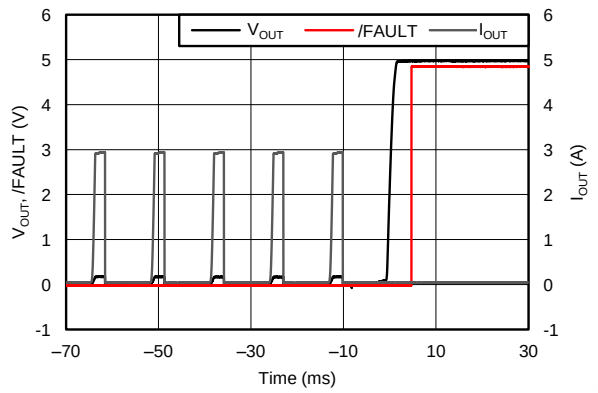


Figure 29. Output Short to No Load Recovery Response

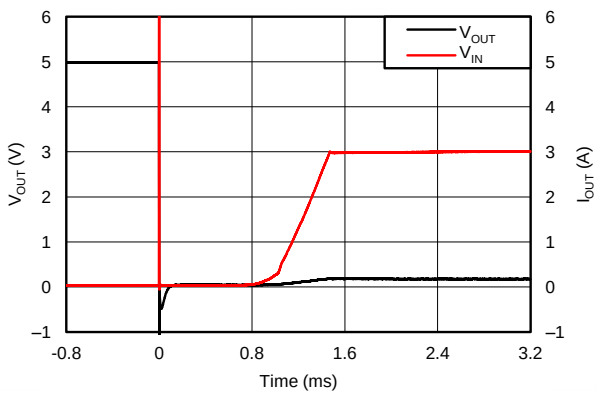


Figure 30. Hot-Short With 50 mΩ

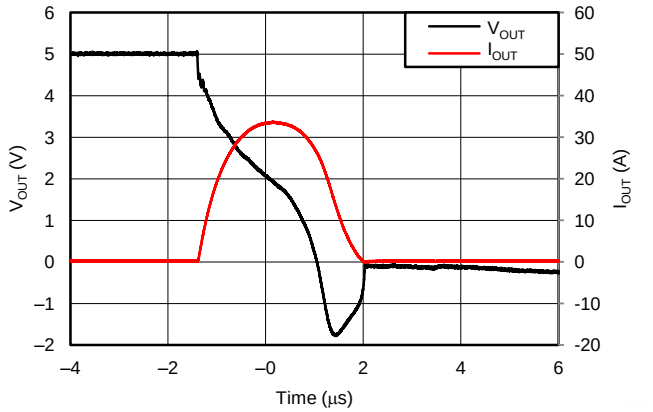


Figure 31. 50-mΩ Hot-Short Response Time

10 Power Supply Recommendations

The TPS25200 is designed for 2.7 V < V_{IN} < 5 V (typical) voltage rails. While there is a V_{OUT} clamp, it is not intended to be used to regulate V_{OUT} at approximately 5.4 V with 6 V < V_{IN} < 7 V. This is a protection feature only.

11 Layout

11.1 Layout Guidelines

- For all applications, a 0.1-µF or greater ceramic bypass capacitor between IN and GND is recommended as close to the device as possible for local noise decoupling.
- For output capacitance, refer to Figure 16, low ESR ceramic cap is recommended.
- The traces routing the R_{ILIM} resistor to the device must be as short as possible to reduce parasitic effects on the current limit accuracy.
- The PowerPAD must be directly connected to PCB ground plane using wide and short copper trace.

11.2 Layout Example

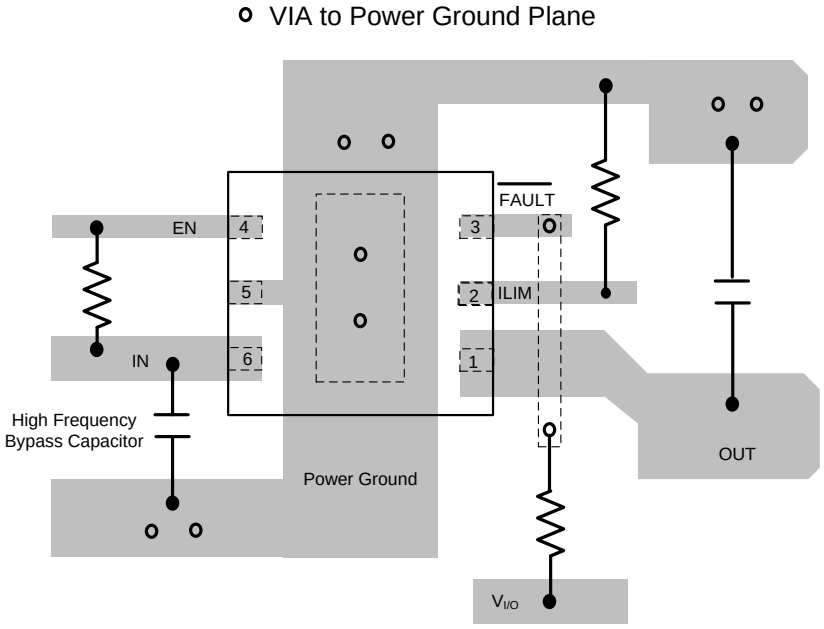


Figure 32. TPS25200 Board Layout

12 器件和文档支持

12.1 文档支持

12.1.1 相关文档

相关文档如下：

TPS25200 EVM 用户指南

12.2 接收文档更新通知

如需接收文档更新通知，请访问 ti.com 上的器件产品文件夹。点击右上角的*提醒我* (Alert me) 注册后，即可每周定期收到已更改的产品信息。有关更改的详细信息，请查阅已修订文档中包含的修订历史记录。

12.3 社区资源

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.4 商标

PowerPAD, E2E are trademarks of Texas Instruments.
All other trademarks are the property of their respective owners.

12.5 静电放电警告

这些装置包含有限的内置 ESD 保护。 存储或装卸时，应将导线一起截短或将装置放置于导电泡棉中，以防止 MOS 门极遭受静电损伤。

12.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 机械、封装和可订购信息

以下页中包括机械封装和可订购信息。这些信息是针对指定器件可提供的最新数据。这些数据会在无通知且不对本文档进行修订的情况下发生改变。欲获得该数据表的浏览器版本，请查阅左侧的导航栏

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS25200DRVR	ACTIVE	WSON	DRV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	SKB	Samples
TPS25200DRVT	ACTIVE	WSON	DRV	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	SKB	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF TPS25200 :

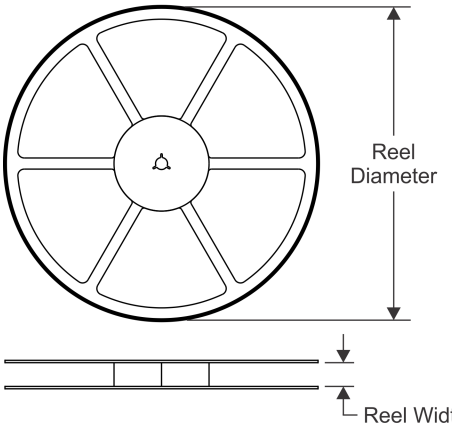
- Automotive: TPS25200-Q1

NOTE: Qualified Version Definitions:

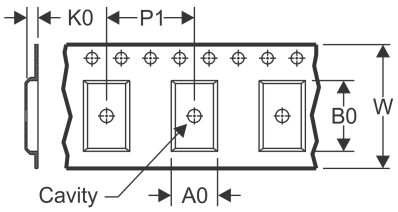
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

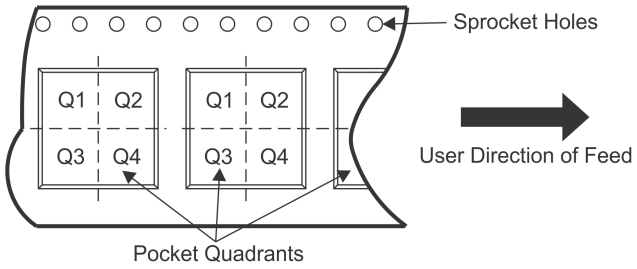


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

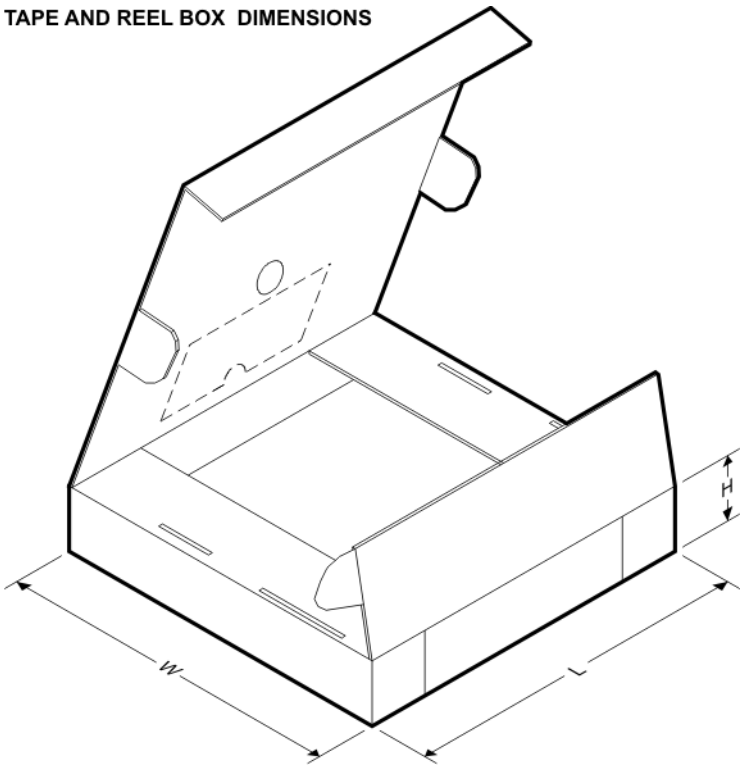
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS25200DRVR	WSON	DRV	6	3000	178.0	8.4	2.25	2.25	1.0	4.0	8.0	Q2
TPS25200DRVT	WSON	DRV	6	250	178.0	8.4	2.25	2.25	1.0	4.0	8.0	Q2

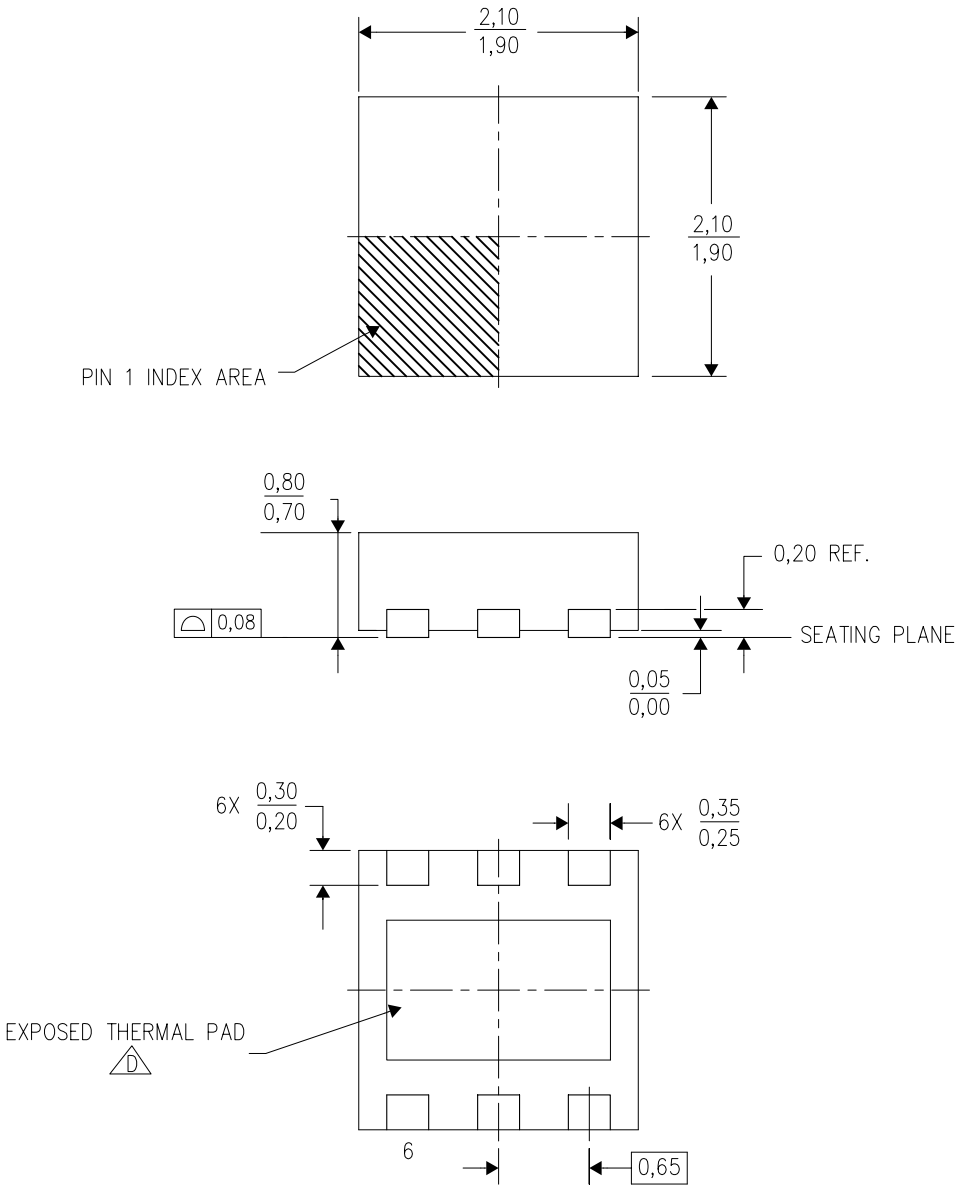
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS25200DRVR	WSON	DRV	6	3000	205.0	200.0	33.0
TPS25200DRVT	WSON	DRV	6	250	205.0	200.0	33.0

DRV (S–PWSON–N6) PLASTIC SMALL OUTLINE NO–LEAD



4206925/E 10/10

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Small Outline No–Lead (SON) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.

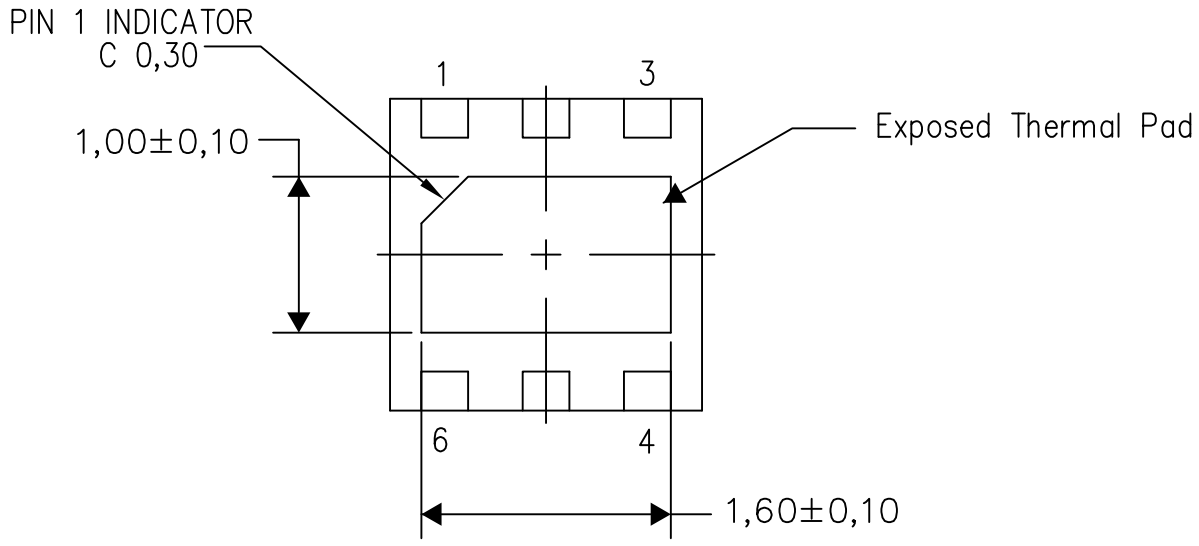
DRV (S–PWSON–N6) PLASTIC SMALL OUTLINE NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



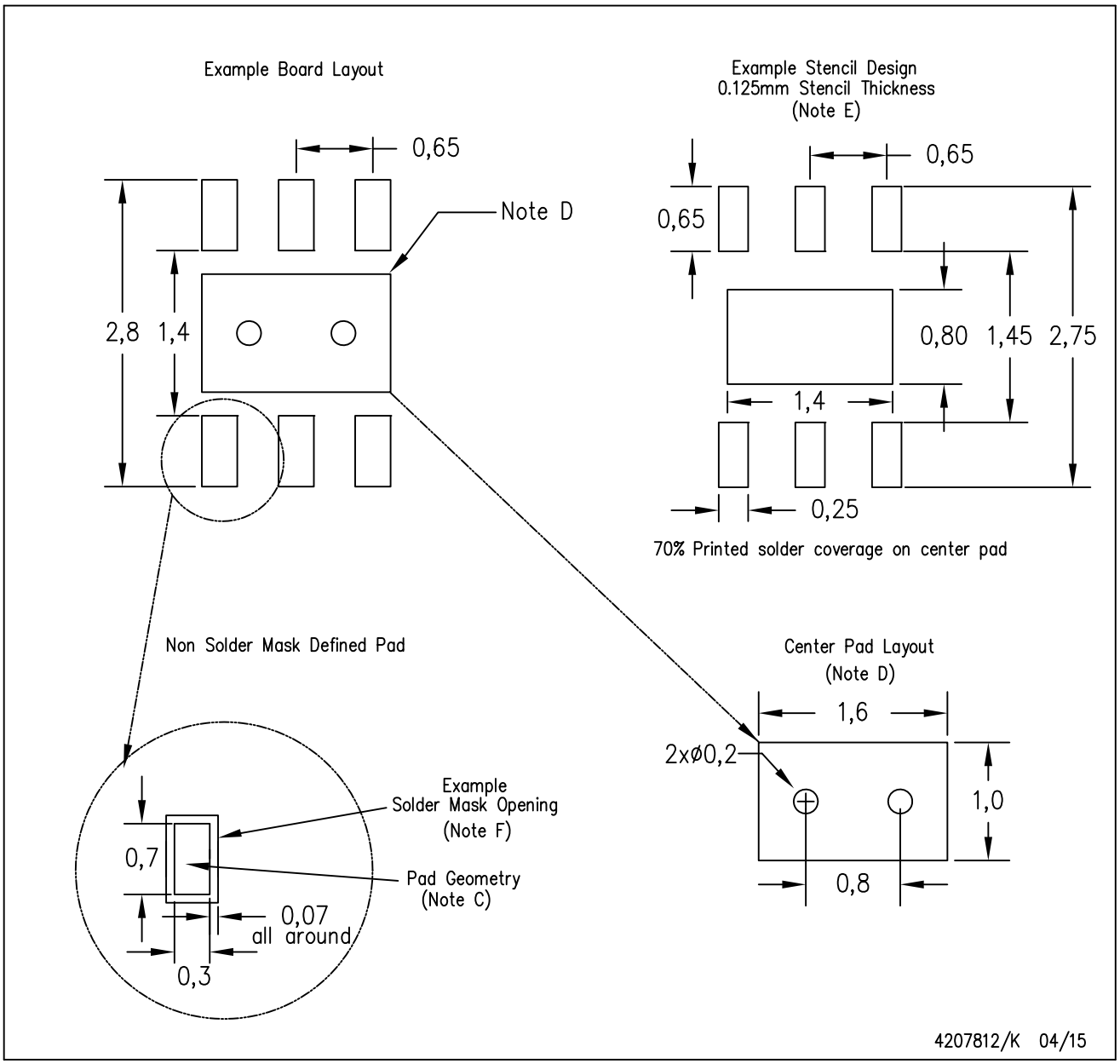
Bottom View

Exposed Thermal Pad Dimensions

4206926/Q 04/15

NOTE: All linear dimensions are in millimeters

DRV (S–PWSON–N6) PLASTIC SMALL OUTLINE NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for solder mask tolerances.

重要声明

德州仪器 (TI) 公司有权按照最新发布的 JESD46 对其半导体产品和服务进行纠正、增强、改进和其他修改，并不再按最新发布的 JESD48 提供任何产品和服务。买方在下订单前应获取最新的相关信息，并验证这些信息是否完整且是最新的。

TI 公布的半导体产品销售条款 (http://www.ti.com/sc/docs/stdterms.htm) 适用于 TI 已认证和批准上市的已封装集成电路产品的销售。另有其他条款可能适用于其他类型 TI 产品及服务的使用或销售。

复制 TI 数据表上 TI 信息的重要部分时，不得变更该等信息，且必须随附所有相关保证、条件、限制和通知，否则不得复制。TI 对该等复制文件不承担任何责任。第三方信息可能受到其它限制条件的制约。在转售 TI 产品或服务时，如果存在对产品或服务参数的虚假陈述，则会失去相关 TI 产品或服务的明示或暗示保证，且构成不公平的、欺诈性商业行为。TI 对此类虚假陈述不承担任何责任。

买方和在系统中整合 TI 产品的其他开发人员（总称“设计人员”）理解并同意，设计人员在设计应用时应自行实施独立的分析、评价和判断，且应全权 负责并确保 应用的安全性， 及设计人员的 应用 （包括应用中使用的所有 TI 产品）应符合所有适用的法律法规及其他相关要求。设计人员就自己设计的 应用声明，其具备制订和实施下列保障措施所需的一切必要专业知识，能够 (1) 预见故障的危险后果，(2) 监视故障及其后果，以及 (3) 降低可能导致危险的故障几率并采取适当措施。设计人员同意，在使用或分发包含 TI 产品的任何 应用前， 将彻底测试该等 应用和 该等应用中所用 TI 产品的 功能。

TI 提供技术、应用或其他设计建议、质量特点、可靠性数据或其他服务或信息，包括但不限于与评估模块有关的参考设计和材料（总称“TI 资源”），旨在帮助设计人员开发整合了 TI 产品的 应用， 如果设计人员（个人，或如果是代表公司，则为设计人员的公司）以任何方式下载、访问或使用任何特定的 TI 资源，即表示其同意仅为该等目标，按照本通知的条款使用任何特定 TI 资源。

TI 所提供的 TI 资源，并未扩大或以其他方式修改 TI 对 TI 产品的公开适用的质保及质保免责声明；也未导致 TI 承担任何额外的义务或责任。TI 有权对其 TI 资源进行纠正、增强、改进和其他修改。除特定 TI 资源的公开文档中明确列出的测试外，TI 未进行任何其他测试。

设计人员只有在开发包含该等 TI 资源所列 TI 产品的 应用时， 才被授权使用、复制和修改任何相关单项 TI 资源。但并未依据禁止反言原则或其他法理授予您任何TI知识产权的任何其他明示或默示的许可，也未授予您 TI 或第三方的任何技术或知识产权的许可，该等产权包括但不限于任何专利权、版权、屏蔽作品权或与使用TI产品或服务的任何整合、机器制作、流程相关的其他知识产权。涉及或参考了第三方产品或服务的信息不构成使用此类产品或服务的许可或与其相关的保证或认可。使用 TI 资源可能需要您向第三方获得对该等第三方专利或其他知识产权的许可。

TI 资源系“按原样”提供。TI 兹免除对资源及其使用作出所有其他明确或默认的保证或陈述，包括但不限于对准确性或完整性、产权保证、无屡发故障保证，以及适销性、适合特定用途和不侵犯任何第三方知识产权的任何默认保证。TI 不负责任何申索，包括但不限于因组合产品所致或与之有关的申索，也不为或对设计人员进行辩护或赔偿，即使该等产品组合已列于 TI 资源或其他地方。对因 TI 资源或其使用引起或与之有关的任何实际的、直接的、特殊的、附带的、间接的、惩罚性的、偶发的、从属或惩戒性损害赔偿，不管 TI 是否获悉可能会产生上述损害赔偿，TI 概不负责。

除 TI 已明确指出特定产品已达到特定行业标准（例如 ISO/TS 16949 和 ISO 26262）的要求外，TI 不对未达到任何该等行业标准要求而承担任何责任。

如果 TI 明确宣称产品有助于功能安全或符合行业功能安全标准，则该等产品旨在帮助客户设计和创作自己的 符合 相关功能安全标准和要求的应用。在应用内使用产品的行为本身不会 配有 任何安全特性。设计人员必须确保遵守适用于其应用的相关安全要求和 标准。设计人员不可将任何 TI 产品用于关乎性命的医疗设备，除非已由各方获得授权的管理人员签署专门的合同对此类应用专门作出规定。关乎性命的医疗设备是指出现故障会导致严重身体伤害或死亡的医疗设备（例如生命保障设备、心脏起搏器、心脏除颤器、人工心脏泵、神经刺激器以及植入设备）。此类设备包括但不限于，美国食品药品监督管理局认定为 III 类设备的设备，以及在美国以外的其他国家或地区认定为同等类别设备的所有医疗设备。

TI 可能明确指定某些产品具备某些特定资格（例如 Q100、军用级或增强型产品）。设计人员同意，其具备一切必要专业知识，可以为自己的应用选择适合的 产品， 并且正确选择产品的风险由设计人员承担。设计人员单方面负责遵守与该等选择有关的所有法律或监管要求。

设计人员同意向 TI 及其代表全额赔偿因其不遵守本通知条款和条件而引起的任何损害、费用、损失和/或责任。

邮寄地址：上海市浦东新区世纪大道 1568 号中建大厦 32 楼，邮政编码：200122