TLV733P-Q1 Capacitor-Free, 300-mA, Low Dropout (LDO) Linear Regulator

1 Features

- Qualified for Automotive Applications
- AEC-Q100 Qualified:
  - Device Temperature Grade 1: –40°C to 125°C Ambient Operating Temperature
  - Device HBM ESD Classification Level 2
  - Device CDM ESD Classification Level C4B
- Input Voltage Range: 1.4 V to 5.5 V
- Stable Operation With or Without Capacitors
- Foldback Overcurrent Protection
- Package:
  - 2.0-mm × 2.0-mm WSON-6
- Very Low Dropout: 125 mV at 300 mA (3.3 V_{OUT})
- Accuracy: 1% Typical, 1.4% Maximum
- Low I_Q: 34 µA
- Available in Fixed-Output Voltages: 1.0 V to 3.3 V
- High PSRR: 50 dB at 1 kHz
- Active Output Discharge

2 Applications

- Camera Modules
- Automotive Infotainment
- Navigation Systems

3 Description

The TLV733P-Q1 family of low dropout (LDO) linear regulators are ultra-small, low quiescent current LDOs that can source 300 mA with good line and load transient performance. These devices provide a typical accuracy of 1%.

The TLV733P-Q1 family is designed with a modern capacitor-free architecture to ensure stability without an input or output capacitor. The removal of the output capacitor allows for a very small solution size, and can eliminate inrush current at startup. Furthermore, the TLV733P-Q1 family is also stable with ceramic output capacitors if an output capacitor is necessary. The TLV733P-Q1 family also provides foldback current control during device power-up and enabling if an output capacitor is used. This functionality is especially important in battery-operated devices.

The TLV733P-Q1 family provides an active pulldown circuit to quickly discharge output loads when disabled.

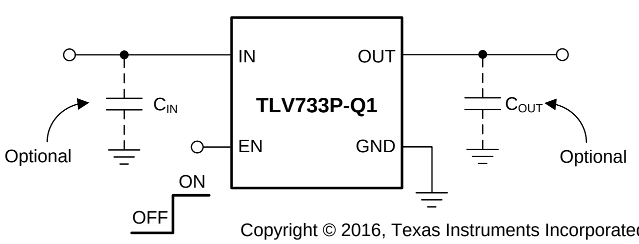
The TLV733P-Q1 family is available in the 6-pin DRV (WSON) package.

Device Information(1)

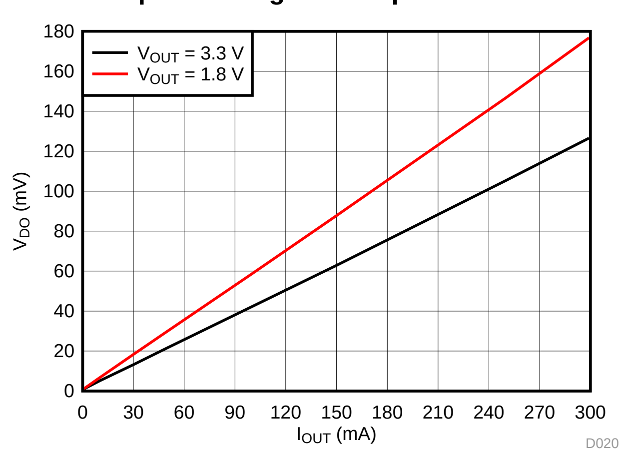
PART NUMBER	PACKAGE	BODY SIZE (NOM)
TLV733P-Q1	WSON (6)	2.00 mm × 2.00 mm

(1) For all available packages, see the package option addendum at the end of the data sheet.

Typical Application Circuit



Dropout Voltage vs Output Current



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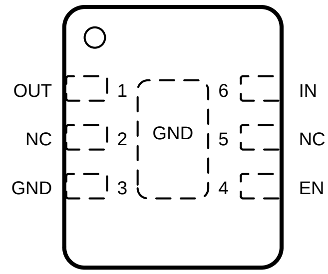
4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (August 2016) to Revision A	Page
• Released to production	1

5 Pin Configuration and Functions

DRV Package
6-Pin WSON
Top View



Not to scale

Pin Functions

NAME	NO.	I/O	DESCRIPTION
EN	4	I	Enable pin. Drive EN greater than 0.9 V to turn on the regulator. Drive EN less than 0.35 V to put the LDO into shutdown mode.
GND	3	—	Ground pin
IN	6	I	Input pin. A small capacitor is recommended from this pin to ground. See the *Input and Output Capacitor Selection* section for more details.
NC	2, 5	—	No internal connection
OUT	1	O	Regulated output voltage pin. For best transient response, use a small 1-µF ceramic capacitor from this pin to ground. See the *Input and Output Capacitor Selection* section for more details.
Thermal pad		—	The thermal pad is electrically connected to the GND node. Connect to the GND plane for improved thermal performance.

6 Specifications

6.1 Absolute Maximum Ratings

over operating junction temperature range (unless otherwise noted); all voltages are with respect to GND[(1)]

		MIN	MAX	UNIT
Voltage	V_{IN}	–0.3	6.0	V
	V_{EN}	–0.3	V_{IN} + 0.3	
	V_{OUT}	–0.3	3.6	
Current	I_{OUT}	Internally limited		A
Output short-circuit duration		Indefinite		
Temperature	Operating junction, T_J	–40	150	°C
	Storage, T_{stg}	–65	160	

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002[(1)]		±2000	V
		Charged-device model (CDM), per AEC Q100-011	All pins	±500	
			Corner pins (1, 3, 4, and 6)	±750	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Recommended Operating Conditions

over operating junction temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{IN}	Input range	1.4		5.5	V
V_{OUT}	Output range	1.0		3.3	V
I_{OUT}	Output current	0		300	mA
V_{EN}	Enable range	0		V_{IN}	V
T_J	Junction temperature	–40		135	°C
T_A	Ambient temperature	–40		125	°C

6.4 Thermal Information

THERMAL METRIC[(1)]		TLV733P-Q1 DRV (WSON) 6 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	92.5	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	123.9	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	61.9	°C/W
ψ_{JT}	Junction-to-top characterization parameter	9.7	°C/W
ψ_{JB}	Junction-to-board characterization parameter	62.3	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	30.9	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Electrical Characteristics

at operating temperature range (T_J, T_A = –40°C to +125°C), V_{IN} = $V_{OUT(nom)}$ + 0.5 V or 2.0 V (whichever is greater), I_{OUT} = 1 mA, V_{EN} = V_{IN}, and C_{IN} = C_{OUT} = 1 µF (unless otherwise noted); all typical values are at T_J = 25°C

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{IN}	Input voltage			1.4		5.5	V
	DC output accuracy	T_J = 25°C		–1%		1%	
		–40°C ≤ T_J ≤ 125°C		–1.4%		1.4%	
UVLO	Undervoltage lockout	V_{IN} rising			1.3	1.4	V
		V_{IN} falling			1.25		
$\Delta V_{O(\Delta VI)}$	Line regulation	ΔVI = $V_{OUT(nom)}$ + 0.5 V or 2.0 V (whichever is greater) to 5.5 V			1		mV
$\Delta V_{O(\Delta IO)}$	Load regulation	ΔIO = 1 mA to 300 mA			25		mV
V_{DO}	Dropout voltage (1)	V_{OUT} = 0.98 × $V_{OUT(nom)}$, I_{OUT} = 300 mA	V_{OUT} = 1.1 V, –40°C ≤ T_J ≤ 125°C			510	mV
			1.2 V ≤ V_{OUT} < 1.5 V, –40°C ≤ T_J ≤ 125°C			450	
			1.5 V ≤ V_{OUT} < 1.8 V, –40°C ≤ T_J ≤ 125°C			400	
			1.8 V ≤ V_{OUT} < 2.5 V, –40°C ≤ T_J ≤ 125°C			300	
			2.5 V ≤ V_{OUT} < 3.3 V, –40°C ≤ T_J ≤ 125°C			290	
			V_{OUT} = 3.3 V, –40°C ≤ T_J ≤ 125°C		125	270	
I_{GND}	Ground pin current	I_{OUT} = 0 mA			34	62	µA
I_{SHDN}	Shutdown current	V_{EN} ≤ 0.35 V, 2.0 V ≤ V_{IN} ≤ 5.5 V, T_J = 25°C			0.1	1	µA
PSRR	Power-supply rejection ratio	V_{OUT} = 1.8 V, I_{OUT} = 300 mA	f = 100 Hz		68		dB
			f = 10 kHz		35		
			f = 100 kHz		28		
V_n	Output noise voltage	BW = 10 Hz to 100 kHz, V_{OUT} = 1.8 V, I_{OUT} = 10 mA			120		μV_{RMS}
$V_{EN(HI)}$	EN pin high voltage (enabled)			0.9	0.63		V
$V_{EN(LO)}$	EN pin low voltage (disabled)				0.52	0.35	V
I_{EN}	EN pin current	V_{EN} = 5.5 V			0.01		µA
	Pulldown resistor	V_{IN} = 2.3 V			120		Ω
I_{LIM}	Output current limit			360			mA
I_{OS}	Short-circuit current limit	V_{OUT} shorted to GND, V_{OUT} = 1.0 V			150		mA
		V_{OUT} shorted to GND, V_{OUT} = 3.3 V			170		
T_{sd}	Thermal shutdown	Shutdown, temperature increasing			160		°C
		Reset, temperature decreasing			140		

(1) Dropout voltage for the TLV73310P is not valid at room temperature. The device engages undervoltage lockout (V_{IN} < $UVLO_{FALL}$) before the dropout condition is met.

6.6 Timing Requirements

			MIN	NOM	MAX	UNIT
t_{STR}	Startup time	Time from EN assertion to 98% × $V_{OUT(nom)}$, V_{OUT} = 1.0 V, I_{OUT} = 0 mA		250		µs
		Time from EN assertion to 98% × $V_{OUT(nom)}$, V_{OUT} = 3.3 V, I_{OUT} = 0 mA		800		

6.7 Typical Characteristics

at operating temperature range (T_J = –40°C to +125°C), V_{IN} = $V_{OUT(nom)}$ + 0.5 V or 2.0 V (whichever is greater), I_{OUT} = 1 mA, V_{EN} = V_{IN}, and C_{IN} = C_{OUT} = 1 µF (unless otherwise noted)

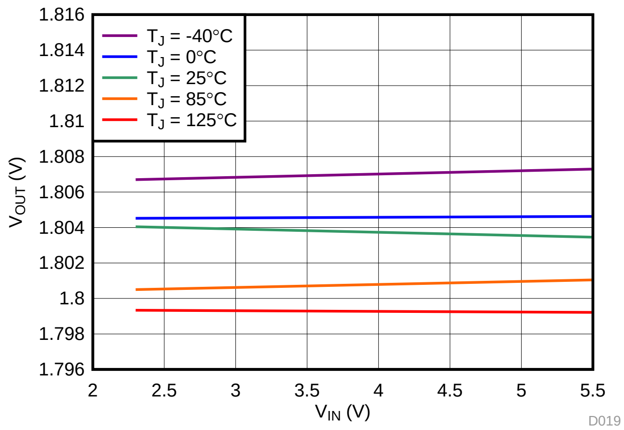


Figure 1. 1.8-V Regulation vs V_{IN} (Line Regulation) and Temperature

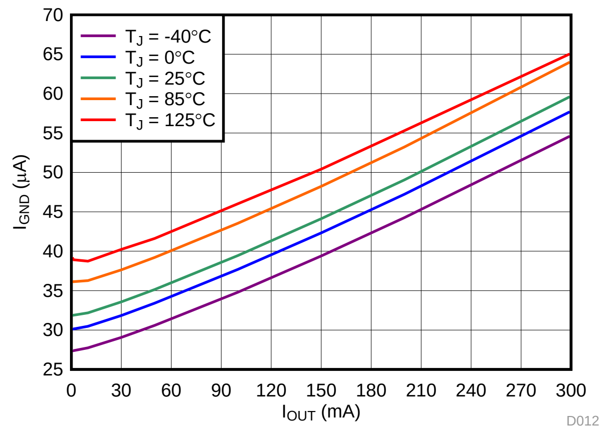


Figure 2. Ground Pin Current vs I_{OUT} and Temperature

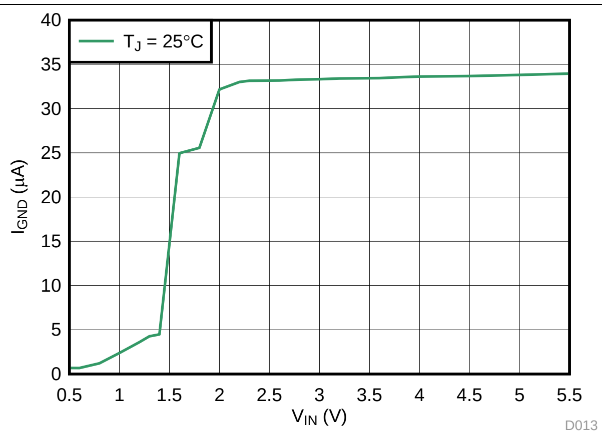


Figure 3. Ground Pin Current vs V_{IN}

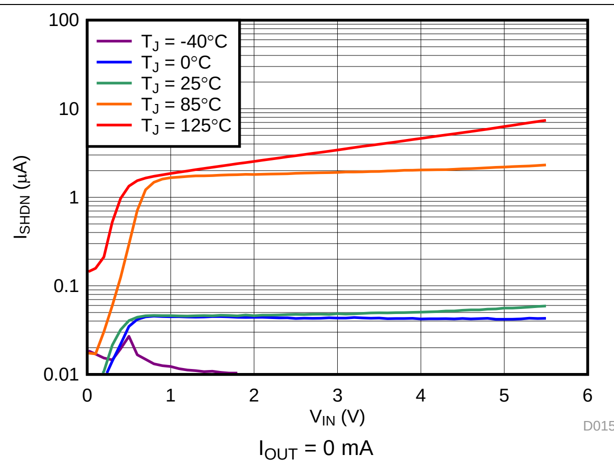


Figure 4. Shutdown Current vs V_{IN} and Temperature

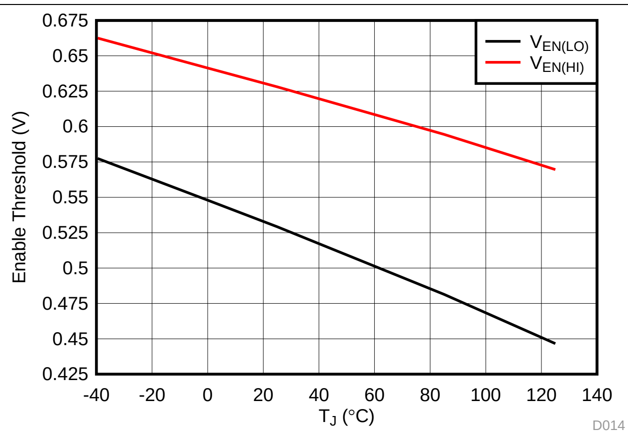


Figure 5. Enable Threshold vs Temperature

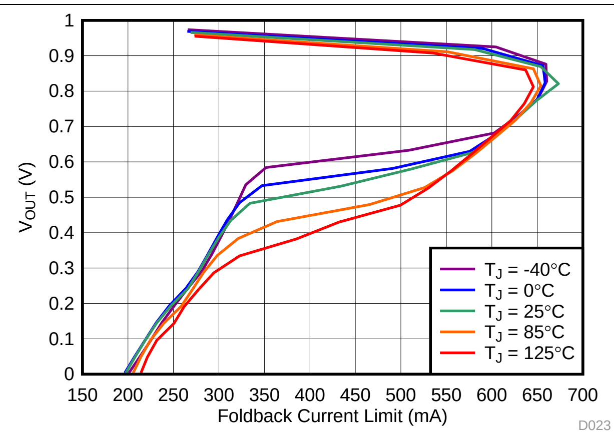


Figure 6. Output Voltage vs 1.0-V Foldback Current Limit and Temperature

Typical Characteristics (continued)

at operating temperature range (T_J = –40°C to +125°C), V_{IN} = $V_{OUT(nom)}$ + 0.5 V or 2.0 V (whichever is greater), I_{OUT} = 1 mA, V_{EN} = V_{IN}, and C_{IN} = C_{OUT} = 1 µF (unless otherwise noted)

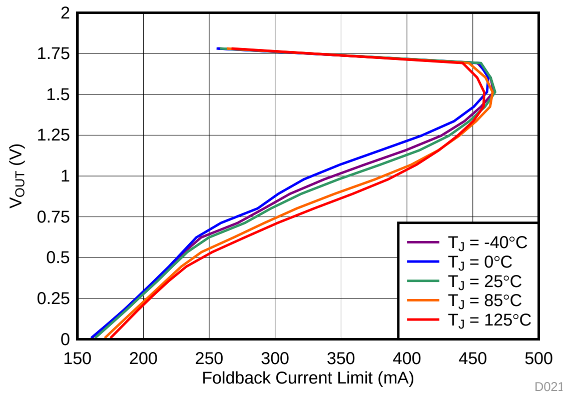


Figure 7. Output Voltage vs 1.8-V Foldback Current Limit and Temperature

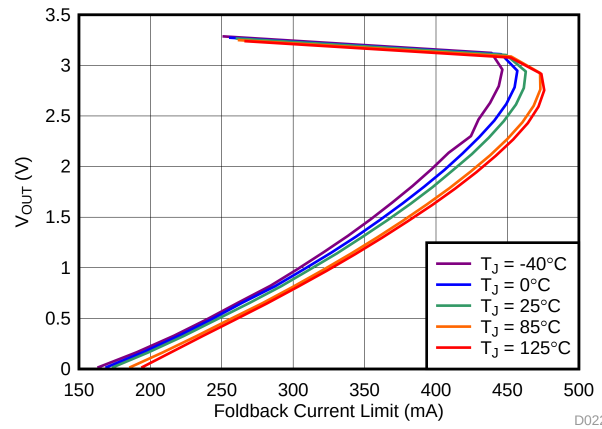
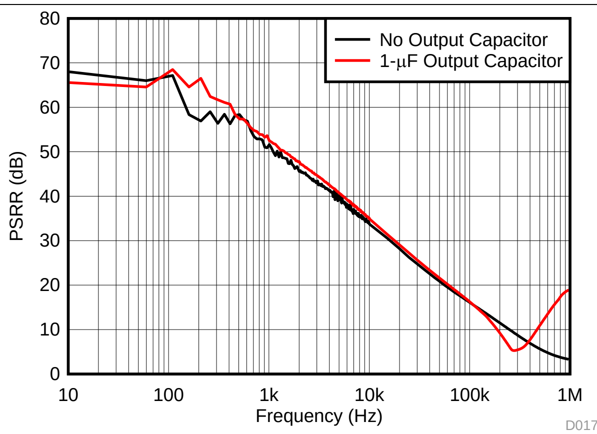
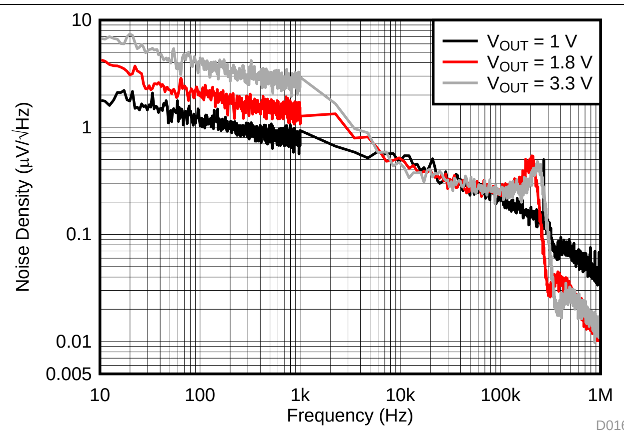


Figure 8. Output Voltage vs 3.3-V Foldback Current Limit and Temperature



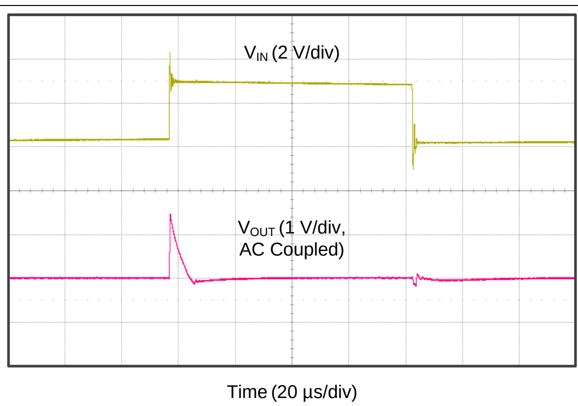
I_{OUT} = 300 mA

Figure 9. Power-Supply Rejection Ratio vs Frequency



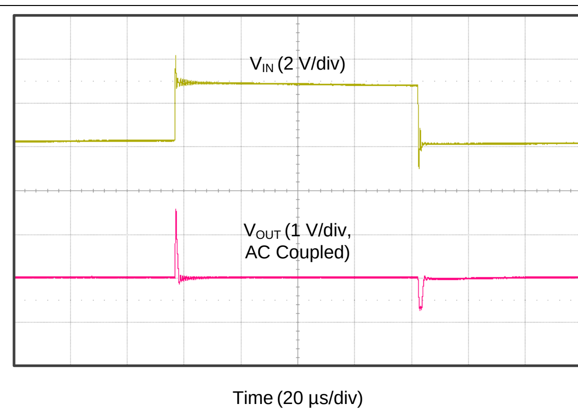
I_{OUT} = 300 mA

Figure 10. Output Spectral Noise Density vs Frequency and Output Voltage



I_{OUT} = 10 mA, 1-µF output capacitor

Figure 11. Line Transient

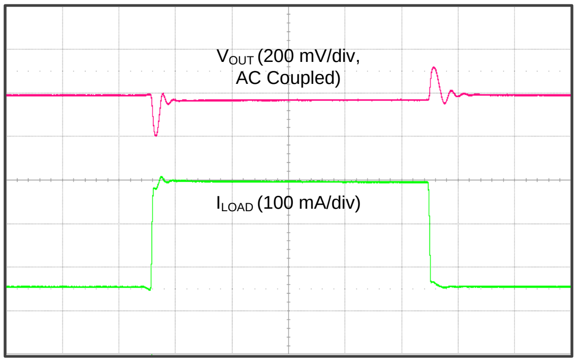


I_{OUT} = 300 mA, 1-µF output capacitor

Figure 12. Line Transient

Typical Characteristics (continued)

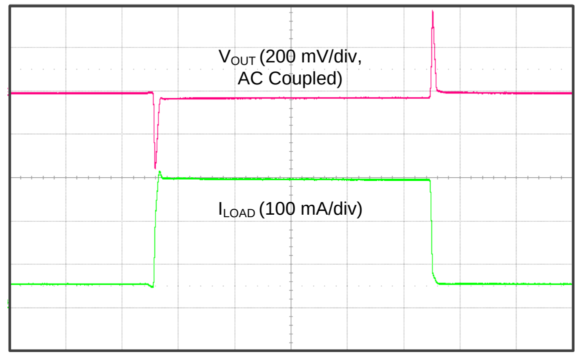
at operating temperature range (T_J = –40°C to +125°C), V_{IN} = $V_{OUT(nom)}$ + 0.5 V or 2.0 V (whichever is greater), I_{OUT} = 1 mA, V_{EN} = V_{IN}, and C_{IN} = C_{OUT} = 1 µF (unless otherwise noted)



Time (20 µs/div)

V_{IN} = 2.0 V, 1-µF output capacitor, output current slew rate = 0.25 A/µs

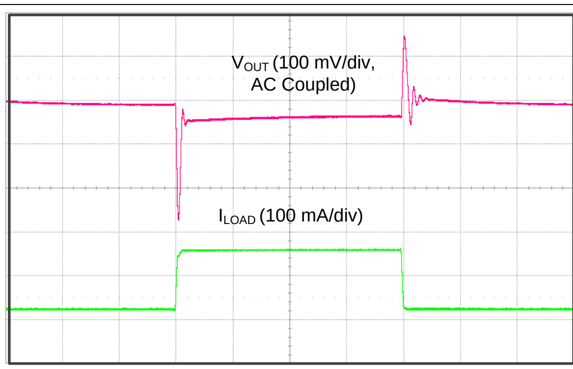
Figure 13. 1.0-V, 50-mA to 300-mA Load Transient



Time (20 µs/div)

V_{IN} = 2.0 V, no output capacitor, output current slew rate = 0.25 A/µs

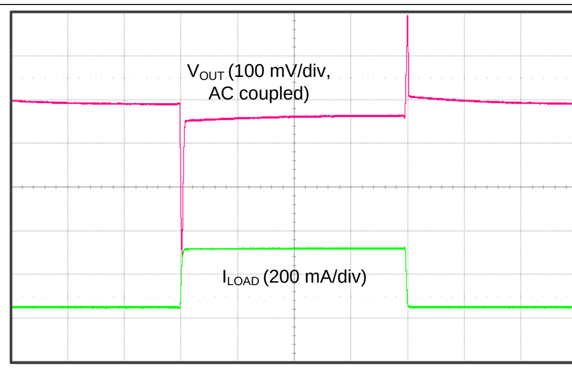
Figure 14. 1.0 V, 50-mA to 300-mA Load Transient



Time (20 µs/div)

V_{IN} = 3.8 V,1-µF output capacitor, output current slew rate = 0.25 A/µs

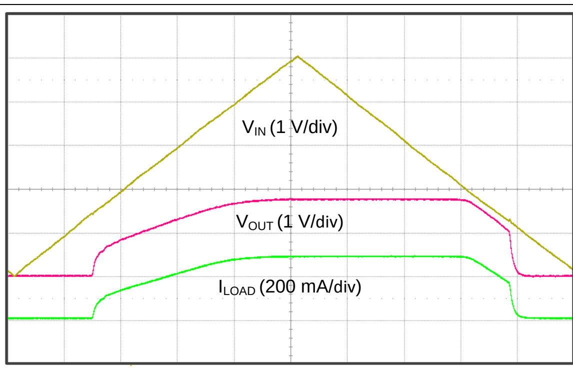
Figure 15. 3.3 V, 50-mA to 300-mA Load Transient



Time (50 µs/div)

V_{IN} = 3.8 V, no output capacitor, output current slew rate = 0.25 A/µs

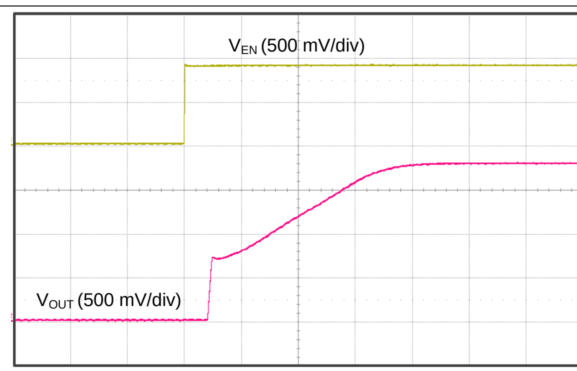
Figure 16. 3.3 V, 50-mA to 300-mA Load Transient



Time (100 µs/div)

R_L = 6.2 Ω, V_{EN} = V_{IN}, 1-µF output capacitor

Figure 17. V_{IN} Power-Up and Power-Down



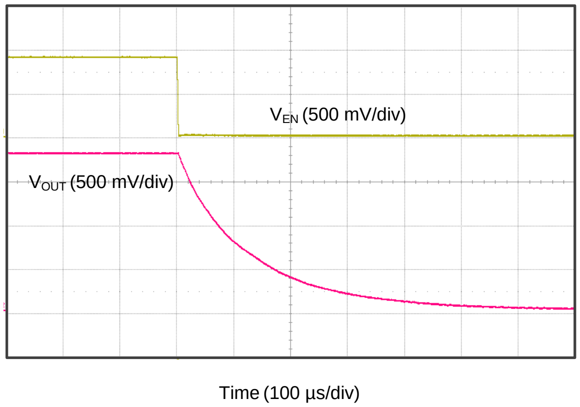
Time (100 µs/div)

R_L = 6.2 Ω, 1-µF output capacitor

Figure 18. Startup with EN

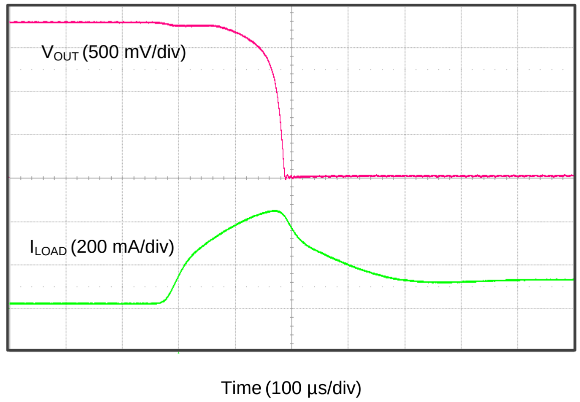
Typical Characteristics (continued)

at operating temperature range (T_J = –40°C to +125°C), V_{IN} = $V_{OUT(nom)}$ + 0.5 V or 2.0 V (whichever is greater), I_{OUT} = 1 mA, V_{EN} = V_{IN}, and C_{IN} = C_{OUT} = 1 µF (unless otherwise noted)



I_{OUT} = 300 mA, 1-µF output capacitor

Figure 19. Shutdown Response with Enable



1-µF output capacitor

Figure 20. Foldback Current Limit Response

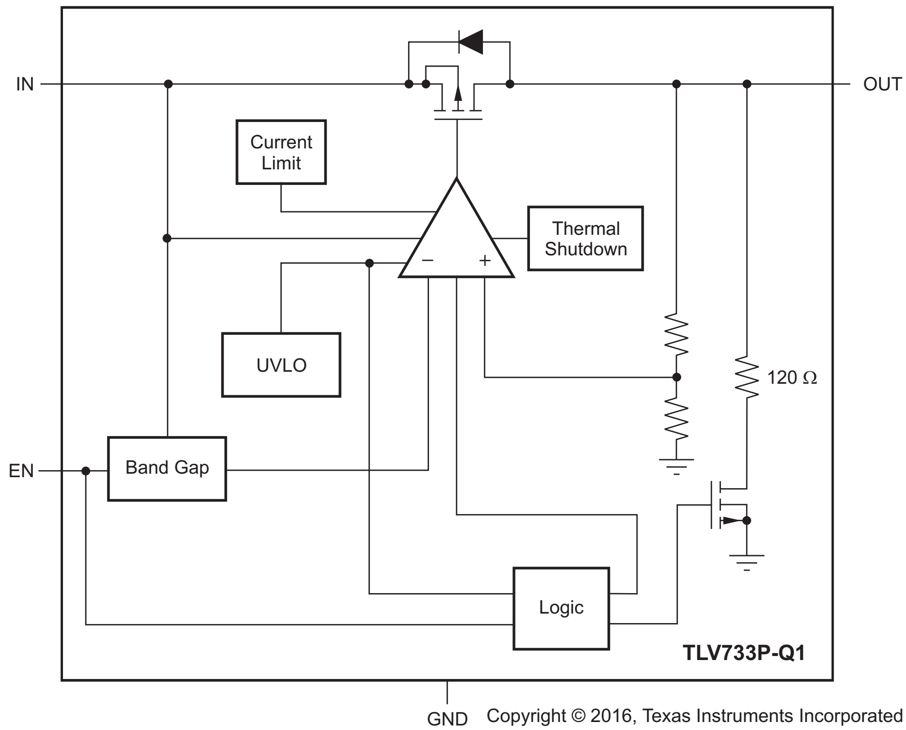
7 Detailed Description

7.1 Overview

The TLV733P-Q1 belongs to a family of low dropout (LDO) linear regulators. These devices consume low quiescent current and deliver excellent line and load transient performance. These characteristics, combined with low noise and good PSRR with low dropout voltage, make this family of devices ideal for portable consumer applications.

This family of regulators offers foldback current limit, shutdown, and thermal protection. The operating junction temperature for this family of devices is –40°C to +135°C.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Undervoltage Lockout (UVLO)

The TLV733P-Q1 family uses an undervoltage lockout (UVLO) circuit that disables the output until the input voltage is greater than the rising UVLO voltage. This circuit ensures that the device does not exhibit any unpredictable behavior when the supply voltage is lower than the operational range of the internal circuitry. During UVLO disable, the output is connected to ground with a 120-Ω pulldown resistor.

7.3.2 Shutdown

The enable pin (EN) is active high. Enable the device by forcing the EN pin to exceed $V_{EN(HI)}$ (0.9 V, minimum). Turn off the device by forcing the EN pin to drop below 0.35 V. If shutdown capability is not required, connect EN to IN.

The TLV733P-Q1 has an internal pulldown MOSFET that connects a 120-Ω resistor to ground when the device is disabled. The discharge time after disabling depends on the output capacitance (C_{OUT}) and the load resistance (R_L) in parallel with the 120-Ω pulldown resistor. The time constant is calculated in Equation 1:

$$\tau = \frac{120 \cdot R_L}{120 + R_L} \cdot C_{OUT} \quad (1)$$

7.3.3 Internal Foldback Current Limit

The TLV733P-Q1 has an internal foldback current limit that protects the regulator during fault conditions. The current allowed through the device is reduced when the output voltage falls. When the output is shorted, the LDO supplies a typical current of 150 mA. The output voltage is not regulated when the device is in current limit. In this condition, the output voltage is the product of the regulated current and the load resistance. When the device output is shorted, the PMOS pass transistor dissipates power [(V_{IN} – V_{OUT}) × I_{OS}] until thermal shutdown is triggered and the device turns off. After the device cools down, the internal thermal shutdown circuit turns the device back on. If the fault condition continues, the device cycles between current limit and thermal shutdown; see the *Thermal Information* table for more details.

The foldback current-limit circuit limits the current allowed through the device to current levels lower than the minimum current limit at a nominal V_{OUT} current limit (I_{LIM}) during startup. See Figure 6 to Figure 8 for typical foldback current limit values. If the output is loaded by a constant-current load during startup, or if the output voltage is negative when the device is enabled, then the load current demanded by the load can exceed the foldback current limit and the device may not rise to the full output voltage. For constant-current loads, disable the output load until the TLV733P-Q1 has fully risen to the nominal output voltage.

The TLV733P-Q1 PMOS pass element has an intrinsic body diode that conducts current when the voltage at the OUT pin exceeds the voltage at the IN pin. Do not force the output voltage to exceed the input voltage because excessively high current can flow through the body diode.

7.3.4 Thermal Shutdown

Thermal shutdown protection disables the output when the junction temperature rises to approximately 160°C. Disabling the device eliminates the power dissipated by the device, allowing the device to cool. When the junction temperature cools to approximately 140°C, the output circuitry is again enabled. Depending on power dissipation, thermal resistance, and ambient temperature, the thermal protection circuit can cycle on and off. This cycling limits regulator dissipation, protecting the device from damage as a result of overheating.

Activating the thermal shutdown feature usually indicates excessive power dissipation as a result of the product of the (V_{IN} – V_{OUT}) voltage and the load current. For reliable operation, limit junction temperature to 135°C (maximum). To estimate the margin of safety in a complete design, increase the ambient temperature until the thermal protection is triggered; use worst-case loads and signal conditions.

The TLV733P-Q1 internal protection circuitry protects against overload conditions but is not intended to be activated in normal operation. Continuously running the TLV733P-Q1 into thermal shutdown degrades device reliability.

7.4 Device Functional Modes

7.4.1 Normal Operation

The device regulates to the nominal output voltage under the following conditions:

- The input voltage has previously exceeded the UVLO rising voltage and has not decreased below the UVLO falling threshold.
- The input voltage is greater than the nominal output voltage added to the dropout voltage.
- The enable voltage has previously exceeded the enable rising threshold voltage and has not decreased below the enable falling threshold.
- The output current is less than the current limit.
- The device junction temperature is less than the thermal shutdown temperature.

7.4.2 Dropout Operation

If the input voltage is lower than the nominal output voltage plus the specified dropout voltage, but all other conditions are met for normal operation, the device operates in dropout mode. In this condition, the output voltage is the same as the input voltage minus the dropout voltage. The transient performance of the device is significantly degraded because the pass device is in a triode state and no longer controls the current through the LDO. Line or load transients in dropout can result in large output voltage deviations.

7.4.3 Disabled

The device is disabled under the following conditions:

- The input voltage is less than the UVLO falling voltage, or has not yet exceeded the UVLO rising threshold.
- The enable voltage is less than the enable falling threshold voltage or has not yet exceeded the enable rising threshold.
- The device junction temperature is greater than the thermal shutdown temperature.

When the device is disabled, the active pulldown resistor discharges the output.

Table 1 shows the conditions that lead to the different modes of operation.

Table 1. Device Functional Mode Comparison

OPERATING MODE	PARAMETER			
	V_{IN}	V_{EN}	I_{OUT}	T_J
Normal mode	$V_{IN} > V_{OUT(nom)} + V_{DO}$ and $V_{IN} > UVLO_{RISE}$	$V_{EN} > V_{EN(HI)}$	$I_{OUT} < I_{LIM}$	$T_J < 160°C$
Dropout mode	$UVLO_{RISE} < V_{IN} < V_{OUT(nom)} + V_{DO}$	$V_{EN} > V_{EN(HI)}$	$I_{OUT} < I_{LIM}$	$T_J < 160°C$
Disabled mode (any true condition disables the device)	$V_{IN} < UVLO_{FALL}$	$V_{EN} < V_{EN(LO)}$	—	$T_J > 160°C$

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

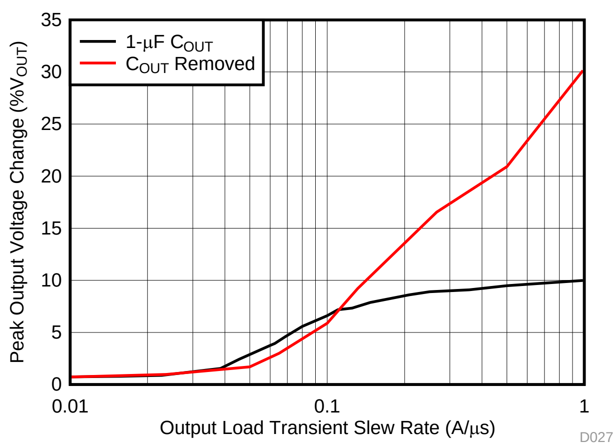
8.1 Application Information

8.1.1 Input and Output Capacitor Selection

The TLV733P-Q1 uses an advanced internal control loop to obtain stable operation both with and without the use of input or output capacitors. Dynamic performance is improved with the use of an output capacitor, and can be improved with an input capacitor. An output capacitance of 0.1 µF or larger generally provides good dynamic response. Use X5R- and X7R-type ceramic capacitors because these capacitors have minimal variation in value and equivalent series resistance (ESR) over temperature.

Although an input capacitor is not required for stability, increased output impedance from the input supply can compromise the performance of the TLV733P-Q1. Good analog design practice is to connect a 0.1-µF to 1-µF capacitor from IN to GND. This capacitor counteracts reactive input sources and improves transient response, input ripple, and PSRR. Use an input capacitor if the source impedance is greater than 0.5 Ω. Use a higher-value capacitor if large, fast rise-time load transients are anticipated, or if the device is located several inches from the input power source.

Figure 21 shows the transient performance improvements with an external 1-µF capacitor on the output versus no output capacitor. The data in this figure are taken with an increasing load step from 50 mA to 300 mA, and the peak output voltage deviation (load transient response) is measured. For low output current slew rates, (< 0.1 A/µs), the transient performance of the device is similar with or without an output capacitor. When the current slew rate is increased, the peak voltage deviation is significantly increased. For loads that exhibit fast current slew rates above 0.1 A/µs, use an output capacitor. For best performance, the maximum recommended output capacitance is 100 µF.



Output current stepped from 50 mA to 300 mA, output voltage change measured at positive dI/dt

Figure 21. Output Voltage Deviation vs Load Step Slew Rate

Some applications benefit from the removal of the output capacitor. In addition to space and cost savings, the removal of the output capacitor lowers inrush current as a result of eliminating the required current flow into the output capacitor at startup. In these cases, take care to ensure that the load is tolerant of the additional output voltage deviations.

Application Information (continued)

8.1.2 Dropout Voltage

The TLV733P-Q1 uses a PMOS pass transistor to achieve low dropout. When (V_{IN} – V_{OUT}) is less than the dropout voltage (V_{DO}), the PMOS pass device is in the linear region of operation and the input-to-output resistance is the $R_{DS(ON)}$ of the PMOS pass element. V_{DO} scales approximately with output current because the PMOS device behaves like a resistor in dropout mode. As with any linear regulator, PSRR and transient response degrade when (V_{IN} – V_{OUT}) approaches dropout operation.

8.2 Typical Applications

8.2.1 DC-DC Converter Post Regulation

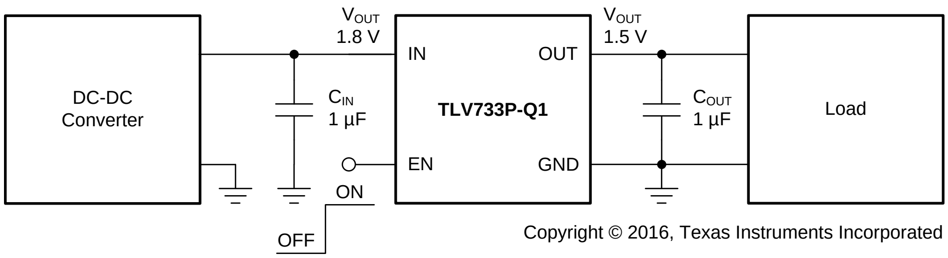


Figure 22. DC-DC Converter Post Regulation

8.2.1.1 Design Requirements

Table 2. Design Parameters

PARAMETER	DESIGN REQUIREMENT
Input voltage	1.8 V, ±5%
Output voltage	1.5 V, ±1%
Output current	200-mA dc, 300-mA peak
Output voltage transient deviation	< 10%, 1-A/µs load step from 50 mA to 200 mA
Maximum ambient temperature	85°C

8.2.1.2 Design Considerations

The TLV733P-Q1 can provide post regulation after a dc-dc converter, as shown in Figure 22. For this application, input and output capacitors are required to achieve the output voltage transient requirements. Capacitance values of 1 µF are selected to give the maximum output capacitance in a small, low-cost package.

8.2.1.3 Application Curve

Figure 23 shows the TLV733P-Q1 startup, regulation, and shutdown as specified in Figure 22.

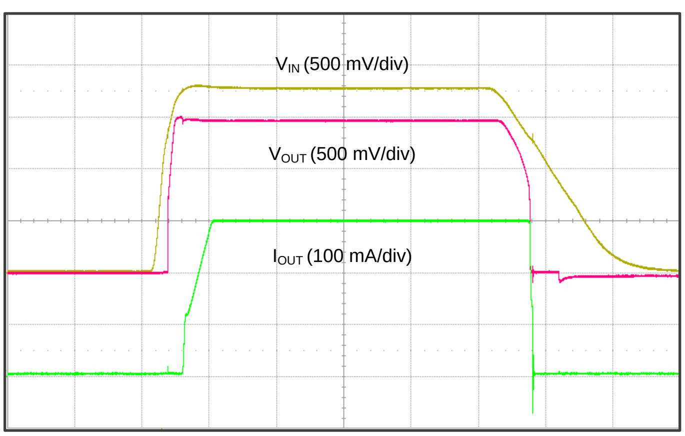


Figure 23. 1.8-V to 1.5-V Regulation at 300 mA

8.2.2 Capacitor-Free Operation from a Battery Input Supply

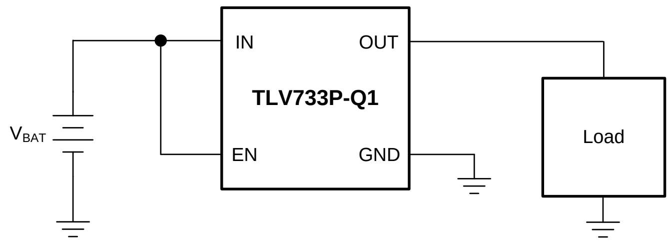


Figure 24. Capacitor-Free Operation from a Battery Input Supply

8.2.2.1 Design Requirements

Table 3. Design Parameters

PARAMETER	DESIGN REQUIREMENT
Input voltage	3.0 V to 1.8 V (two 1.5-V batteries)
Output voltage	1.0 V, ±1%
Input current	200 mA, maximum
Output load	100-mA dc
Maximum ambient temperature	70°C

8.2.2.2 Design Considerations

The TLV733P-Q1 can be directly powered off of a battery, as shown in Figure 24. An input capacitor is not required for this design because of the direct low impedance connection to the battery.

Eliminating the output capacitor allows for the minimal possible inrush current during startup, ensuring that the 200-mA maximum input current is not exceeded.

8.2.2.3 Application Curve

Figure 25 shows no inrush with the capacitor-free startup.

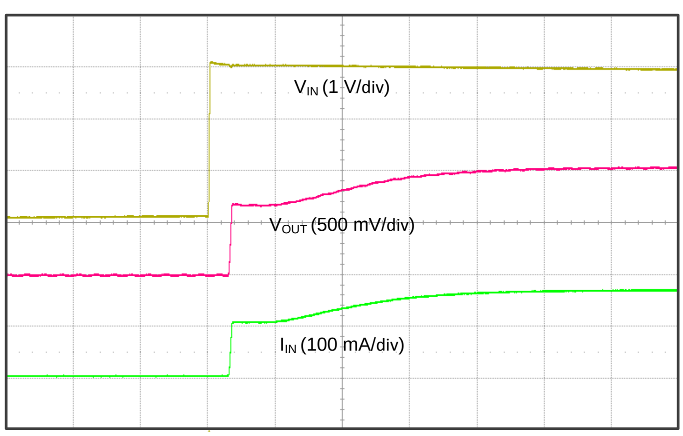


Figure 25. No Inrush Startup, 3.0-V to 1.0-V Regulation

9 Power-Supply Recommendations

Connect a low output impedance power supply directly to the IN pin of the TLV733P-Q1. Inductive impedances between the input supply and the IN pin can create significant voltage excursions at the IN pin during startup or load transient events. If inductive impedances are unavoidable, use an input capacitor.

10 Layout

10.1 Layout Guidelines

- Place input and output capacitors as close to the device as possible.
- Use copper planes for device connections, in order to optimize thermal performance.
- Place thermal vias around the device to distribute the heat.

Figure 26 shows an example of how the TLV733P-Q1 is laid out on a printed circuit board (PCB).

10.2 Layout Example

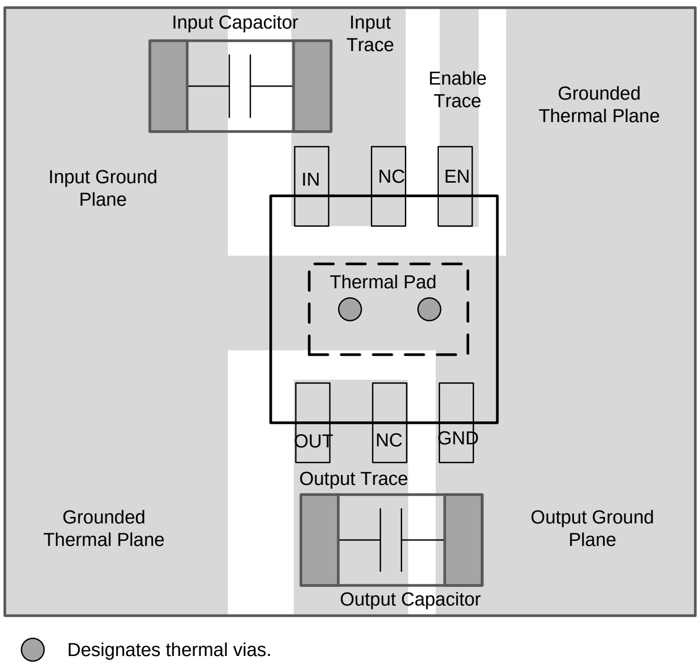


Figure 26. WSON Layout Example

11 Device and Documentation Support

11.1 Device Support

11.1.1 Development Support

11.1.1.1 Evaluation Module

An evaluation module (EVM) is available to assist in the initial circuit performance evaluation using the TLV733P-Q1. The TLV73312PEVM-643 evaluation module (and related user guide) can be requested at the Texas Instruments website through the product folders or purchased directly from the TI eStore.

11.1.2 Device Nomenclature

Table 4. Device Nomenclature(1)(2)

PRODUCT	V_{OUT}
TLV733P-Q1**xx(x)Pyyyz**Q1	**xx(x)** is the nominal output voltage. For output voltages with a resolution of 100 mV, two digits are used in the ordering number; otherwise, three digits are used (for example, 28 = 2.8 V; 125 = 1.25 V). **P** indicates an active output discharge feature. All members of the TLV733P-Q1 family will actively discharge the output when the device is disabled. **yyy** is the package designator. **z** is the package quantity. R is for reel (3000 pieces), T is for tape (250 pieces).

(1) For the most current package and ordering information see the Package Option Addendum at the end of this document, or visit the device product folder on www.ti.com.
(2) Output voltages from 1.0 V to 3.3 V in 50-mV increments are available. Contact the factory for details and availability.

11.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.4 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

11.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TLV73310PQDRVRQ1	ACTIVE	WSON	DRV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	12P	Samples
TLV73311PQDRVRQ1	ACTIVE	WSON	DRV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	12Q	Samples
TLV73312PQDRVRQ1	ACTIVE	WSON	DRV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	12R	Samples
TLV73315PQDRVRQ1	ACTIVE	WSON	DRV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	12S	Samples
TLV73318PQDRVRQ1	ACTIVE	WSON	DRV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	12T	Samples
TLV73325PQDRVRQ1	ACTIVE	WSON	DRV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	12U	Samples
TLV73328PQDRVRQ1	ACTIVE	WSON	DRV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	12V	Samples
TLV73333PQDRVRQ1	ACTIVE	WSON	DRV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	12W	Samples

[1] The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

[2] Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

[3] MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF TLV733P-Q1 :

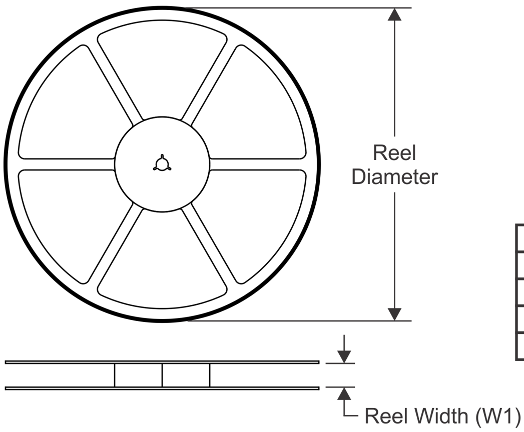
- Catalog: TLV733P

NOTE: Qualified Version Definitions:

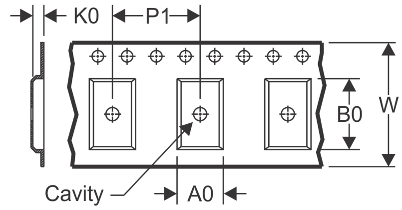
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

REEL DIMENSIONS

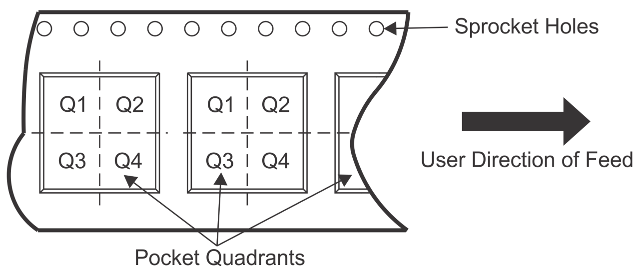


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

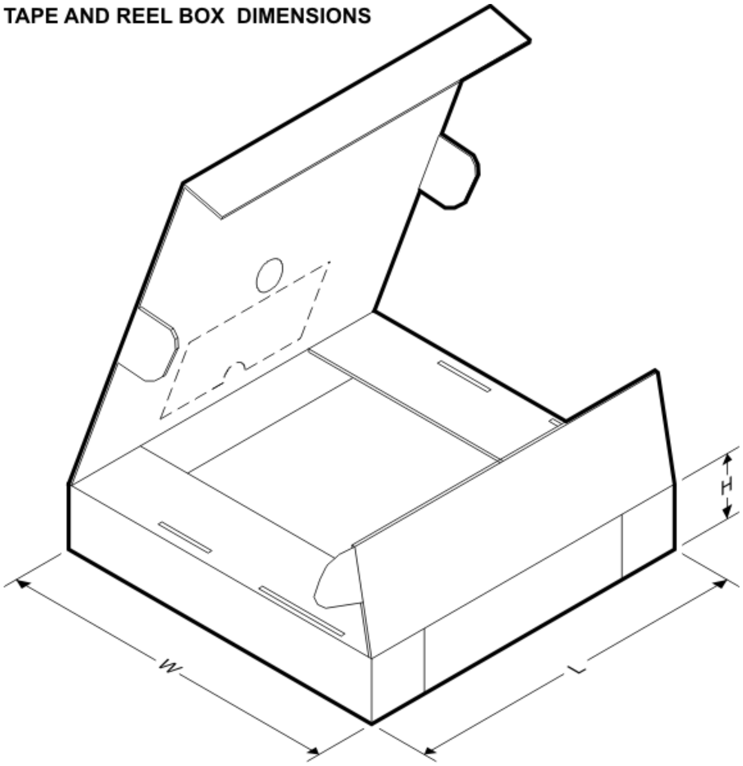
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLV73310PQDRVRQ1	WSON	DRV	6	3000	179.0	8.4	2.2	2.2	1.2	4.0	8.0	Q2
TLV73311PQDRVRQ1	WSON	DRV	6	3000	179.0	8.4	2.2	2.2	1.2	4.0	8.0	Q2
TLV73312PQDRVRQ1	WSON	DRV	6	3000	179.0	8.4	2.2	2.2	1.2	4.0	8.0	Q2
TLV73315PQDRVRQ1	WSON	DRV	6	3000	179.0	8.4	2.2	2.2	1.2	4.0	8.0	Q2
TLV73318PQDRVRQ1	WSON	DRV	6	3000	179.0	8.4	2.2	2.2	1.2	4.0	8.0	Q2
TLV73325PQDRVRQ1	WSON	DRV	6	3000	179.0	8.4	2.2	2.2	1.2	4.0	8.0	Q2
TLV73328PQDRVRQ1	WSON	DRV	6	3000	179.0	8.4	2.2	2.2	1.2	4.0	8.0	Q2
TLV73333PQDRVRQ1	WSON	DRV	6	3000	179.0	8.4	2.2	2.2	1.2	4.0	8.0	Q2

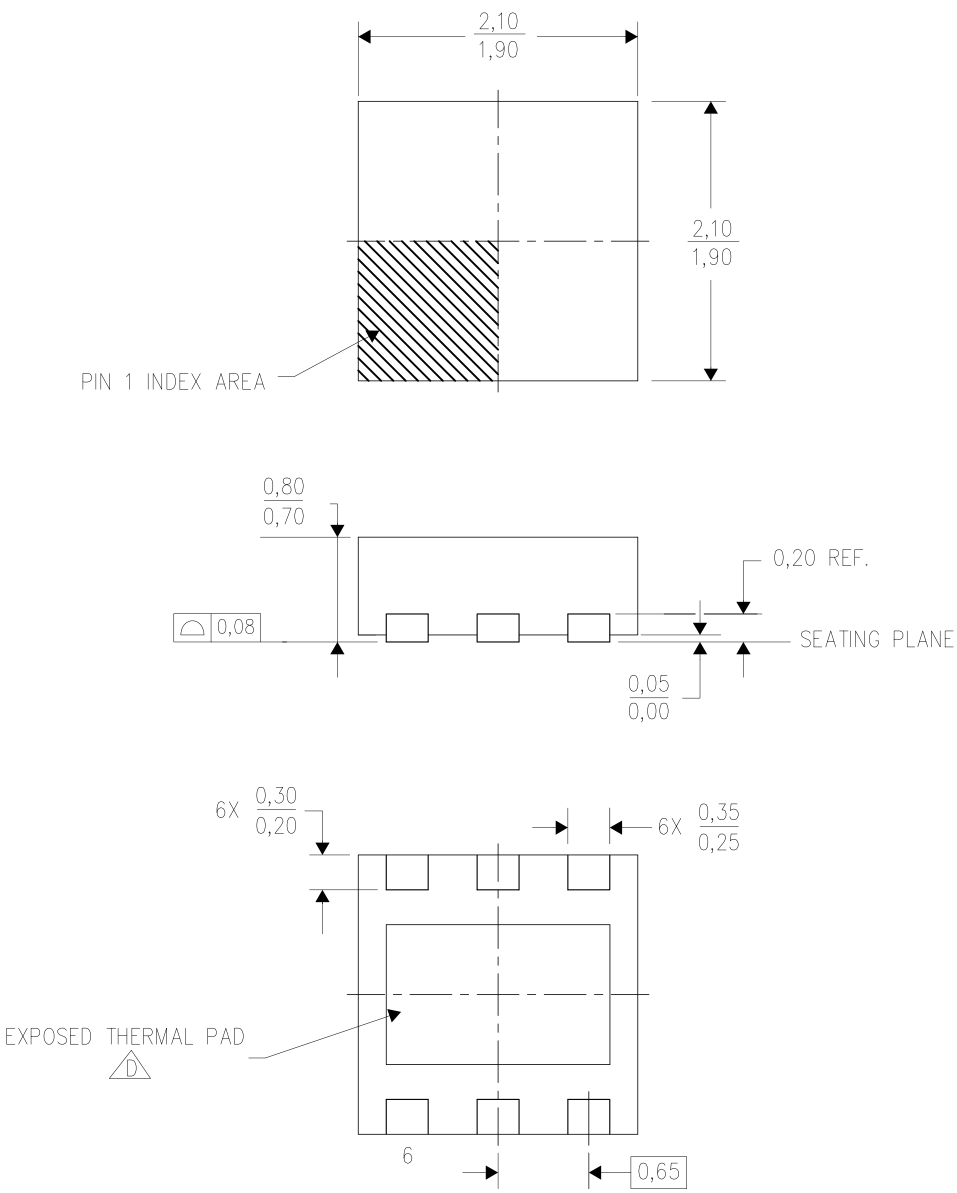
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLV73310PQDRVRQ1	WSON	DRV	6	3000	203.0	203.0	35.0
TLV73311PQDRVRQ1	WSON	DRV	6	3000	203.0	203.0	35.0
TLV73312PQDRVRQ1	WSON	DRV	6	3000	203.0	203.0	35.0
TLV73315PQDRVRQ1	WSON	DRV	6	3000	203.0	203.0	35.0
TLV73318PQDRVRQ1	WSON	DRV	6	3000	203.0	203.0	35.0
TLV73325PQDRVRQ1	WSON	DRV	6	3000	203.0	203.0	35.0
TLV73328PQDRVRQ1	WSON	DRV	6	3000	203.0	203.0	35.0
TLV73333PQDRVRQ1	WSON	DRV	6	3000	203.0	203.0	35.0

DRV (S-PWSON-N6) PLASTIC SMALL OUTLINE NO-LEAD



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NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
B. This drawing is subject to change without notice.
C. Small Outline No-Lead (SON) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.

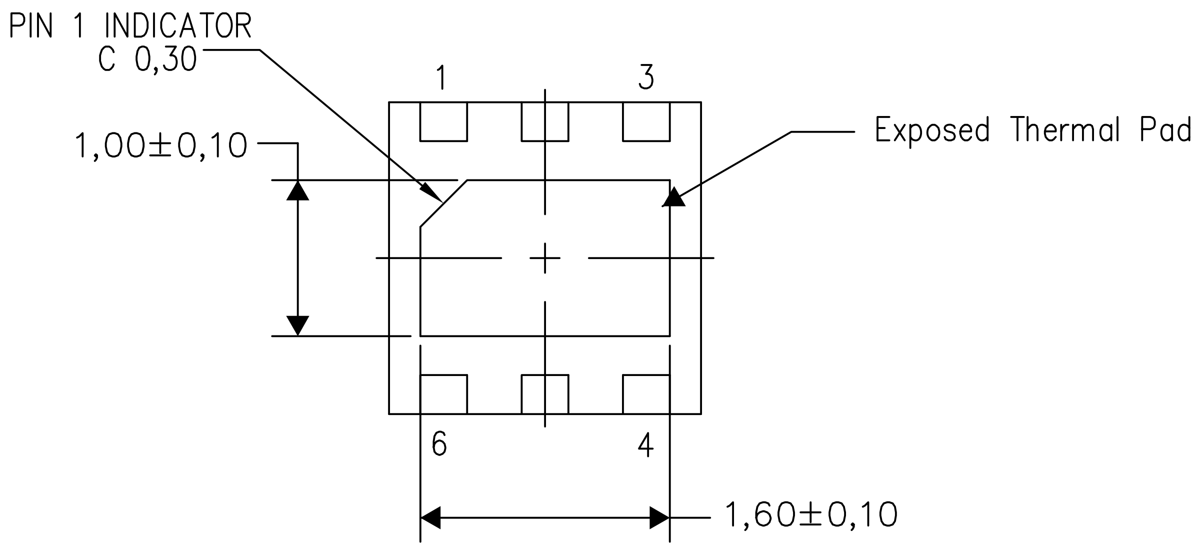
DRV (S-PWSON-N6) PLASTIC SMALL OUTLINE NO-LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Bottom View

Exposed Thermal Pad Dimensions

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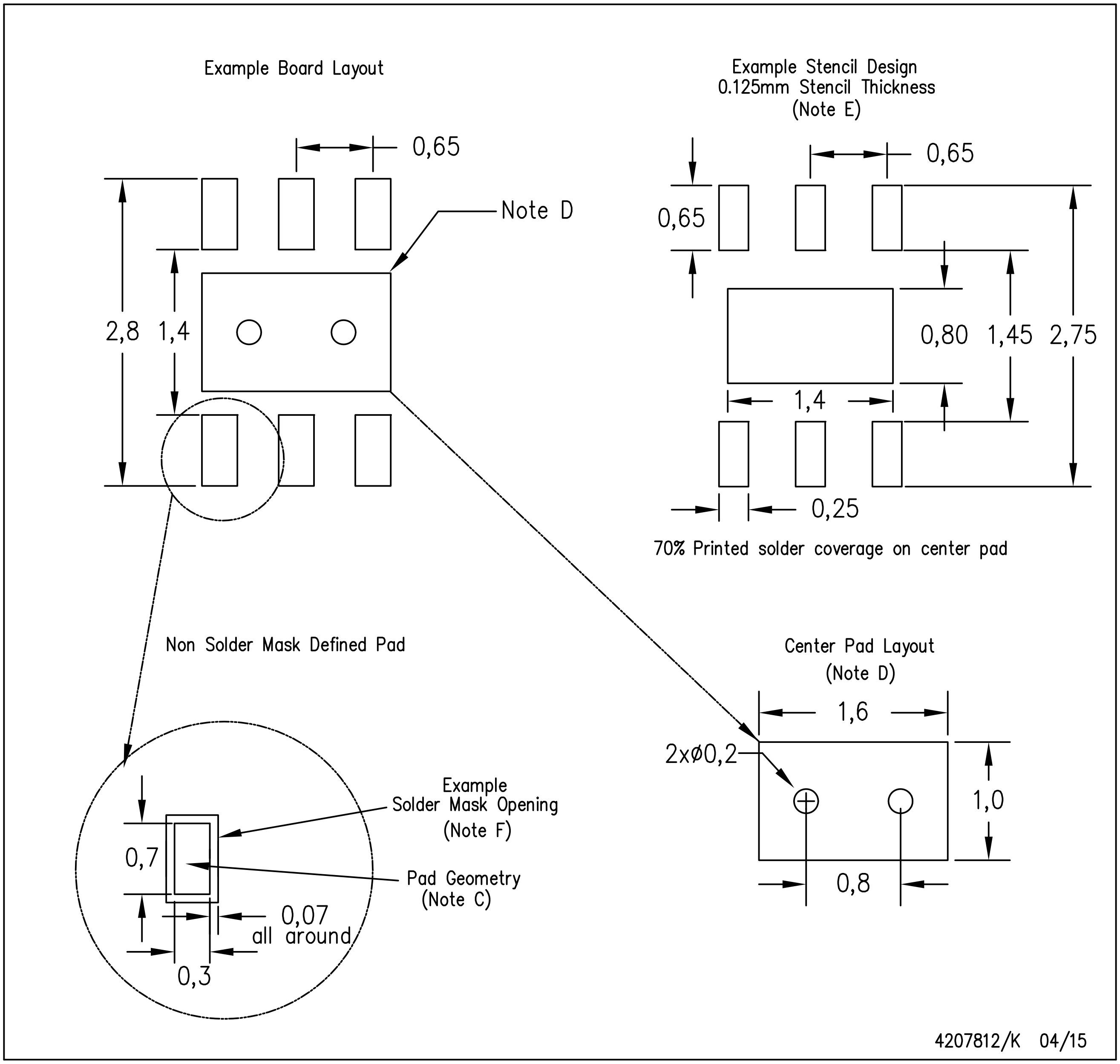
NOTE: All linear dimensions are in millimeters

DRV (S–PWSON–N6) PLASTIC SMALL OUTLINE NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for solder mask tolerances.

IMPORTANT NOTICE

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265