TS3A5223 0.45Ω 双通道 SPDT 双向模拟开关

1 特性

- 低导通电阻开关
  - 电压为 3.6V 时为 0.45Ω（典型值）
  - 电压为 1.8V 时为 0.85Ω（典型值）
- 宽电源电压：1.65V 至 3.6V
- 1.0V 兼容逻辑接口
- 高切换带宽 80MHz
- 在整个波段上，总谐波失真 (THD) 为 0.01%
- 额定最小先开后合
- 双向切换
- –75dB 通道至通道串扰
- 具有极低功率耗散和泄漏电流的 -70dB 通道至通道关闭隔离
- 极小型 QFN-10 封装：1.8mm x 1.4mm
- 针对所有引脚的 ESD 保护
  - 2kV HBM，500V CDM

2 应用

- 便携式电子产品
- 智能手机、平板电脑
- 家用电器
- 有线通信

3 说明

TS3A5223 是一款高速双通道模拟开关，此开关具有先断后通以及双向信号切换功能。TS3A5223 可被用作一个双路 2:1 复用器或者一个 1:2 双路去复用器。

TS3A5223 提供极低的导通电阻、很低的 THD 和通道间串扰以及很高的关闭隔离。这些 特性 使得 TS3A5223 适用于音频信号传输和切换 应用。

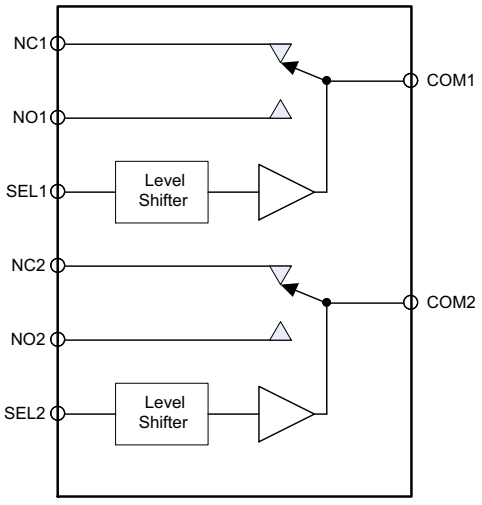
TS3A5223 控制逻辑支持 1V - 3.6V CMOS 逻辑电平。此逻辑接口可在不增加电源输出电流 (I_{CC}) 的前提下实现与各种 CPU 和微控制器的直接对接，从而降低了功耗。

器件信息(1)

器件型号	封装	封装尺寸（标称值）
TS3A5223	µQFN (10)	1.80mm x 1.40mm

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。

功能图



目录

4 修订历史记录

注：之前版本的页码可能与当前版本有所不同。

Changes from Revision A (February 2013) to Revision B **Page**

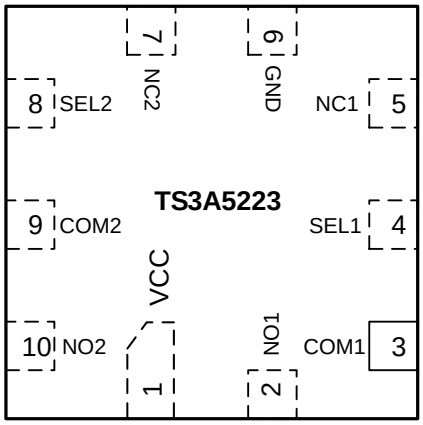
- 添加了*器件信息* 表、*ESD 额定值* 表、*热性能信息* 表、*特性* *说明* 部分、*器件功能模式*、*应用和实施* 部分、*电源建议* 部分、*布局* 部分、*器件和文档支持* 部分以及*机械、封装和可订购信息* 部分 ... 1
- Changed the V_{Max} MAX value From: 3.6 V To: V_{CC} in the *Recommended Operating Conditions* table ... 4
- Deleted: "dt/dv, SEL pin Input rise and fall time limit" from the *Recommended Operating Conditions* table ... 4
- Deleted the Dissipation Ratings table ... 4

Changes from Original (January 2013) to Revision A **Page**

- 将器件状态从“预览”更改为“生产” ... 1

5 Pin Configuration and Functions

RSW Package
10 Pin UQFN
Top View



Pin Functions

NAME	PIN NUMBER	DESCRIPTION
VCC	1	Positive supply Input – Connect 1.65 V to 3.6 V supply voltage
NC1	5	Signal path Input/Output signal pins
NO1	2	
NC2	7	
NO2	10	
COM1, COM2	3, 9	Common signal path Input/Output signal pins
GND	6	Ground reference pin
SEL1, SEL2	4, 8	Select digital logic pin. Logic low connects COM to NC, Logic high connects COM to NO

6 Specifications

6.1 Absolute Maximum Ratings(1)

Specified at T_A= –40°C to 85°C unless otherwise noted.

			VALUE		UNIT
			MIN	MAX	
VCC	Positive DC supply voltage		–0.3	4.3(2)	V
V_{COM} V_{NO} V_{NC}	Analog voltage		–0.3	4.3(2)	V
I_{COM} I_{NO} I_{NC}	On-state switch continuous current			±300	mA
I_{COM} I_{NO} I_{NC}	On-state switch peak current (1ms pulse at 10% duty cycle)			±500	mA
P_D	Total device power dissipation at T_A = 85°C	10-µQFN RSW		430	mW
T_A	Operating free-air ambient temperature range		–40	85	°C
T_J	Junction temperature range		–55	150	°C
T_{stg}	Storage temperature range		–55	150	°C

(1) Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Not rated for continuous operation, 0.5% duty cycle at 1 kHz recommended

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_{CC}	Positive DC supply voltage	1.65	3.6	V
V_{COM}, V_{NO}, V_{NC}	Analog voltage range	0	V_{CC}	V
V_{SEL1} V_{SEL2}	Digital logic voltage	0	V_{CC}	V
T_A	Operating free-air ambient temperature range	–40	85	ºC

6.4 Thermal Information

THERMAL METRIC(1)		TS3A5223 RSW (UQFN) 10 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	92.5	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	46.0	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	44.5	°C/W
ψ_{JT}	Junction-to-top characterization parameter	1.5	°C/W
ψ_{JB}	Junction-to-board characterization parameter	44.5	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	31.2	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

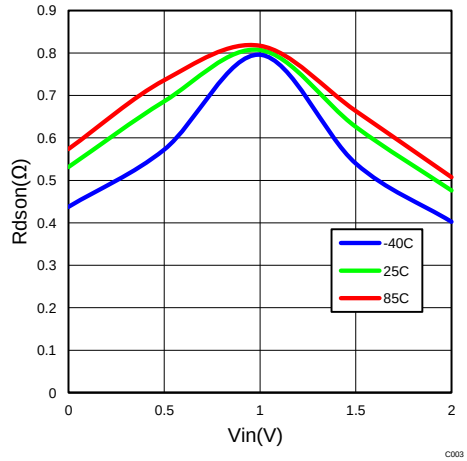
6.5 Electrical Characteristics

Specified over the recommended junction temperature range $T_A = T_J = –40°C$ to 85°C Typical values are at $T_A = T_J = 25°C$ (unless otherwise noted).

PARAMETER		V_{CC} (V)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
DC CHARACTERISTICS							
V_{IH}	High-level Input voltage SEL1, SEL2 inputs	3.6		0.8			V
		2.3		0.8			
		1.8		0.8			
V_{IL}	Low-level Input voltage SEL1, SEL2 inputs	3.6				0.3	V
		2.3				0.3	
		1.8				0.3	
R_{ON}	Switch ON Resistance	3.6	V_S = 0 to V_{CC}, I_S = 100 mA, V_{SEL} = 1 V, 0 V		0.45	0.6	Ω
		2.3			0.6	0.8	
		1.8			0.85	1.2	
ΔR_{ON}	Difference of on-state resistance between switches	3.6	V_S = 2 V, 0.8 V, IS = 100 mA, V_{SEL} = 1 V, 0 V		0.05		Ω
$R_{ON-FLAT}$	ON resistance flatness	3.6	V_S = 0 to V_{CC}, IS = 100mA, V_{SEL} = 1 V, 0 V		0.1	0.2	Ω
		2.3			0.15	0.35	
		1.8			0.4	0.65	
I_{OFF}	NC, NO pin leakage current when switch is off	3.6	V_S = 0.3 or 3.0V, V_{COM} = 3 or 0.3 V		5	90	nA
$I_{S(ON)}$	NC, NO pin leakage current when switch is on	3.6	V_S = 0.3 or 3.0V, V_{COM} = No Load		4	60	nA
I_{SEL}	Select pin input leakage current	V_S	V_S = 0 or 3.6 V			100	nA
I_{CC}	Quiescent supply current	3.6	V_{SEL} = 0 or V_{CC}		700	2000	nA
I_{CCLV}	Supply current change	3.6	V_{SEL} = 1 V to V_{SEL} = V_{CC}			200	nA
SWITCHING PARAMETERS(1)(2)							
t_{PHL}	Logic high to low propagation delay	3.6	R_L = 50 Ω, C_L = 35 pF		0.1		ns
		2.5			0.2		
		1.8			0.2		
t_{PLH}	Logic low to high propagation delay	3.6	R_L = 50 Ω, C_L = 35 pF		0.1		ns
		2.5			0.2		
		1.8			0.2		
t_{ON}	Turn-ON time	2.3 - 3.6	R_L = 50 Ω, C_L = 35 pF, V_S = 1.5 V			70	ns
t_{OFF}	Turn-OFF time	2.3 - 3.6	R_L = 50 Ω, C_L = 35 pF, V_S = 1.5 V			75	ns
t_{BBM}	Break-before-make time delay	3.6	R_L = 50 Ω, C_L = 35 pF, V_S = 1.5 V	2	8		ns
Q_{INJ}	Charge Injection	3.6	C_L = 1 nF, V_S = 0 V		40		pC
AC CHARACTERISTICS							
BW	-3 dB Bandwidth	1.65 - 3.6	R_L = 50 Ω, C_L = 35 pF		80		MHz
V_{ISO}	Channel OFF isolation	1.65 - 3.6	V_S = 1 Vrms, f = 100 kHz		–70		dB
V_{Xtalk}	Channel-to-Channel Crosstalk	1.65 - 3.6	V_S = 1 Vrms, f = 100kHz		–75		dB
THD	Total harmonic distortion	1.65 - 3.6	R_L = 600 Ω, V_{SEL} = 2 Vpk-pk, f = 20 Hz to 20 kHz		0.01%		
C_{SEL}	Select pin input capacitance	3.3	f = 1 MHz		3		pF
C_{ON}	NC, NO, and COM input capacitance when switch is on	3.3	f = 1 MHz		115		pF
C_{OFF}	NC, NO, and COM input capacitance when switch is off	3.3	f = 1 MHz		50		pF

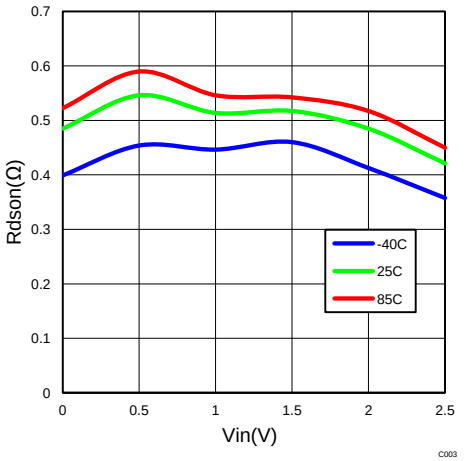
(1) Rise and Fall propagation delays, t_{PHL} and t_{PLH}, are measured between 50% values of the input and the corresponding output signal amplitude transition.
(2) Specified by characterization only. Validated during qualification. Not measured in production testing.

6.6 Typical Characteristics



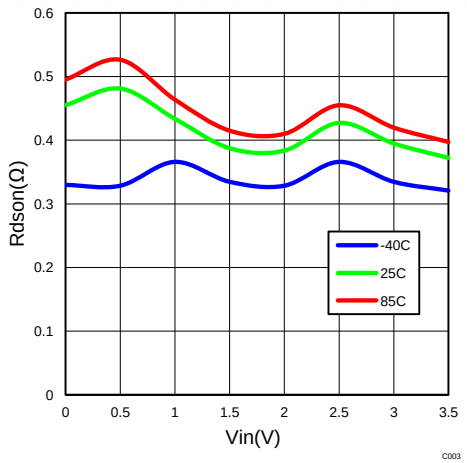
V_{CC} = 1.8 V

Figure 1. On-Resistance vs Switch Input Voltage



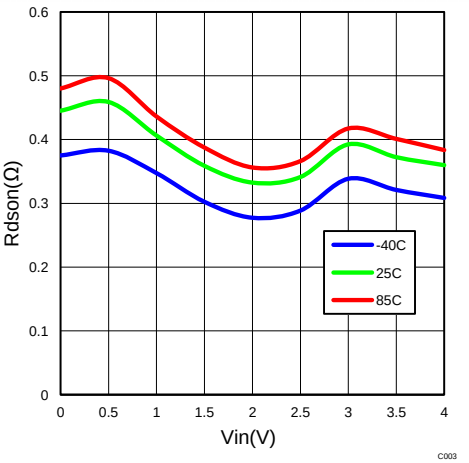
V_{CC} = 2.3 V

Figure 2. On-Resistance vs Switch Input Voltage



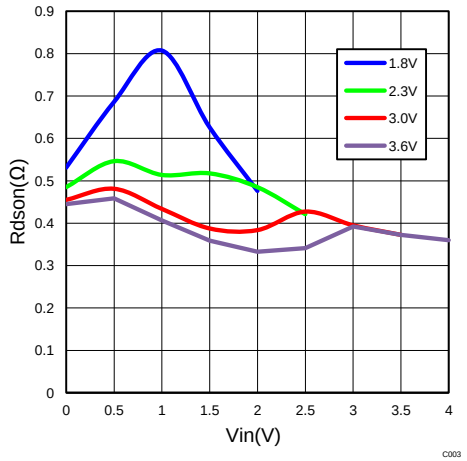
V_{CC} = 3 V

Figure 3. On-Resistance vs Switch Input Voltage



V_{CC} = 3.6 V

Figure 4. On-Resistance vs. Switch Input Voltage



T_A = 25°C

Figure 5. On-Resistance vs. Switch Input Voltage

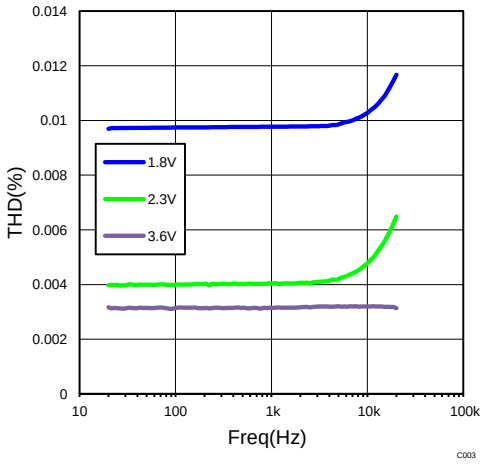


Figure 6. Total Harmonic Distortion

7 Parameter Measurement Information

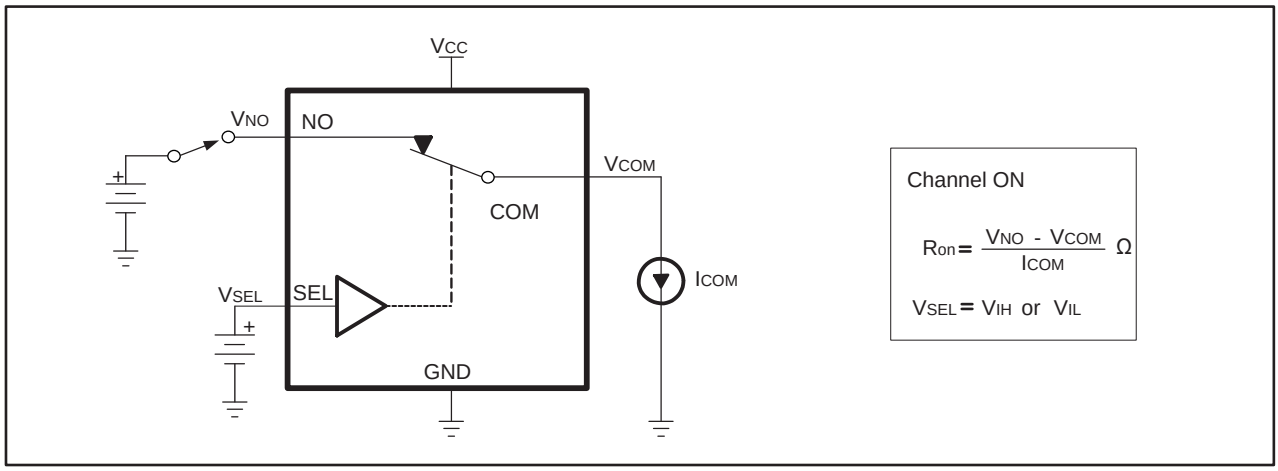


Figure 7. ON-State Resistance (R_{ON})

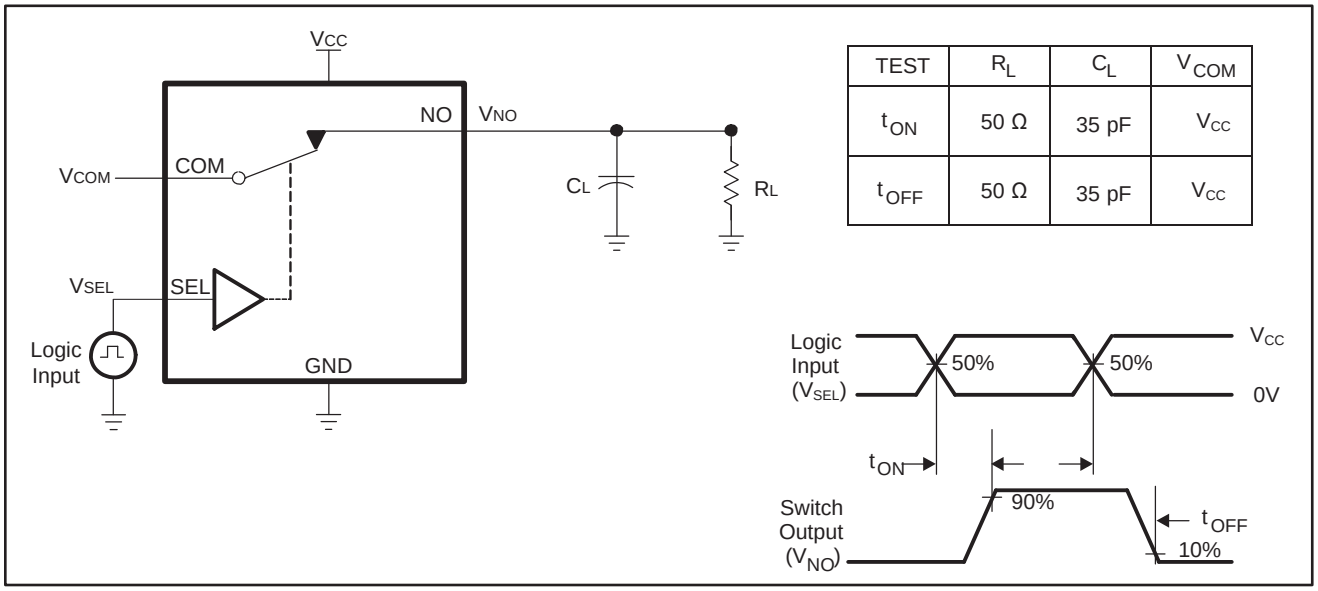


Figure 8. Turn-On (t_{ON}) and Turn-Off Time (t_{OFF})

Parameter Measurement Information (continued)

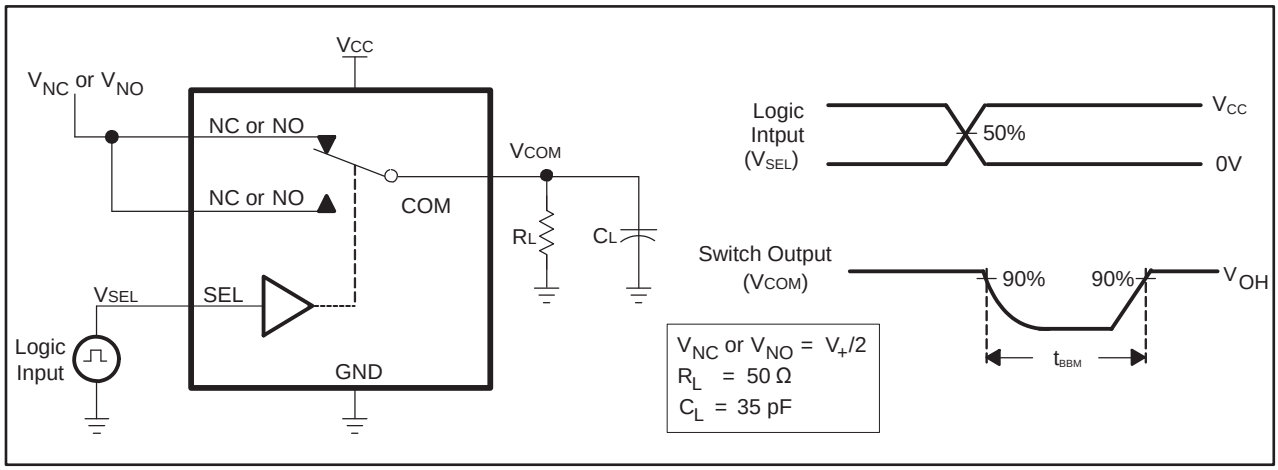


Figure 9. Break-Before-Make Time (t_{BBM})

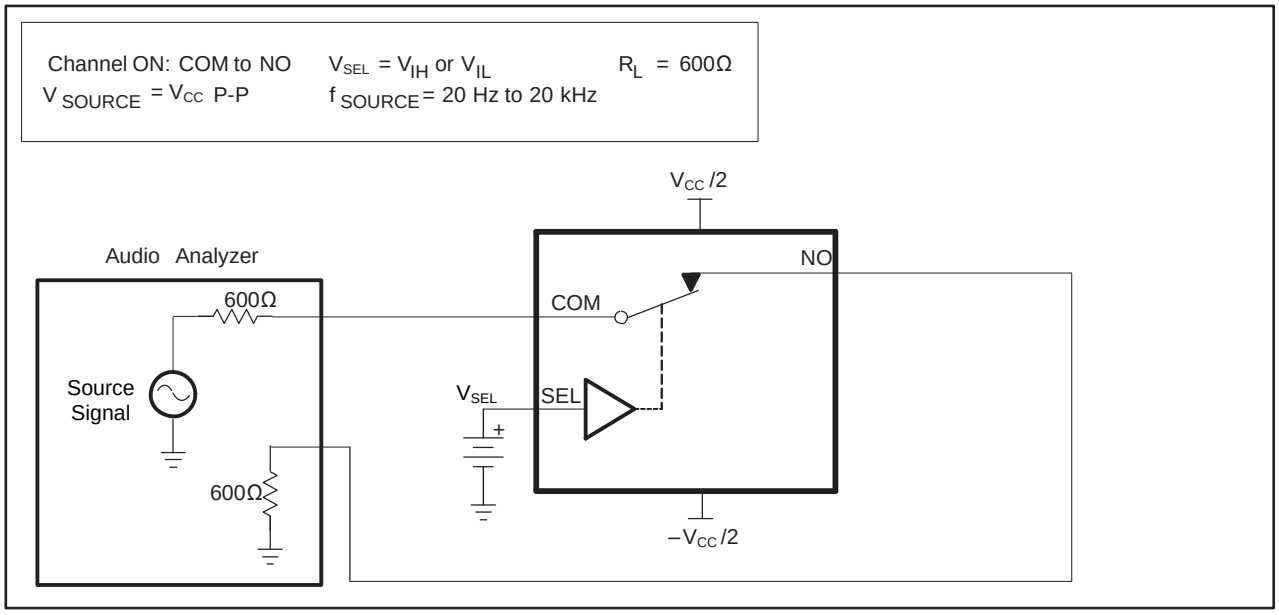


Figure 10. TOTAL HARMONIC DISTORTION (THD)

Parameter Measurement Information (continued)

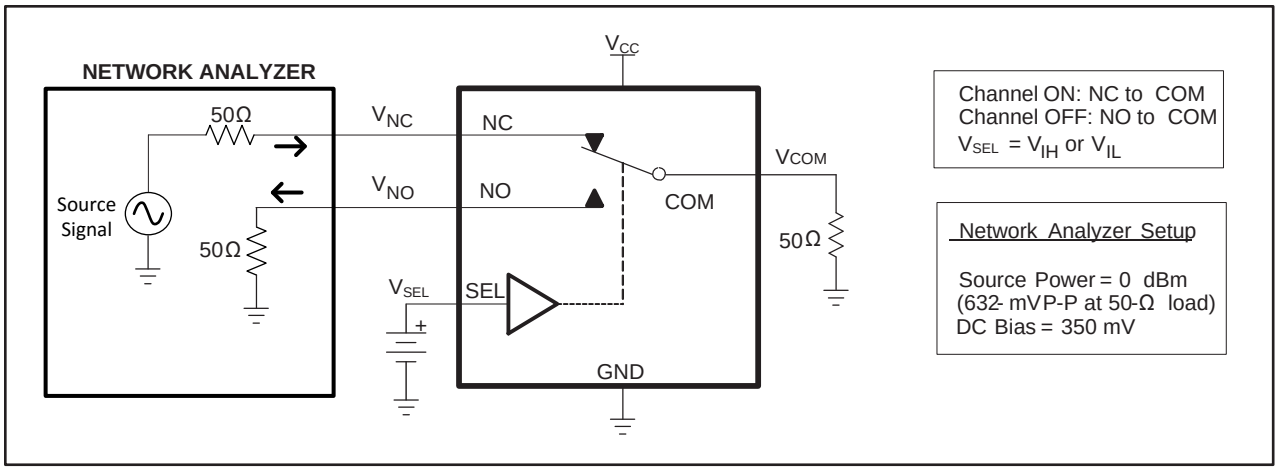


Figure 11. Crosstalk (X_{TALK})

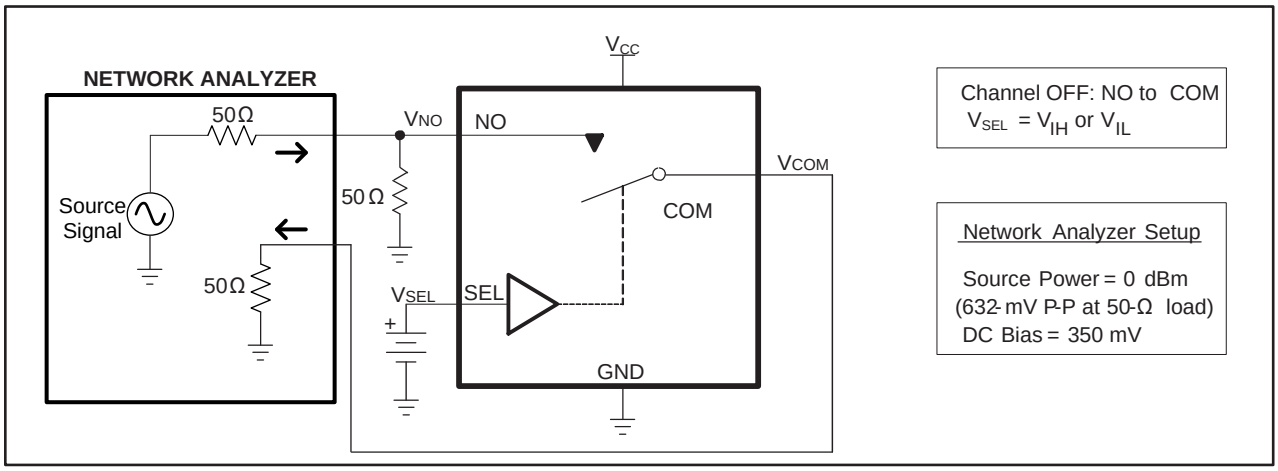


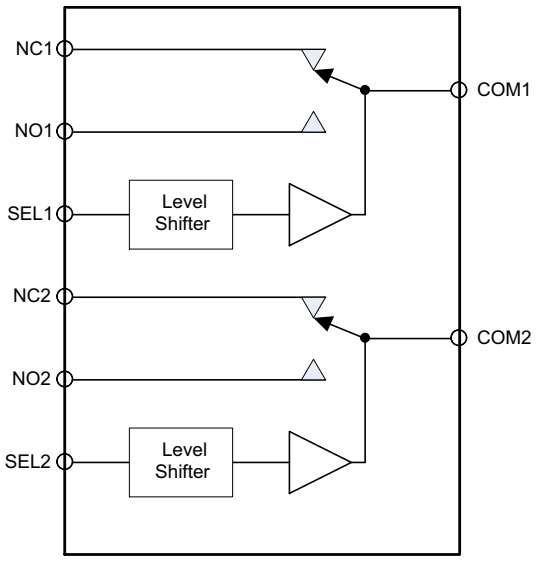
Figure 12. OFF Isolation (O_{ISO})

8 Detailed Description

8.1 Overview

The TS3A5223 is a bidirectional, 2-channel, single-pole double-throw (2:1 SPDT) analog switch that is designed to operate from 1.65 V to 3.6 V. This switch solution comes in a small 1.4mm x 1.8 mm QFN package while maintaining excellent signal integrity, which makes the TS3A5223 suitable for a wide range of applications in personal electronics, portable instrumentation, and test and home electronics. The device maintains the signal integrity by its low ON-state resistance, excellent ON-state resistance matching, and total harmonic distortion (THD) performance. To prevent signal distortion during the transferring of a signal from one channel to another, the TS3A5223 device also has a specified break-before-make feature.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Digital Logic Translation

The TS3A5223 devices supports down to 1-V logic signals irrespective of the supply voltage. The device accomplishes this with integrated level shifters on the digital input SEL1 and SEL2 pis.

8.3.2 Break-Before-Make

The TS3A5223 devices prevents signal distortions when switching signals between the NO and NC pins by completely turning off one signal path before turning on the other signal path. The break-before-make timing specifications are found in the *Electrical Characteristics* table.

8.4 Device Functional Modes

Logic low voltage on SEL1 or SEL2 pins connect the COM pin to NC pin.

Logic high voltage on SEL1 or SEL2 pins connect the COM pin to NO pin.

Table 1. TS3A5223 Function Table

SEL1	SEL2	COM1	COM2
0	0	NC1	NC2
1	1	NO1	NO2
1	0	NO1	NC2
0	1	NC1	NO2

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The TS3A5223 switch is bidirectional, so the NO, NC and COM pins can be used as either inputs or outputs. This switch is typically used when there is only one signal path that needs to be able to communicate to 2 different signal paths.

9.2 Typical Application

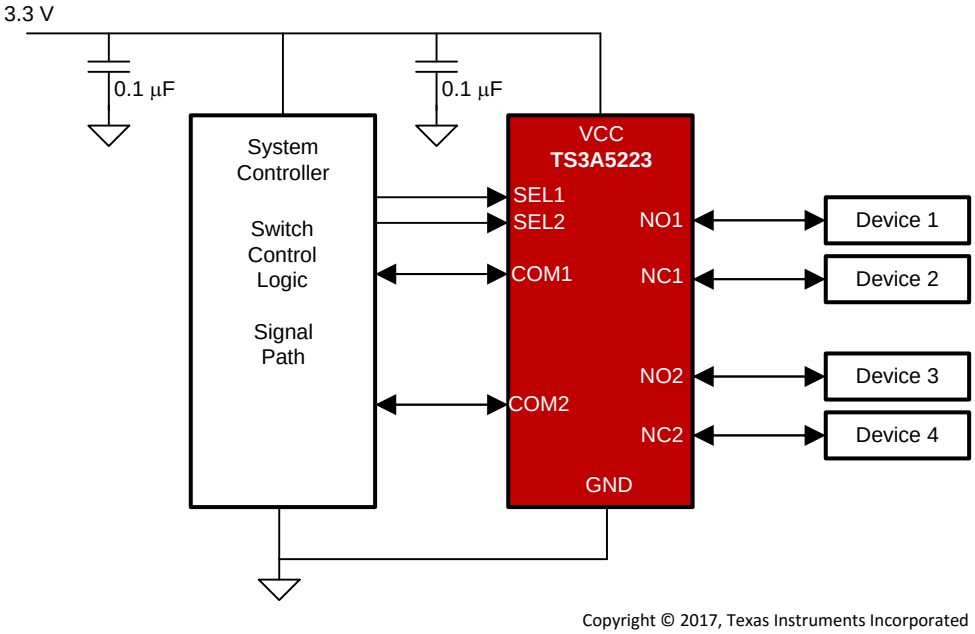


Figure 13. Typical Application

9.2.1 Design Requirements

The TS3A5223 can be properly operated without any external components.

Unused, pins COM, NC, and NO may be left floating or grounded.

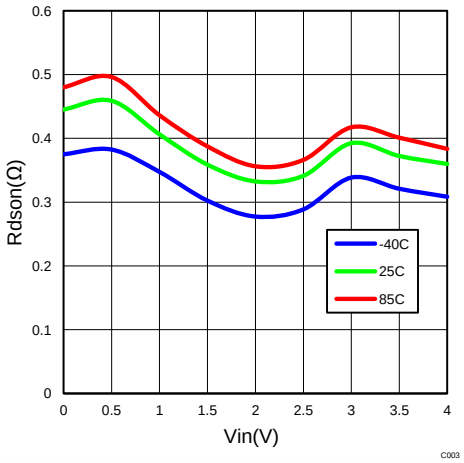
Digital control pins IN must be pulled up to VCC or down to GND to avoid undesired switch positions that could result from the floating pin and cause excess current consumption. For more information, refer to the application note *Implications of Slow or Floating CMOS Inputs* (SCBA002).

9.2.2 Detailed Design Procedure

Ensure that all of the signals passing through the switch are within the ranges specified in *Recommended Operating Conditions* to ensure proper performance.

Typical Application (continued)

9.2.3 Application Curves



V_{CC} = 3.6 V

Figure 14. On-Resistance vs. Switch Input Voltage

10 Power Supply Recommendations

TI recommends proper power-supply sequencing for all CMOS devices. Do not exceed the absolute-maximum ratings, because stresses beyond the listed ratings can cause permanent damage to the device. Always sequence VCC on first, followed by NO, NC, or COM. Although it is not required, power-supply bypassing improves noise margin and prevents switching noise propagation from the VCC supply to other components. A 0.1-μF capacitor, connected from VCC to GND, is adequate for most applications.

11 Layout

11.1 Layout Guidelines

- TI recommends following common printed-circuit board layout guidelines to ensure reliability of the device.
- Bypass capacitors should be used on power supplies.
- Short trace lengths should be used to avoid excessive loading.

11.2 Layout Example

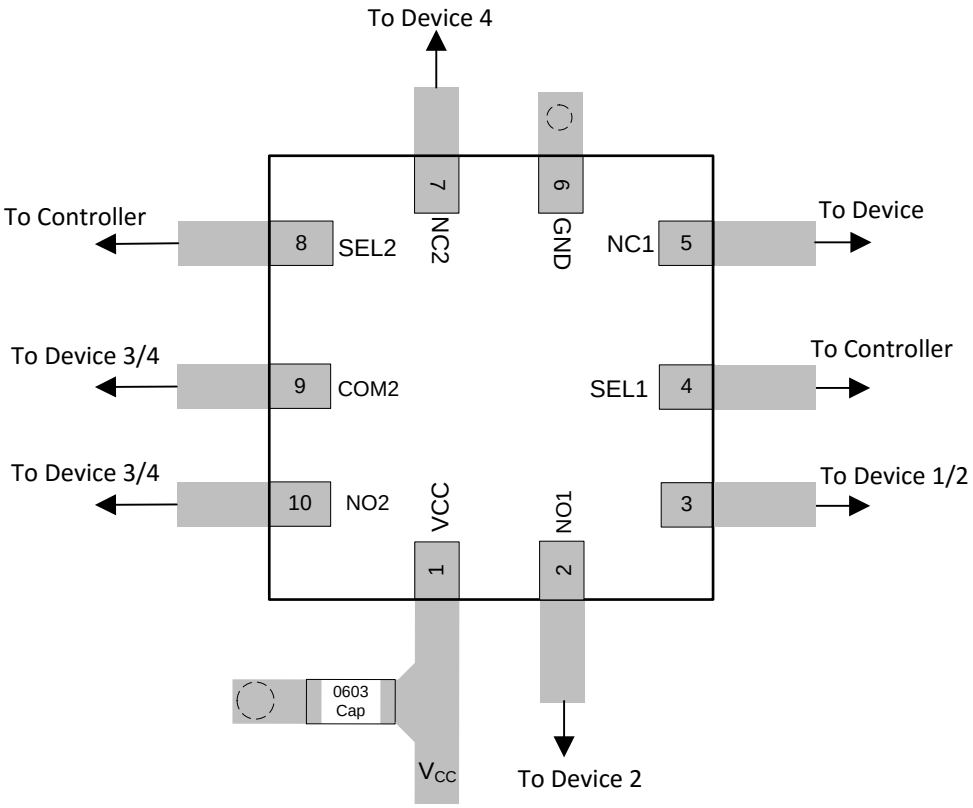


Figure 15. Layout Example

12 器件和文档支持

12.1 文档支持

12.2 接收文档更新通知

要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。请单击右上角的*通知我* 进行注册，即可收到任意产品信息更改每周摘要。有关更改的详细信息，请查看任意已修订文档中包含的修订历史记录。

12.3 社区资源

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.4 商标

E2E is a trademark of Texas Instruments.

12.5 静电放电警告

ESD 可能会损坏该集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理措施和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。 精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

12.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 机械、封装和可订购信息

以下页面包括机械、封装和可订购信息。这些信息是指定器件的最新可用数据。这些数据发生变化时，我们可能不会另行通知或修订此文档。如欲获取此产品说明书的浏览器版本，请参见左侧的导航栏。

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TS3A5223RSWR	ACTIVE	UQFN	RSW	10	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	B2A	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

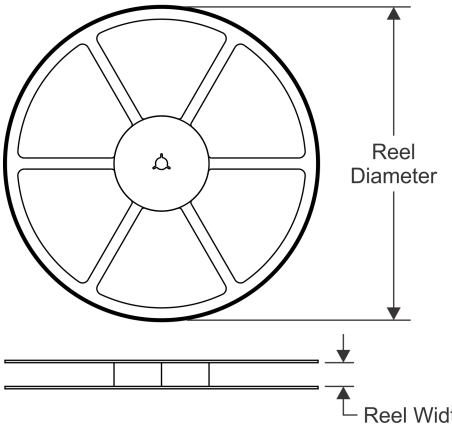
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

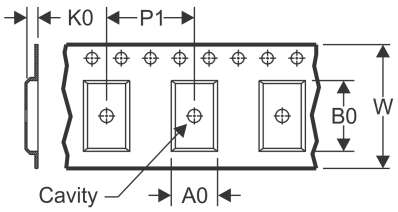
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

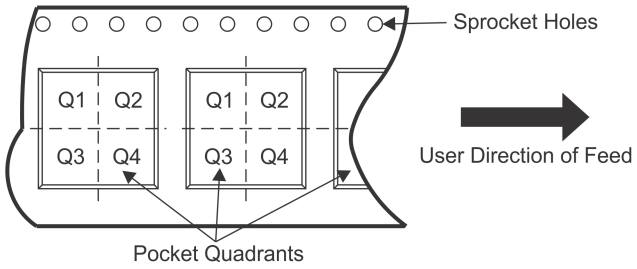


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

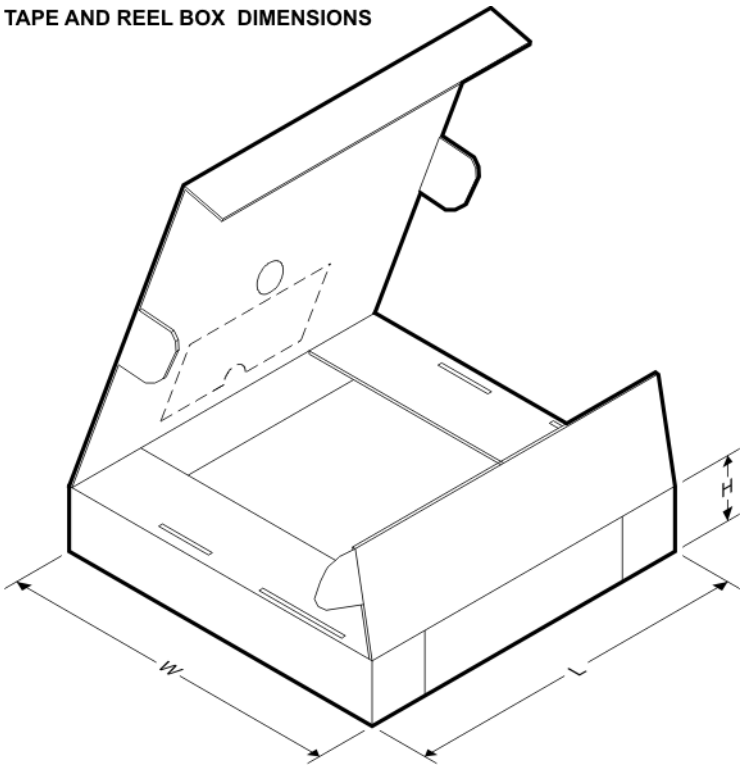
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TS3A5223RSWR	UQFN	RSW	10	3000	180.0	9.5	1.16	1.16	0.5	4.0	8.0	Q1

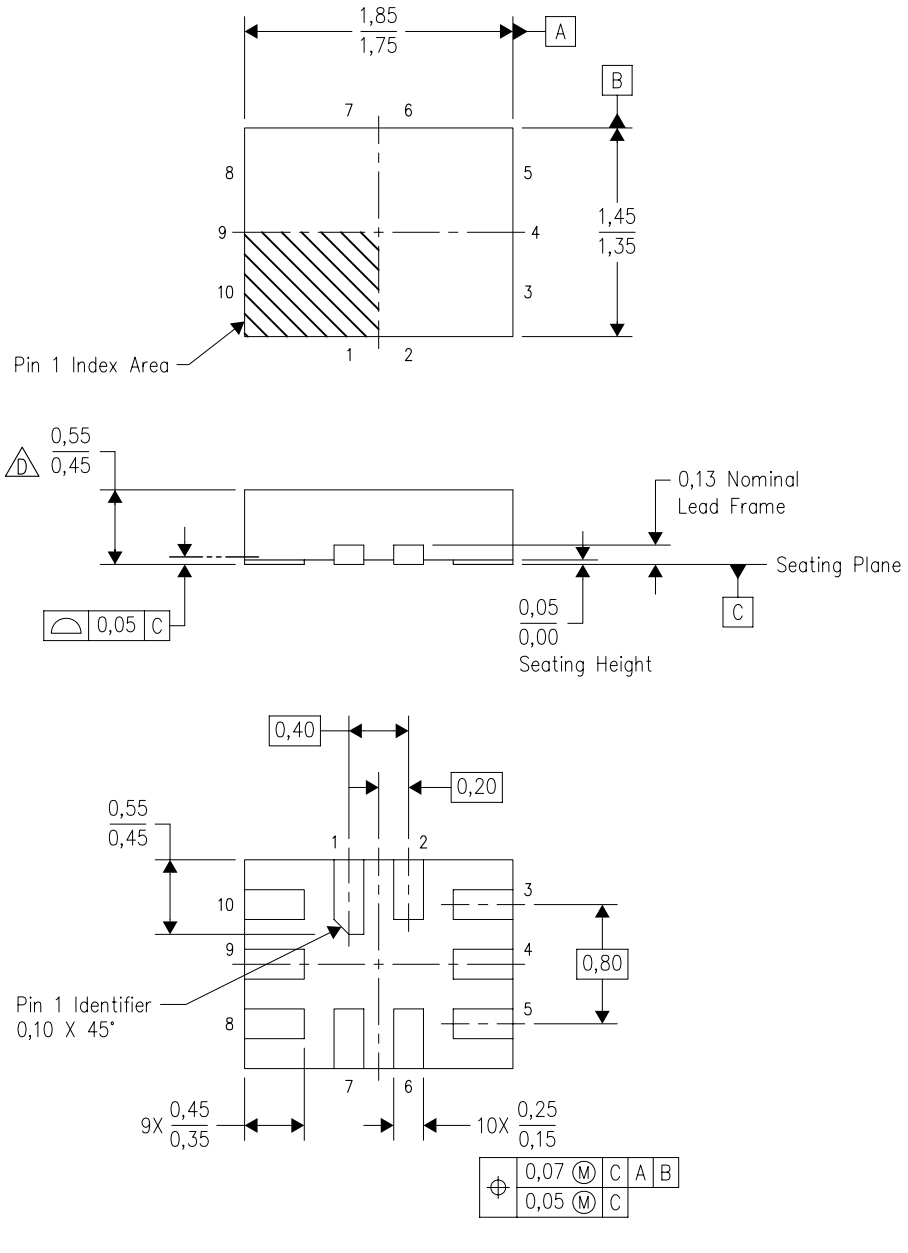
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TS3A5223RSWR	UQFN	RSW	10	3000	184.0	184.0	19.0

RSW (R–PUQFN–N10) PLASTIC QUAD FLATPACK NO–LEAD



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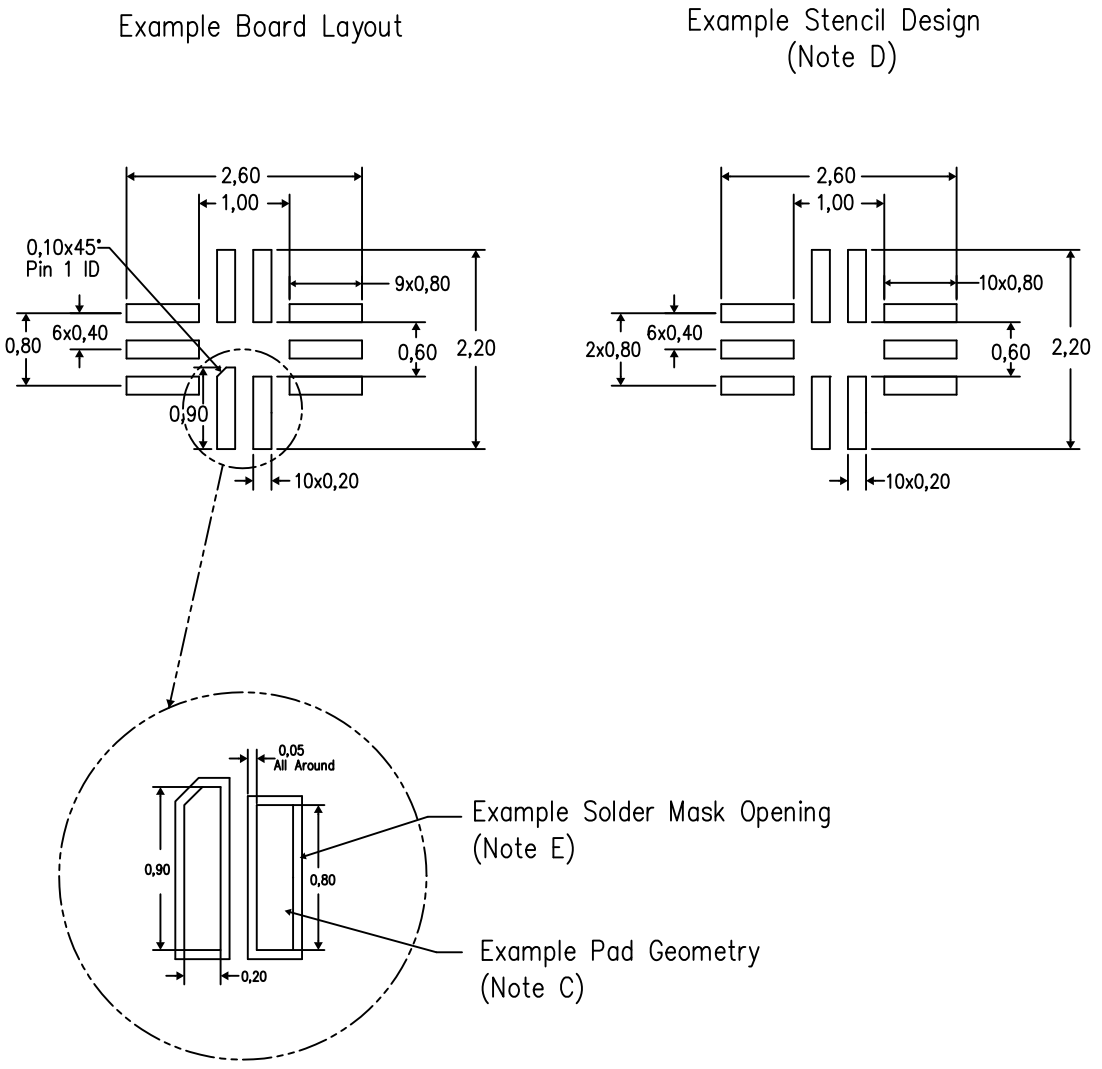
NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. QFN (Quad Flatpack No–lead) package configuration.
D. This package complies to JEDEC MO–288 variation UDEE, except minimum package height.

RSW (R–PUQFN–N10) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
E. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.

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