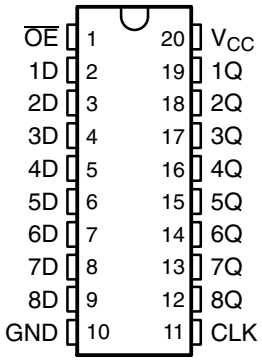
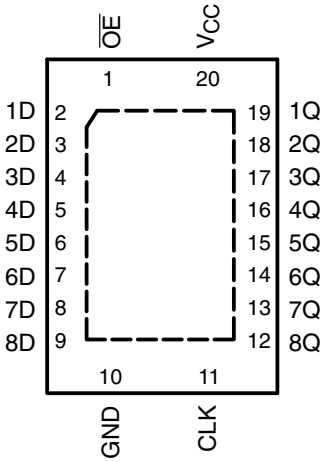
- **Operate From 1.65 V to 3.6 V**
- **Inputs Accept Voltages to 5.5 V**
- **Specified From –40°C to 85°C, –40°C to 125°C, and –55°C to 125°C**
- **Max $t_{pd}$ of 7 ns at 3.3 V**
- **Typical $V_{OLP}$ (Output Ground Bounce) <0.8 V at $V_{CC}$ = 3.3 V, $T_A$ = 25°C**
- **Typical $V_{OHV}$ (Output $V_{OH}$ Undershoot) >2 V at $V_{CC}$ = 3.3 V, $T_A$ = 25°C**
- **Support Mixed-Mode Signal Operation on All Ports (5-V Input/Output Voltage With 3.3-V $V_{CC}$)**
- **$I_{off}$ Supports Partial-Power-Down Mode Operation**
- **Latch-Up Performance Exceeds 250 mA Per JESD 17**
- **ESD Protection Exceeds JESD 22**
  - **2000-V Human-Body Model (A114-A)**
  - **200-V Machine Model (A115-A)**
  - **1000-V Charged-Device Model (C101)**

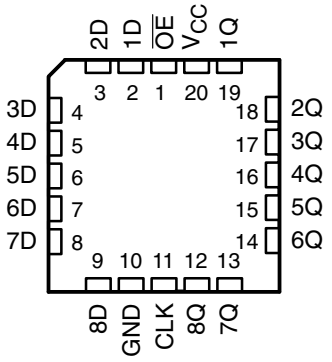
**SN54LVC574A . . . J OR W PACKAGE**
**SN74LVC574A . . . DB, DGV, DW, N, NS, OR PW PACKAGE**
**(TOP VIEW)**




**SN74LVC574A . . . RGY PACKAGE**
**(TOP VIEW)**




**SN54LVC574A . . . FK PACKAGE**
**(TOP VIEW)**




## description/ordering information

The SN54LVC574A octal edge-triggered D-type flip-flop is designed for 2.7-V to 3.6-V $V_{CC}$ operation, and the SN74LVC574A octal edge-triggered D-type flip-flop is designed for 1.65-V to 3.6-V $V_{CC}$ operation.

These devices feature 3-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. They are particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

On the positive transition of the clock (CLK) input, the Q outputs are set to the logic levels at the data (D) inputs.

A buffered output-enable ($\overline{OE}$) input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or the high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive bus lines without interface or pullup components.

$\overline{OE}$ does not affect the internal operations of the flip-flops. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

These devices are fully specified for partial-power-down applications using $I_{off}$. The $I_{off}$ circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

## description/ordering information (continued)

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to $V_{CC}$ through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

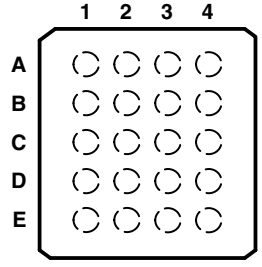
Inputs can be driven from either 3.3-V or 5-V devices. This feature allows the use of these devices as translators in a mixed 3.3-V/5-V system environment.

**ORDERING INFORMATION**

| $T_A$ | PACKAGE† | | ORDERABLE PART NUMBER | TOP-SIDE MARKING |
|---|---|---|---|---|
| –40°C to 85°C | QFN – RGY | Reel of 1000 | SN74LVC574ARGYR | LC574A |
| | VFBGA – GQN | Reel of 1000 | SN74LVC574AGQNR | LC574A |
| | VFBGA – ZQN (Pb-free) | | SN74LVC574AZQNR | |
| –40°C to 125°C | PDIP – N | Tube of 20 | SN74LVC574AN | SN74LVC574AN |
| | SOIC – DW | Tube of 25 | SN74LVC574ADW | LVC574A |
| | | Reel of 2000 | SN74LVC574ADWR | |
| | SOP – NS | Reel of 2000 | SN74LVC574ANSR | LVC574A |
| | SSOP – DB | Reel of 2000 | SN74LVC574ADBR | LC574A |
| | TSSOP – PW | Tube of 70 | SN74LVC574APW | LC574A |
| | | Reel of 2000 | SN74LVC574APWR | |
| | | Reel of 250 | SN74LVC574APWT | |
| | TVSOP – DGV | Reel of 2000 | SN74LVC574ADGVR | LC574A |
| –55°C to 125°C | CDIP – J | Tube of 20 | SNJ54LVC574AJ | SNJ54LVC574AJ |
| | CFP – W | Tube of 85 | SNJ54LVC574AW | SNJ54LVC574AW |
| | LCCC – FK | Tube of 55 | SNJ54LVC574AFK | SNJ54LVC574AFK |

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

**GQN OR ZQN PACKAGE**
**(TOP VIEW)**



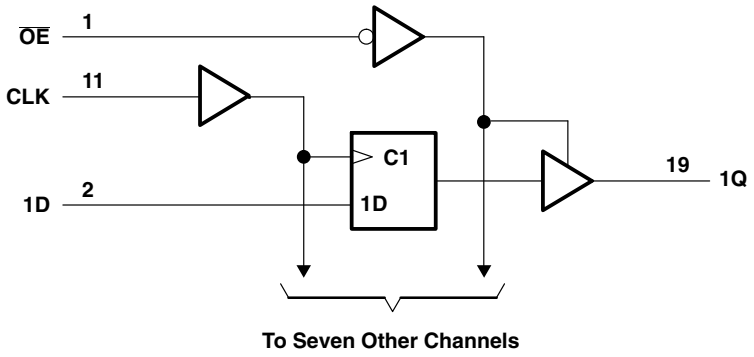

### terminal assignments

| | 1 | 2 | 3 | 4 |
|---|---|---|---|---|
| A | 1D | $\overline{OE}$ | $V_{CC}$ | 1Q |
| B | 3D | 3Q | 2D | 2Q |
| C | 5D | 4D | 5Q | 4Q |
| D | 7D | 7Q | 6D | 6Q |
| E | GND | 8D | CLK | 8Q |

**FUNCTION TABLE**
**(each flip-flop)**

| INPUTS | | | OUTPUT |
|---|---|---|---|
| $\overline{OE}$ | CLK | D | Q |
| L | ↑ | H | H |
| L | ↑ | L | L |
| L | L | X | $Q_0$ |
| H | X | X | Z |

### logic diagram (positive logic)




Pin numbers shown are for the DB, DGV, DW, FK, J, N, NS, PW, RGY, and W packages.

### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, $V_{CC}$ . . . . . –0.5 V to 6.5 V
Input voltage range, $V_I$ (see Note 1) . . . . . –0.5 V to 6.5 V
Voltage range applied to any output in the high-impedance or power-off state, $V_O$
(see Note 1) . . . . . –0.5 V to 6.5 V
Voltage range applied to any output in the high or low state, $V_O$
(see Notes 1 and 2) . . . . . –0.5 V to $V_{CC}$ + 0.5 V
Input clamp current, $I_{IK}$ ($V_I$ < 0) . . . . . –50 mA
Output clamp current, $I_{OK}$ ($V_O$ < 0) . . . . . –50 mA
Continuous output current, $I_O$ . . . . . ±50 mA
Continuous current through $V_{CC}$ or GND . . . . . ±100 mA
Package thermal impedance, $\theta_{JA}$ (see Note 3): DB package . . . . . 70°C/W
(see Note 3): DGV package . . . . . 92°C/W
(see Note 3): DW package . . . . . 58°C/W
(see Note 3): GQN/ZQN package . . . . . 78°C/W
(see Note 3): N package . . . . . 69°C/W
(see Note 3): NS package . . . . . 60°C/W
(see Note 3): PW package . . . . . 83°C/W
(see Note 4): RGY package . . . . . 37°C/W
Storage temperature range, $T_{stg}$ . . . . . –65°C to 150°C
Power dissipation, $P_{tot}$ ($T_A$ = –40°C to 125°C) (see Notes 5 and 6) . . . . . 500 mW

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The value of $V_{CC}$ is provided in the recommended operating conditions table.
3. The package thermal impedance is calculated in accordance with JESD 51-7.
4. The package thermal impedance is calculated in accordance with JESD 51-5.
5. For the DW package: above 70°C the value of $P_{tot}$ derates linearly with 8 mW/K.
6. For the DB, DGV, N, NS, and PW packages: above 60°C the value of $P_{tot}$ derates linearly with 5.5 mW/K.

## recommended operating conditions (see Note 7)

| | | | SN54LVC574A | | UNIT |
|---|---|---|---|---|---|
| | | | –55 TO 125°C | | |
| | | | MIN | MAX | |
| $V_{CC}$ | Supply voltage | Operating | 2 | 3.6 | V |
| | | Data retention only | 1.5 | | |
| $V_{IH}$ | High-level input voltage | $V_{CC}$ = 2.7 V to 3.6 V | 2 | | V |
| $V_{IL}$ | Low-level input voltage | $V_{CC}$ = 2.7 V to 3.6 V | | 0.8 | V |
| $V_I$ | Input voltage | | 0 | 5.5 | V |
| $V_O$ | Output voltage | High or low state | 0 | $V_{CC}$ | V |
| | | 3–state | 0 | 5.5 | |
| $I_{OH}$ | High-level output current | $V_{CC}$ = 2.7 V | | –12 | mA |
| | | $V_{CC}$ = 3 V | | –24 | |
| $I_{OL}$ | Low-level output current | $V_{CC}$ = 2.7 V | | 12 | mA |
| | | $V_{CC}$ = 3 V | | 24 | |
| $\Delta t/\Delta v$ | Input transition rise or fall rate | | | 6 | ns/V |

NOTE 7: All unused inputs of the device must be held at $V_{CC}$ or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

## recommended operating conditions (see Note 7)

| | | | SN74LVC574A | | | | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | $T_A$ = 25°C | | –40 TO 85°C | | –40 TO 125°C | | |
| | | | MIN | MAX | MIN | MAX | MIN | MAX | |
| $V_{CC}$ | Supply voltage | Operating | 1.65 | 3.6 | 1.65 | 3.6 | 1.65 | 3.6 | V |
| | | Data retention only | 1.5 | | 1.5 | | 1.5 | | |
| $V_{IH}$ | High-level input voltage | $V_{CC}$ = 1.65 V to 1.95 V | 0.65 × $V_{CC}$ | | 0.65 × $V_{CC}$ | | 0.65 × $V_{CC}$ | | V |
| | | $V_{CC}$ = 2.3 V to 2.7 V | 1.7 | | 1.7 | | 1.7 | | |
| | | $V_{CC}$ = 2.7 V to 3.6 V | 2 | | 2 | | 2 | | |
| $V_{IL}$ | Low-level input voltage | $V_{CC}$ = 1.65 V to 1.95 V | | 0.35 × $V_{CC}$ | | 0.35 × $V_{CC}$ | | 0.35 × $V_{CC}$ | V |
| | | $V_{CC}$ = 2.3 V to 2.7 V | | 0.7 | | 0.7 | | 0.7 | |
| | | $V_{CC}$ = 2.7 V to 3.6 V | | 0.8 | | 0.8 | | 0.8 | |
| $V_I$ | Input voltage | | 0 | 5.5 | 0 | 5.5 | 0 | 5.5 | V |
| $V_O$ | Output voltage | High or low state | 0 | $V_{CC}$ | 0 | $V_{CC}$ | 0 | $V_{CC}$ | V |
| | | 3–state | 0 | 5.5 | 0 | 5.5 | 0 | 5.5 | |
| $I_{OH}$ | High-level output current | $V_{CC}$ = 1.65 V | | –4 | | –4 | | –4 | mA |
| | | $V_{CC}$ = 2.3 V | | –8 | | –8 | | –8 | |
| | | $V_{CC}$ = 2.7 V | | –12 | | –12 | | –12 | |
| | | $V_{CC}$ = 3 V | | –24 | | –24 | | –24 | |
| $I_{OL}$ | Low-level output current | $V_{CC}$ = 1.65 V | | 4 | | 4 | | 4 | mA |
| | | $V_{CC}$ = 2.3 V | | 8 | | 8 | | 8 | |
| | | $V_{CC}$ = 2.7 V | | 12 | | 12 | | 12 | |
| | | $V_{CC}$ = 3 V | | 24 | | 24 | | 24 | |
| $\Delta t/\Delta v$ | Input transition rise or fall rate | | | 6 | | 6 | | 6 | ns/V |

NOTE 7: All unused inputs of the device must be held at $V_{CC}$ or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

**electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)**

| PARAMETER | TEST CONDITIONS | | $V_{CC}$ | SN54LVC574A –55 TO 125°C | | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | | MIN | TYP† | MAX | |
| $V_{OH}$ | $I_{OH}$ = –100 μA | | 2.7 V to 3.6 V | $V_{CC}$ – 0.2 | | | V |
| | $I_{OH}$ = –12 mA | | 2.7 V | 2.2 | | | |
| | | | 3 V | 2.4 | | | |
| | $I_{OH}$ = –24 mA | | 3 V | 2.2 | | | |
| $V_{OL}$ | $I_{OL}$ = 100 μA | | 2.7 V to 3.6 V | | | 0.2 | V |
| | $I_{OL}$ = 12 mA | | 2.7 V | | | 0.4 | |
| | $I_{OL}$ = 24 mA | | 3 V | | | 0.55 | |
| $I_I$ | $V_I$ = 5.5 V or GND | | 3.6 V | | | ±5 | μA |
| $I_{OZ}$ | $V_O$ = 0 to 5.5 V | | 3.6 V | | | ±15 | μA |
| $I_{CC}$ | $V_I = V_{CC}$ or GND | $I_O$ = 0 | 3.6 V | | | 10 | μA |
| | 3.6 V ≤ $V_I$ ≤ 5.5 V‡ | | | | | 10 | |
| $\Delta I_{CC}$ | One input at $V_{CC}$ – 0.6 V, Other inputs at $V_{CC}$ or GND | | 2.7 V to 3.6 V | | | 500 | μA |
| $C_i$ | $V_I = V_{CC}$ or GND | | 3.3 V | | 4 | | pF |
| $C_o$ | $V_O = V_{CC}$ or GND | | 3.3 V | | 5.5 | | pF |

† $T_A$ = 25°C
‡ This applies in the disabled state only.

### electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | | $V_{CC}$ | SN74LVC574A | | | | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | $T_A$ = 25°C | | | –40 TO 85°C | | –40 TO 125°C | | |
| | | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| $V_{OH}$ | $I_{OH}$ = –100 μA | | 1.65 V to 3.6 V | $V_{CC}$ – 0.2 | | | $V_{CC}$ – 0.2 | | $V_{CC}$ – 0.2 | | V |
| | $I_{OH}$ = –4 mA | | 1.65 V | 1.29 | | | 1.2 | | 1.2 | | |
| | $I_{OH}$ = –8 mA | | 2.3 V | 1.9 | | | 1.7 | | 1.7 | | |
| | $I_{OH}$ = –12 mA | | 2.7 V | 2.2 | | | 2.2 | | 2.2 | | |
| | | | 3 V | 2.4 | | | 2.4 | | 2.4 | | |
| | $I_{OH}$ = –24 mA | | 3 V | 2.3 | | | 2.2 | | 2.2 | | |
| $V_{OL}$ | $I_{OL}$ = 100 μA | | 1.65 V to 3.6 V | | | 0.1 | | 0.2 | | 0.2 | V |
| | $I_{OL}$ = 4 mA | | 1.65 V | | | 0.24 | | 0.45 | | 0.45 | |
| | $I_{OL}$ = 8 mA | | 2.3 V | | | 0.3 | | 0.7 | | 0.7 | |
| | $I_{OL}$ = 12 mA | | 2.7 V | | | 0.4 | | 0.4 | | 0.4 | |
| | $I_{OL}$ = 24 mA | | 3 V | | | 0.55 | | 0.55 | | 0.55 | |
| $I_I$ | $V_I$ = 5.5 V or GND | | 3.6 V | | | ±1 | | ±5 | | ±5 | μA |
| $I_{off}$ | $V_I$ or $V_O$ = 5.5 V | | 0 | | | ±4 | | ±10 | | ±10 | μA |
| $I_{OZ}$ | $V_I$ = 0 to 5.5 V | | 3.6 V | | | ±1 | | ±10 | | ±10 | μA |
| $I_{CC}$ | $V_I$ = $V_{CC}$ or GND | $I_O$ = 0 | 3.6 V | | | 1.5 | | 10 | | 10 | μA |
| | 3.6 V ≤ $V_I$ ≤ 5.5 V† | | | | | 1.5 | | 10 | | 10 | |
| $\Delta I_{CC}$ | One input at $V_{CC}$ – 0.6 V, Other inputs at $V_{CC}$ or GND | | 2.7 V to 3.6 V | | | 500 | | 500 | | 500 | μA |
| $C_i$ | $V_I$ = $V_{CC}$ or GND | | 3.3 V | | 4 | | | | | | pF |
| $C_o$ | $V_O$ = $V_{CC}$ or GND | | 3.3 V | | 5.5 | | | | | | pF |

† This applies in the disabled state only.

### timing requirements over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

| | | $V_{CC}$ | SN54LVC574A | | UNIT |
|---|---|---|---|---|---|
| | | | –55 TO 125°C | | |
| | | | MIN | MAX | |
| $f_{clock}$ | Clock frequency | 2.7 V | | 150 | MHz |
| | | 3.3 V ± 0.3 V | | 150 | |
| $t_w$ | Pulse duration, CLK high or low | 2.7 V | 3.3 | | ns |
| | | 3.3 V ± 0.3 V | 3.3 | | |
| $t_{su}$ | Setup time, data before CLK↑ | 2.7 V | 2 | | ns |
| | | 3.3 V ± 0.3 V | 2 | | |
| $t_h$ | Hold time, data after CLK↑ | 2.7 V | 2 | | ns |
| | | 3.3 V ± 0.3 V | 2 | | |

**switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)**

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | $V_{CC}$ | SN54LVC574A | | UNIT |
|---|---|---|---|---|---|---|
| | | | | –55 TO 125°C | | |
| | | | | MIN | MAX | |
| $f_{max}$ | | | 2.7 V | 150 | | MHz |
| | | | 3.3 V ± 0.3 V | 150 | | |
| $t_{pd}$ | CLK | Q | 2.7 V | | 8 | ns |
| | | | 3.3 V ± 0.3 V | 1 | 7 | |
| $t_{en}$ | $\overline{OE}$ | Q | 2.7 V | | 9 | ns |
| | | | 3.3 V ± 0.3 V | 1 | 7.5 | |
| $t_{dis}$ | $\overline{OE}$ | Q | 2.7 V | | 7 | ns |
| | | | 3.3 V ± 0.3 V | 0.5 | 6.4 | |

**timing requirements over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)**

| | | $V_{CC}$ | SN74LVC574A | | | | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | $T_A$ = 25°C | | | –40 TO 85°C | | –40 TO 125°C | |
| | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| $f_{clock}$ | Clock frequency | 1.8 V ± 0.15 V | | | 55 | | 55 | | 40 | MHz |
| | | 2.5 V ± 0.2 V | | | 95 | | 95 | | 80 | |
| | | 2.7 V | | | 150 | | 150 | | 150 | |
| | | 3.3 V ± 0.3 V | | | 150 | | 150 | | 150 | |
| $t_w$ | Pulse duration, CLK high or low | 1.8 V ± 0.15 V | 9 | | | 9 | | 9 | | ns |
| | | 2.5 V ± 0.2 V | 4 | | | 4 | | 4 | | |
| | | 2.7 V | 3.3 | | | 3.3 | | 3.3 | | |
| | | 3.3 V ± 0.3 V | 3.3 | | | 3.3 | | 3.3 | | |
| $t_{su}$ | Setup time, data before CLK↑ | 1.8 V ± 0.15 V | 6 | | | 6 | | 6 | | ns |
| | | 2.5 V ± 0.2 V | 4 | | | 4 | | 4 | | |
| | | 2.7 V | 2 | | | 2 | | 2 | | |
| | | 3.3 V ± 0.3 V | 2 | | | 2 | | 2 | | |
| $t_h$ | Hold time, data after CLK↑ | 1.8 V ± 0.15 V | 4 | | | 4 | | 4 | | ns |
| | | 2.5 V ± 0.2 V | 2 | | | 2 | | 2 | | |
| | | 2.7 V | 1.5 | | | 1.5 | | 1.5 | | |
| | | 3.3 V ± 0.3 V | 1.5 | | | 1.5 | | 1.5 | | |

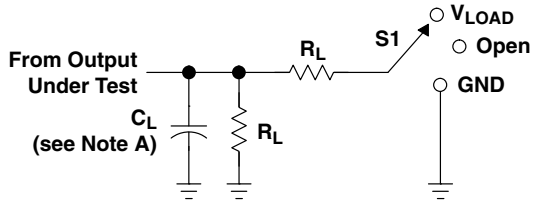
**switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)**

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | $V_{CC}$ | SN74LVC574A | | | | | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | $T_A$ = 25°C | | | –40 TO 85°C | | –40 TO 125°C | | |
| | | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| $f_{max}$ | | | 1.8 V ± 0.15 V | 55 | | | 55 | | 40 | | MHz |
| | | | 2.5 V ± 02 V | 95 | | | 95 | | 80 | | |
| | | | 2.7 V | 150 | | | 150 | | 150 | | |
| | | | 3.3 V ± 0.3 V | 150 | | | 150 | | 150 | | |
| $t_{pd}$ | CLK | Q | 1.8 V ± 0.15 V | 1.0 | 7.1 | 21.5 | 1 | 21.6 | 1.0 | 21.6 | ns |
| | | | 2.5 V ± 0.2 V | 1.0 | 4.9 | 10.0 | 1 | 10.5 | 1.0 | 10.5 | |
| | | | 2.7 V | 1.0 | 5.0 | 7.8 | 1 | 8 | 1.0 | 8.0 | |
| | | | 3.3 V ± 0.3 V | 2.2 | 4.6 | 6.8 | 2.2 | 7 | 2.2 | 7.0 | |
| $t_{en}$ | $\overline{OE}$ | Q | 1.8 V ± 0.15 V | 1.0 | 6.6 | 19.0 | 1 | 19.5 | 1.0 | 19.5 | ns |
| | | | 2.5 V ± 0.2 V | 1.0 | 4.8 | 10.0 | 1 | 10.5 | 1.0 | 10.5 | |
| | | | 2.7 V | 1.0 | 5.5 | 8.3 | 1 | 8.5 | 1.0 | 8.5 | |
| | | | 3.3 V ± 0.3 V | 1.5 | 4.4 | 7.3 | 1.5 | 7.5 | 1.5 | 7.5 | |
| $t_{dis}$ | $\overline{OE}$ | Q | 1.8 V ± 0.15 V | 1.0 | 5.4 | 18.3 | 1 | 18.8 | 1.0 | 18.8 | ns |
| | | | 2.5 V ± 0.2 V | 1.0 | 3.0 | 7.3 | 1 | 7.8 | 1.0 | 7.8 | |
| | | | 2.7 V | 1.0 | 4.0 | 6.8 | 1 | 7 | 1.0 | 7.3 | |
| | | | 3.3 V ± 0.3 V | 1.7 | 3.9 | 6.2 | 1.7 | 6.4 | 1.7 | 6.6 | |
| $t_{sk(o)}$ | | | 3.3 V ± 0.3 V | | | | | 1 | | 1 | ns |

**operating characteristics, $T_A$ = 25°C**

| PARAMETER | | TEST CONDITIONS | $V_{CC}$ | TYP | UNIT |
|---|---|---|---|---|---|
| $C_{pd}$ Power dissipation capacitance per flip–flop | Outputs enabled | f = 10 MHz | 1.8 V | 25 | pF |
| | | | 2.5 V | 29 | |
| | | | 3.3 V | 30 | |
| | Outputs disabled | | 1.8 V | 9 | |
| | | | 2.5 V | 9 | |
| | | | 3.3 V | 11 | |

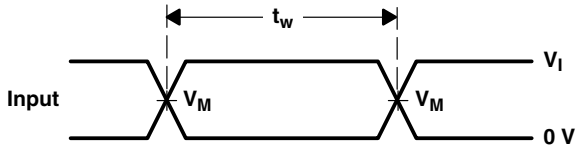
## PARAMETER MEASUREMENT INFORMATION



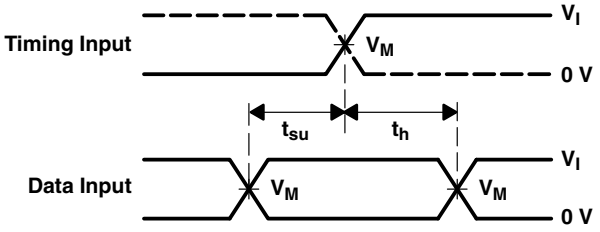

LOAD CIRCUIT

| TEST | S1 |
|---|---|
| $t_{PLH}/t_{PHL}$ | Open |
| $t_{PLZ}/t_{PZL}$ | $V_{LOAD}$ |
| $t_{PHZ}/t_{PZH}$ | GND |

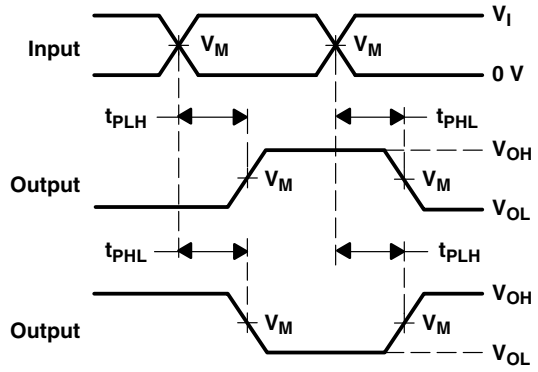
| $V_{CC}$ | INPUTS | | $V_M$ | $V_{LOAD}$ | $C_L$ | $R_L$ | $V_\Delta$ |
|---|---|---|---|---|---|---|---|
| | $V_I$ | $t_r/t_f$ | | | | | |
| 1.8 V ± 0.15 V | $V_{CC}$ | ≤2 ns | $V_{CC}/2$ | $2 \times V_{CC}$ | 30 pF | 1 kΩ | 0.15 V |
| 2.5 V ± 0.2 V | $V_{CC}$ | ≤2 ns | $V_{CC}/2$ | $2 \times V_{CC}$ | 30 pF | 500 Ω | 0.15 V |
| 2.7 V | 2.7 V | ≤2.5 ns | 1.5 V | 6 V | 50 pF | 500 Ω | 0.3 V |
| 3.3 V ± 0.3 V | 2.7 V | ≤2.5 ns | 1.5 V | 6 V | 50 pF | 500 Ω | 0.3 V |



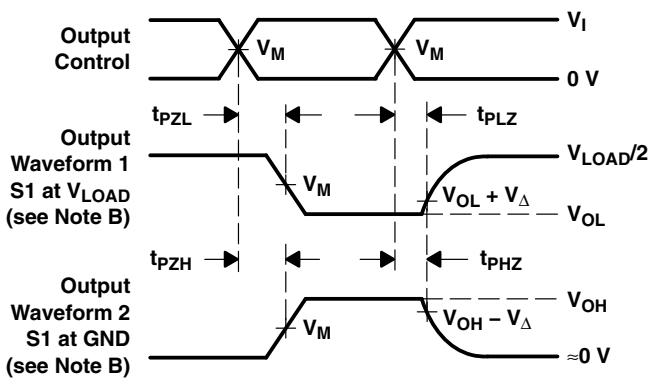

VOLTAGE WAVEFORMS
PULSE DURATION




VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES




VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS




VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES: A. $C_L$ includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, $Z_O$ = 50 Ω.
D. The outputs are measured one at a time, with one transition per measurement.
E. $t_{PLZ}$ and $t_{PHZ}$ are the same as $t_{dis}$.
F. $t_{PZL}$ and $t_{PZH}$ are the same as $t_{en}$.
G. $t_{PLH}$ and $t_{PHL}$ are the same as $t_{pd}$.
H. All parameters and waveforms are not applicable to all devices.

**Figure 1. Load Circuit and Voltage Waveforms**

# THERMAL PAD MECHANICAL DATA

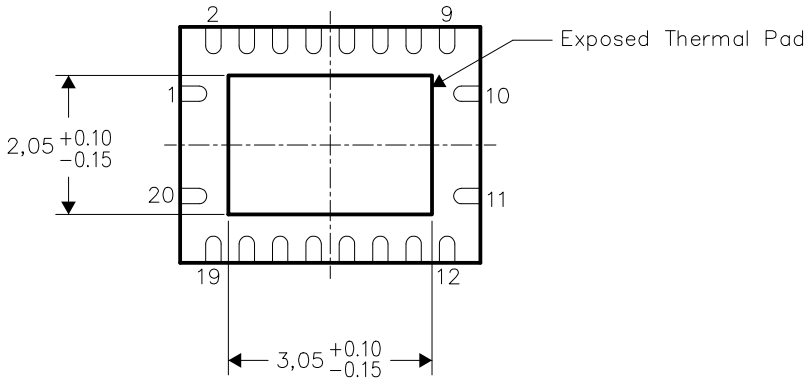
## RGY (R–PQFP–N20)

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB), the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to a ground plane or special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, Quad Flatpack No–Lead Logic Packages, Texas Instruments Literature No. SCBA017. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.




Bottom View

NOTE: All linear dimensions are in millimeters

Exposed Thermal Pad Dimensions

4206353–4/A 11/04

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 5962-9757601Q2A | ACTIVE | LCCC | FK | 20 | 1 | TBD | POST-PLATE | N / A for Pkg Type | -55 to 125 | 5962-9757601Q2A SNJ54LVC574AFK | Samples |
| 5962-9757601QRA | ACTIVE | CDIP | J | 20 | 1 | TBD | A42 | N / A for Pkg Type | -55 to 125 | 5962-9757601QRA SNJ54LVC574AJ | Samples |
| 5962-9757601QSA | ACTIVE | CFP | W | 20 | 1 | TBD | A42 | N / A for Pkg Type | -55 to 125 | 5962-9757601QSA SNJ54LVC574AW | Samples |
| SN74LVC574ADBLE | OBSOLETE | SSOP | DB | 20 | | TBD | Call TI | Call TI | -40 to 125 | | |
| SN74LVC574ADBR | ACTIVE | SSOP | DB | 20 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | LC574A | Samples |
| SN74LVC574ADBRE4 | ACTIVE | SSOP | DB | 20 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | LC574A | Samples |
| SN74LVC574ADBRG4 | ACTIVE | SSOP | DB | 20 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | LC574A | Samples |
| SN74LVC574ADGVR | ACTIVE | TVSOP | DGV | 20 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | LC574A | Samples |
| SN74LVC574ADGVRE4 | ACTIVE | TVSOP | DGV | 20 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | LC574A | Samples |
| SN74LVC574ADW | ACTIVE | SOIC | DW | 20 | 25 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | LVC574A | Samples |
| SN74LVC574ADWE4 | ACTIVE | SOIC | DW | 20 | 25 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | LVC574A | Samples |
| SN74LVC574ADWG4 | ACTIVE | SOIC | DW | 20 | 25 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | LVC574A | Samples |
| SN74LVC574ADWR | ACTIVE | SOIC | DW | 20 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | LVC574A | Samples |
| SN74LVC574ADWRE4 | ACTIVE | SOIC | DW | 20 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | LVC574A | Samples |
| SN74LVC574AGQNR | OBSOLETE | BGA MICROSTAR JUNIOR | GQN | 20 | | TBD | Call TI | Call TI | -40 to 125 | LC574A | |

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| SN74LVC574AN | ACTIVE | PDIP | N | 20 | 20 | Pb-Free (RoHS) | CU NIPDAU | N / A for Pkg Type | -40 to 125 | SN74LVC574AN | Samples |
| SN74LVC574ANSR | ACTIVE | SO | NS | 20 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | LVC574A | Samples |
| SN74LVC574ANSRE4 | ACTIVE | SO | NS | 20 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | LVC574A | Samples |
| SN74LVC574ANSRG4 | ACTIVE | SO | NS | 20 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | LVC574A | Samples |
| SN74LVC574APW | ACTIVE | TSSOP | PW | 20 | 70 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -55 to 125 | LC574A | Samples |
| SN74LVC574APWE4 | ACTIVE | TSSOP | PW | 20 | 70 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | LC574A | Samples |
| SN74LVC574APWG4 | ACTIVE | TSSOP | PW | 20 | 70 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | LC574A | Samples |
| SN74LVC574APWLE | OBSOLETE | TSSOP | PW | 20 | | TBD | Call TI | Call TI | -40 to 125 | | |
| SN74LVC574APWR | ACTIVE | TSSOP | PW | 20 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU \| CU SN | Level-1-260C-UNLIM | -40 to 125 | LC574A | Samples |
| SN74LVC574APWRE4 | ACTIVE | TSSOP | PW | 20 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | LC574A | Samples |
| SN74LVC574APWRG4 | ACTIVE | TSSOP | PW | 20 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | LC574A | Samples |
| SN74LVC574APWT | ACTIVE | TSSOP | PW | 20 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 125 | LC574A | Samples |
| SN74LVC574ARGYR | ACTIVE | VQFN | RGY | 20 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | LC574A | Samples |
| SN74LVC574ARGYRG4 | ACTIVE | VQFN | RGY | 20 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | LC574A | Samples |
| SN74LVC574AZQNR | ACTIVE | BGA MICROSTAR JUNIOR | ZQN | 20 | 1000 | Green (RoHS & no Sb/Br) | SNAGCU | Level-1-260C-UNLIM | -40 to 85 | LC574A | Samples |
| SNJ54LVC574AFK | ACTIVE | LCCC | FK | 20 | 1 | TBD | POST-PLATE | N / A for Pkg Type | -55 to 125 | 5962-9757601Q2A SNJ54LVC 574AFK | Samples |
| SNJ54LVC574AJ | ACTIVE | CDIP | J | 20 | 1 | TBD | A42 | N / A for Pkg Type | -55 to 125 | 5962-9757601QR A SNJ54LVC574AJ | Samples |

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| SNJ54LVC574AW | ACTIVE | CFP | W | 20 | 1 | TBD | A42 | N / A for Pkg Type | -55 to 125 | 5962-9757601QS A SNJ54LVC574AW | Samples |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
**TBD:** The Pb-Free/Green conversion plan has not been defined.
**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

**OTHER QUALIFIED VERSIONS OF SN54LVC574A, SN74LVC574A :**

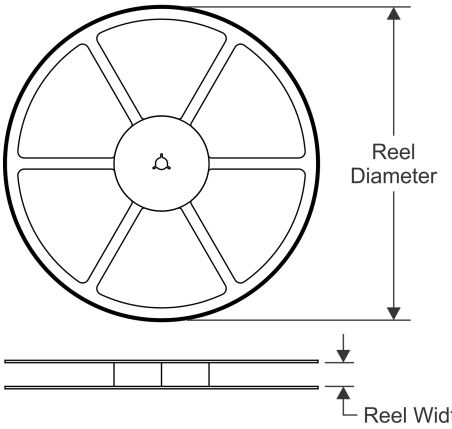
- Catalog: SN74LVC574A
- Automotive: SN74LVC574A-Q1, SN74LVC574A-Q1
- Enhanced Product: SN74LVC574A-EP, SN74LVC574A-EP
- Military: SN54LVC574A

NOTE: Qualified Version Definitions:

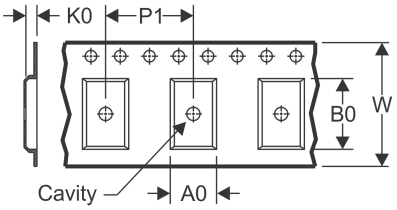
- Catalog - TI's standard catalog product
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects
- Enhanced Product - Supports Defense, Aerospace and Medical Applications
- Military - QML certified for Military and Defense Applications

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

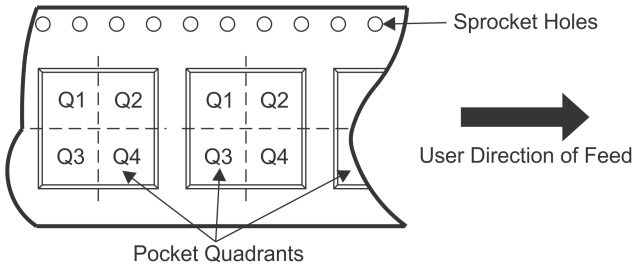



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

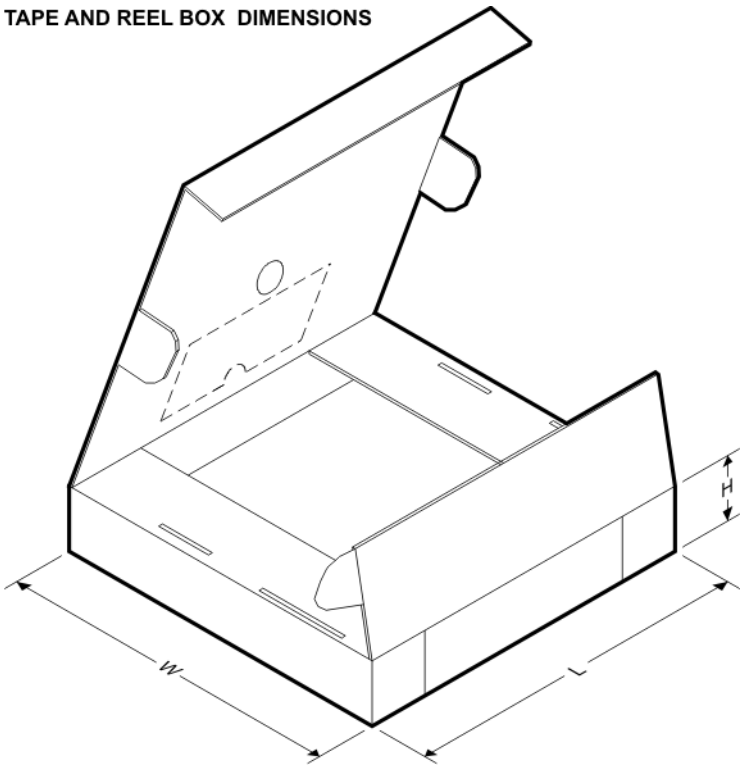
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| SN74LVC574ADBR | SSOP | DB | 20 | 2000 | 330.0 | 16.4 | 8.2 | 7.5 | 2.5 | 12.0 | 16.0 | Q1 |
| SN74LVC574ADGVR | TVSOP | DGV | 20 | 2000 | 330.0 | 12.4 | 6.9 | 5.6 | 1.6 | 8.0 | 12.0 | Q1 |
| SN74LVC574ADWR | SOIC | DW | 20 | 2000 | 330.0 | 24.4 | 10.8 | 13.3 | 2.7 | 12.0 | 24.0 | Q1 |
| SN74LVC574ANSR | SO | NS | 20 | 2000 | 330.0 | 24.4 | 8.2 | 13.0 | 2.5 | 12.0 | 24.0 | Q1 |
| SN74LVC574APWR | TSSOP | PW | 20 | 2000 | 330.0 | 16.4 | 6.95 | 7.1 | 1.6 | 8.0 | 16.0 | Q1 |
| SN74LVC574APWR | TSSOP | PW | 20 | 2000 | 330.0 | 16.4 | 6.95 | 7.1 | 1.6 | 8.0 | 16.0 | Q1 |
| SN74LVC574APWRG4 | TSSOP | PW | 20 | 2000 | 330.0 | 16.4 | 6.95 | 7.1 | 1.6 | 8.0 | 16.0 | Q1 |
| SN74LVC574APWT | TSSOP | PW | 20 | 250 | 330.0 | 16.4 | 6.95 | 7.1 | 1.6 | 8.0 | 16.0 | Q1 |
| SN74LVC574ARGYR | VQFN | RGY | 20 | 3000 | 330.0 | 12.4 | 3.8 | 4.8 | 1.6 | 8.0 | 12.0 | Q1 |
| SN74LVC574AZQNR | BGA MICROSTAR JUNIOR | ZQN | 20 | 1000 | 330.0 | 12.4 | 3.3 | 4.3 | 1.6 | 8.0 | 12.0 | Q1 |

**TAPE AND REEL BOX DIMENSIONS**



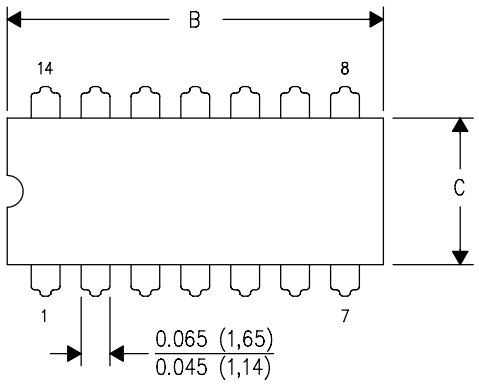

*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| SN74LVC574ADBR | SSOP | DB | 20 | 2000 | 367.0 | 367.0 | 38.0 |
| SN74LVC574ADGVR | TVSOP | DGV | 20 | 2000 | 367.0 | 367.0 | 35.0 |
| SN74LVC574ADWR | SOIC | DW | 20 | 2000 | 367.0 | 367.0 | 45.0 |
| SN74LVC574ANSR | SO | NS | 20 | 2000 | 367.0 | 367.0 | 45.0 |
| SN74LVC574APWR | TSSOP | PW | 20 | 2000 | 364.0 | 364.0 | 27.0 |
| SN74LVC574APWR | TSSOP | PW | 20 | 2000 | 367.0 | 367.0 | 38.0 |
| SN74LVC574APWRG4 | TSSOP | PW | 20 | 2000 | 367.0 | 367.0 | 38.0 |
| SN74LVC574APWT | TSSOP | PW | 20 | 250 | 367.0 | 367.0 | 38.0 |
| SN74LVC574ARGYR | VQFN | RGY | 20 | 3000 | 367.0 | 367.0 | 35.0 |
| SN74LVC574AZQNR | BGA MICROSTAR JUNIOR | ZQN | 20 | 1000 | 338.1 | 338.1 | 20.6 |

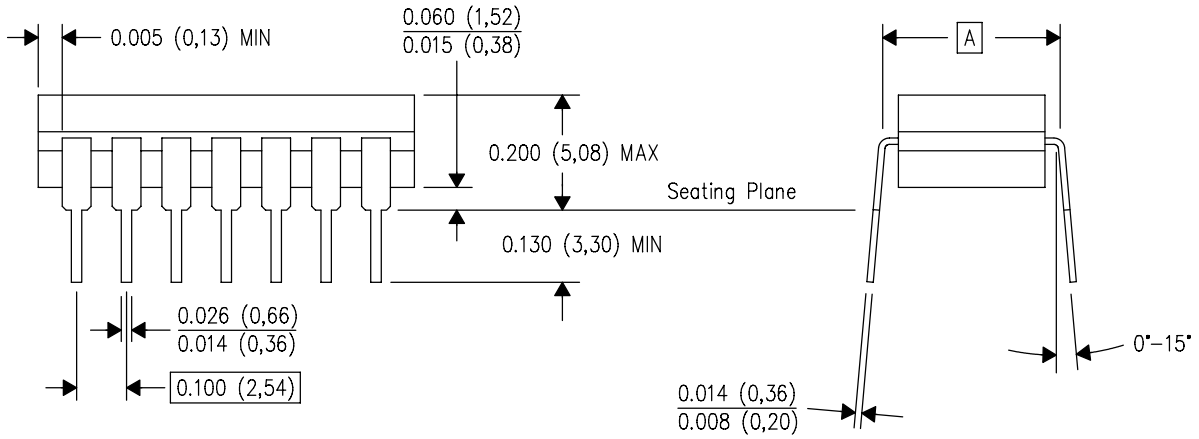
J (R–GDIP–T**)

14 LEADS SHOWN

# CERAMIC DUAL IN–LINE PACKAGE



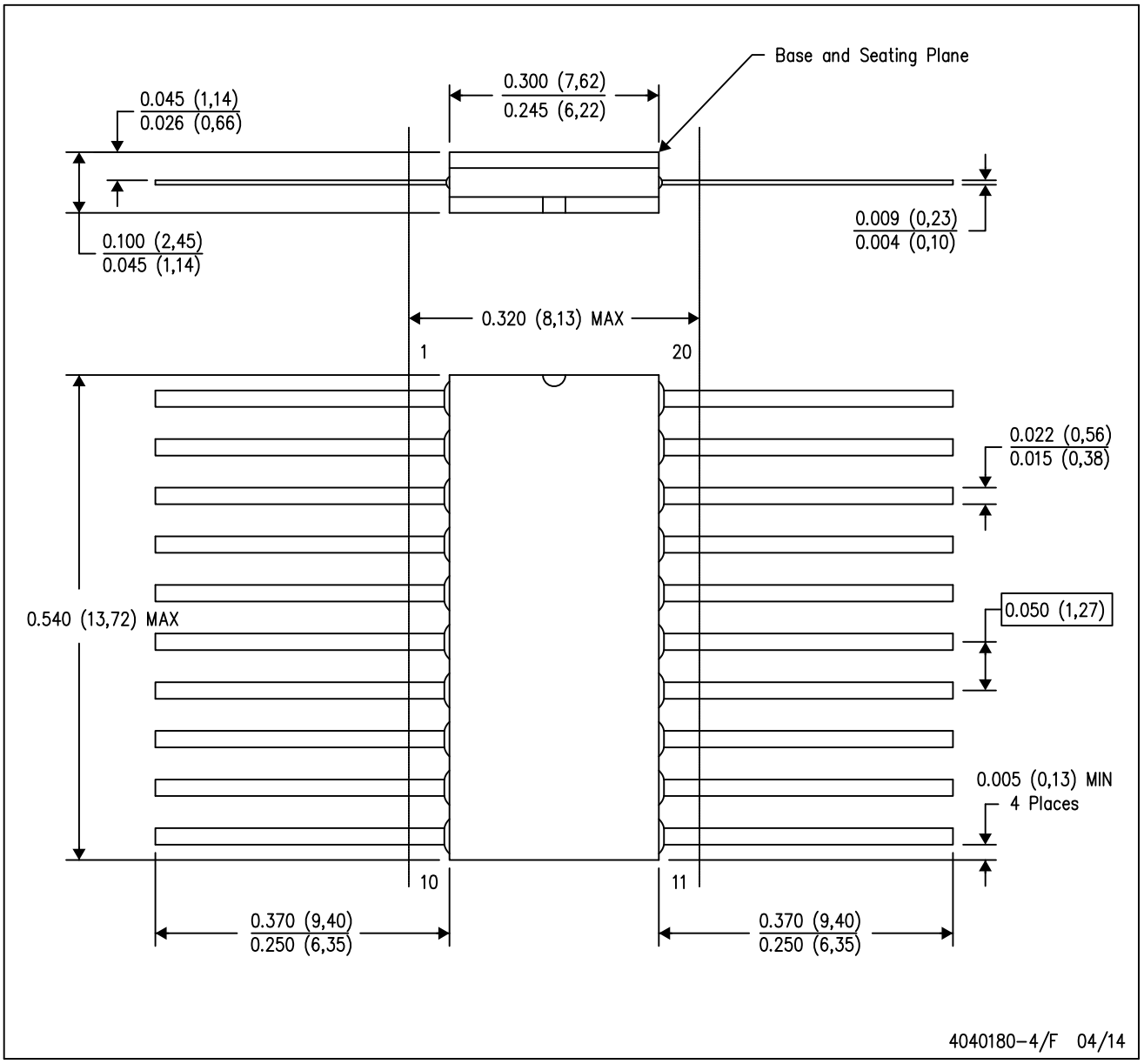

| DIM \ PINS ** | 14 | 16 | 18 | 20 |
|---|---|---|---|---|
| A | 0.300 (7,62) BSC | 0.300 (7,62) BSC | 0.300 (7,62) BSC | 0.300 (7,62) BSC |
| B MAX | 0.785 (19,94) | .840 (21,34) | 0.960 (24,38) | 1.060 (26,92) |
| B MIN | — | — | — | — |
| C MAX | 0.300 (7,62) | 0.300 (7,62) | 0.310 (7,87) | 0.300 (7,62) |
| C MIN | 0.245 (6,22) | 0.245 (6,22) | 0.220 (5,59) | 0.245 (6,22) |




4040083/F 03/03

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package is hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
E. Falls within MIL STD 1835 GDIP1–T14, GDIP1–T16, GDIP1–T18 and GDIP1–T20.

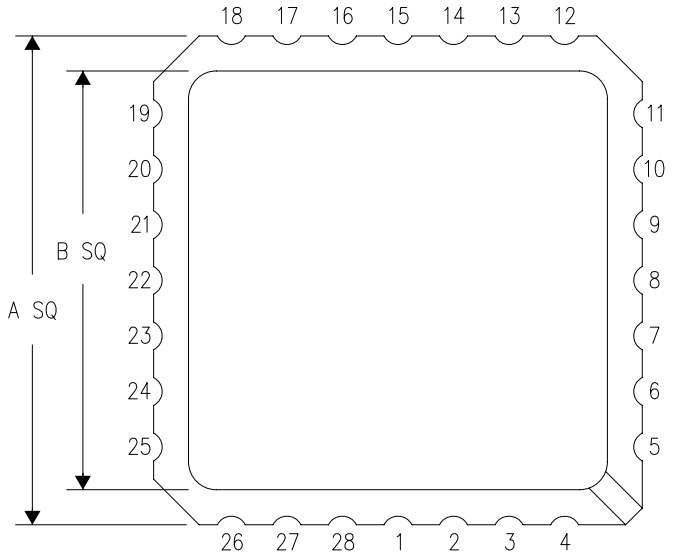
W (R–GDFP–F20) CERAMIC DUAL FLATPACK



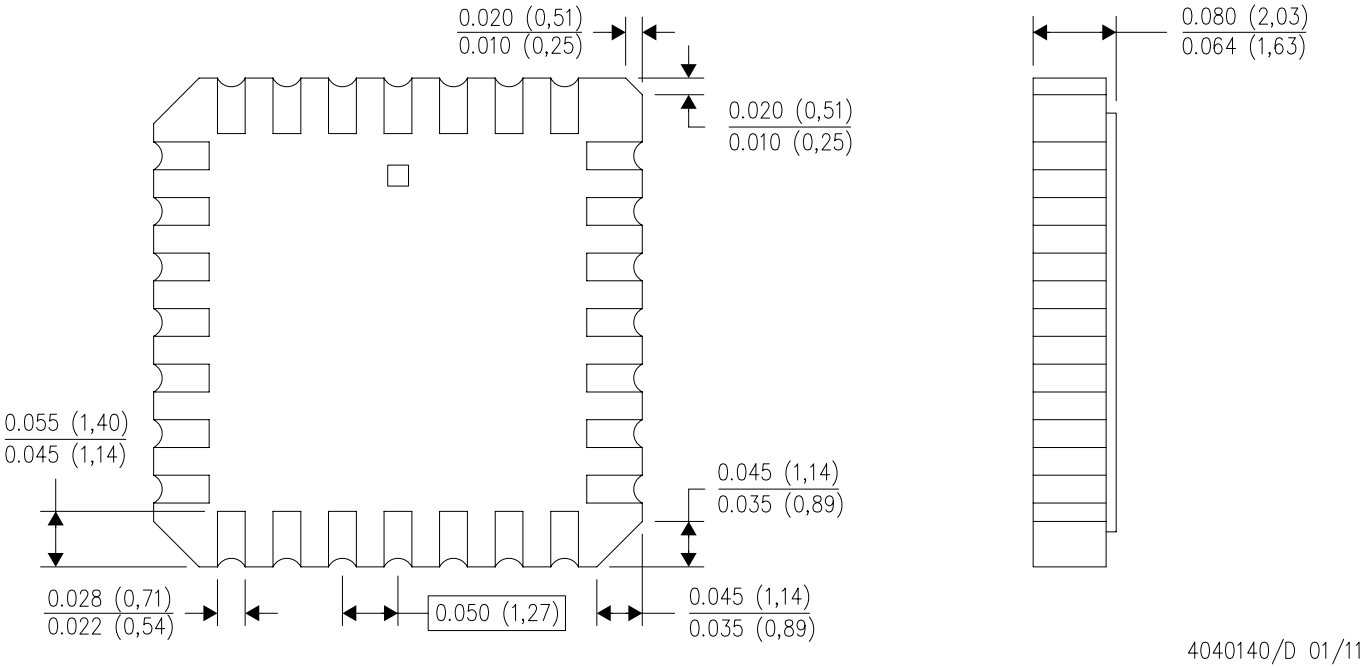

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only.
E. Falls within Mil–Std 1835 GDFP2–F20

FK (S–CQCC–N**) LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN



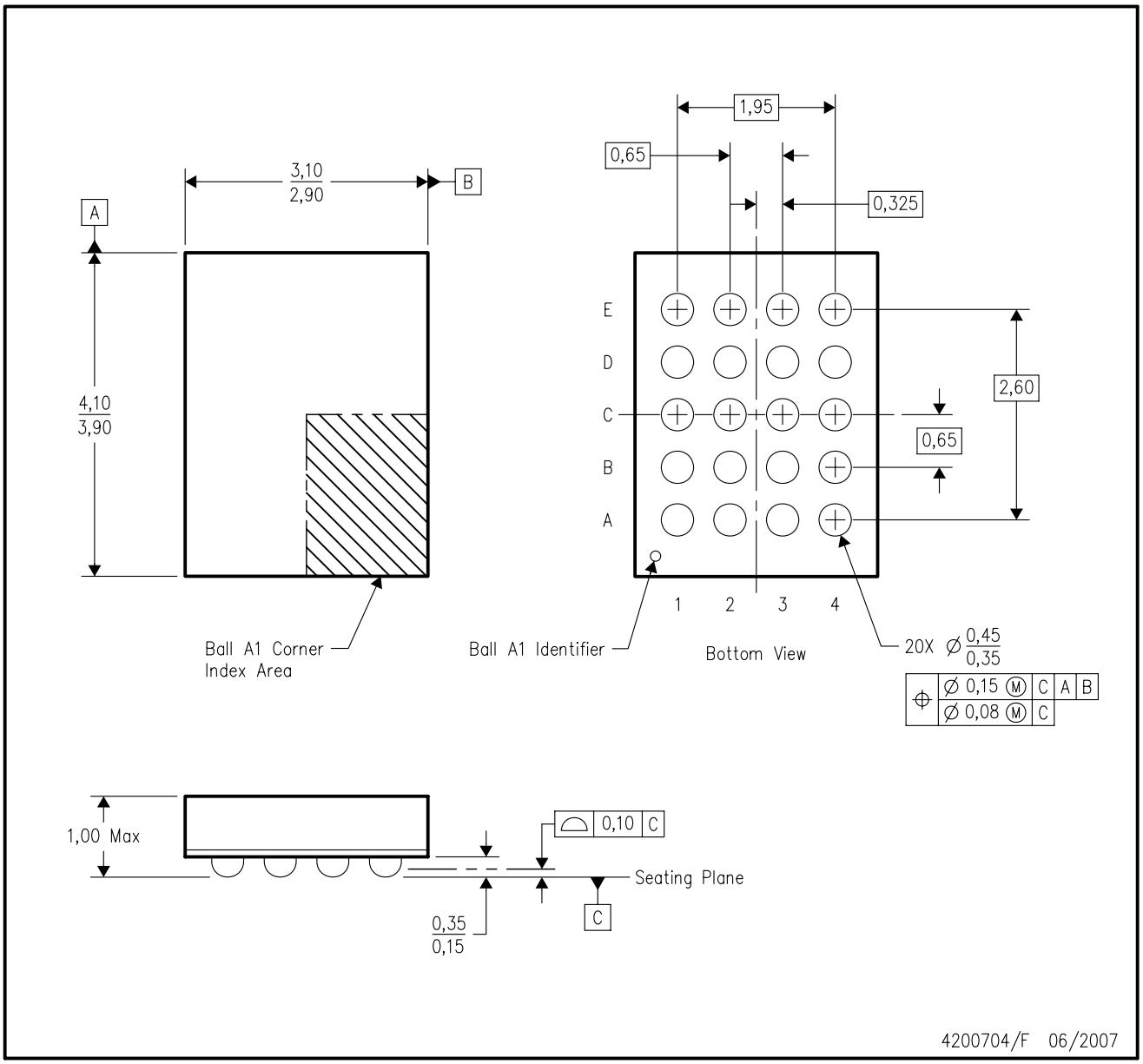

| NO. OF TERMINALS ** | A | | B | |
|---|---|---|---|---|
| | MIN | MAX | MIN | MAX |
| 20 | 0.342 (8,69) | 0.358 (9,09) | 0.307 (7,80) | 0.358 (9,09) |
| 28 | 0.442 (11,23) | 0.458 (11,63) | 0.406 (10,31) | 0.458 (11,63) |
| 44 | 0.640 (16,26) | 0.660 (16,76) | 0.495 (12,58) | 0.560 (14,22) |
| 52 | 0.740 (18,78) | 0.761 (19,32) | 0.495 (12,58) | 0.560 (14,22) |
| 68 | 0.938 (23,83) | 0.962 (24,43) | 0.850 (21,6) | 0.858 (21,8) |
| 84 | 1.141 (28,99) | 1.165 (29,59) | 1.047 (26,6) | 1.063 (27,0) |




4040140/D 01/11

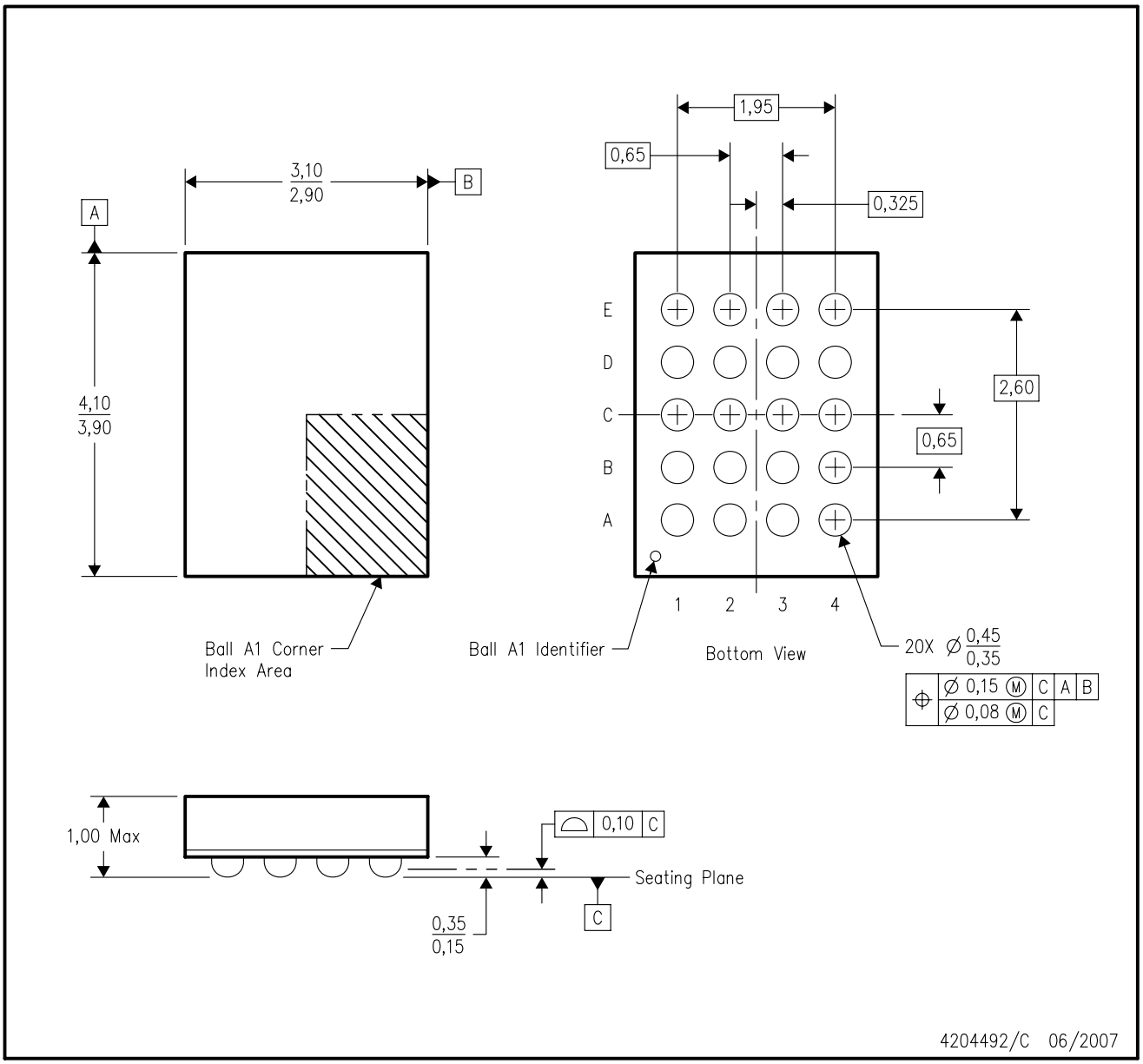
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a metal lid.
D. Falls within JEDEC MS–004

## GQN (R–PBGA–N20) PLASTIC BALL GRID ARRAY




NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Falls within JEDEC MO–285 variation BC–2.
D. This package is tin–lead (SnPb). Refer to the 20 ZQN package (drawing 4204492) for lead–free.

## ZQN (R–PBGA–N20) PLASTIC BALL GRID ARRAY

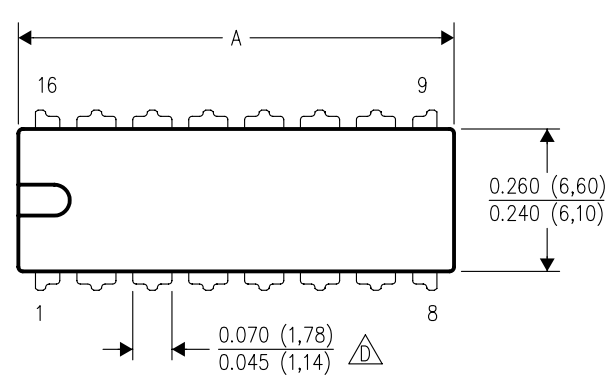



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Falls within JEDEC MO–285 variation BC–2.
D. This package is lead–free. Refer to the 20 GQN package (drawing 4200704) for tin–lead (SnPb).

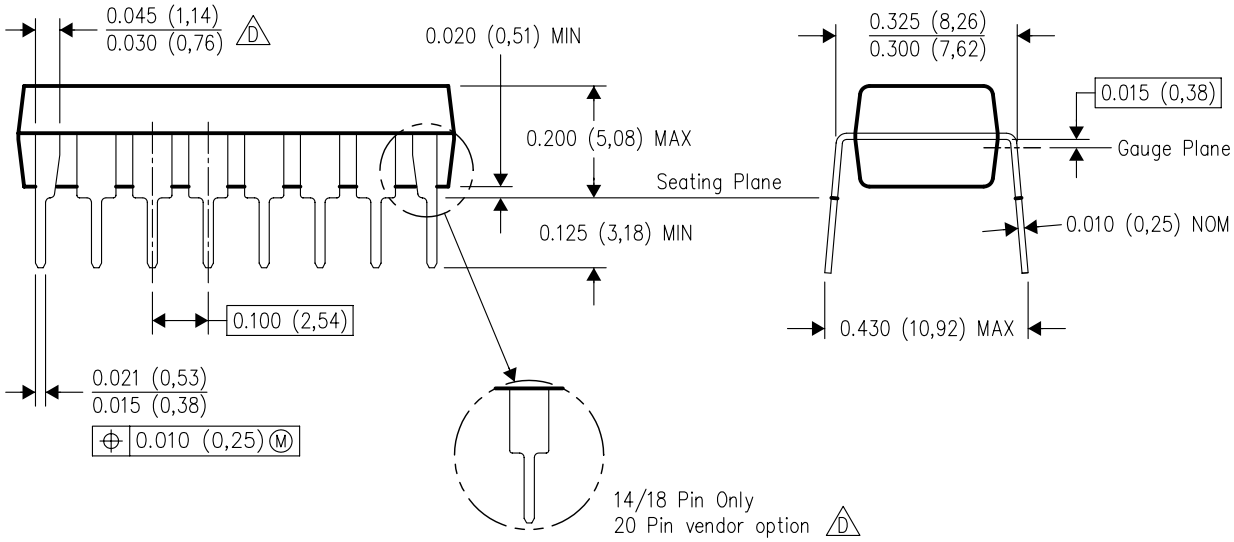
## N (R–PDIP–T**)

## PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN




| DIM \ PINS ** | 14 | 16 | 18 | 20 |
|---|---|---|---|---|
| A MAX | 0.775 (19,69) | 0.775 (19,69) | 0.920 (23,37) | 1.060 (26,92) |
| A MIN | 0.745 (18,92) | 0.745 (18,92) | 0.850 (21,59) | 0.940 (23,88) |
| MS–001 VARIATION (C) | AA | BB | AC | AD |

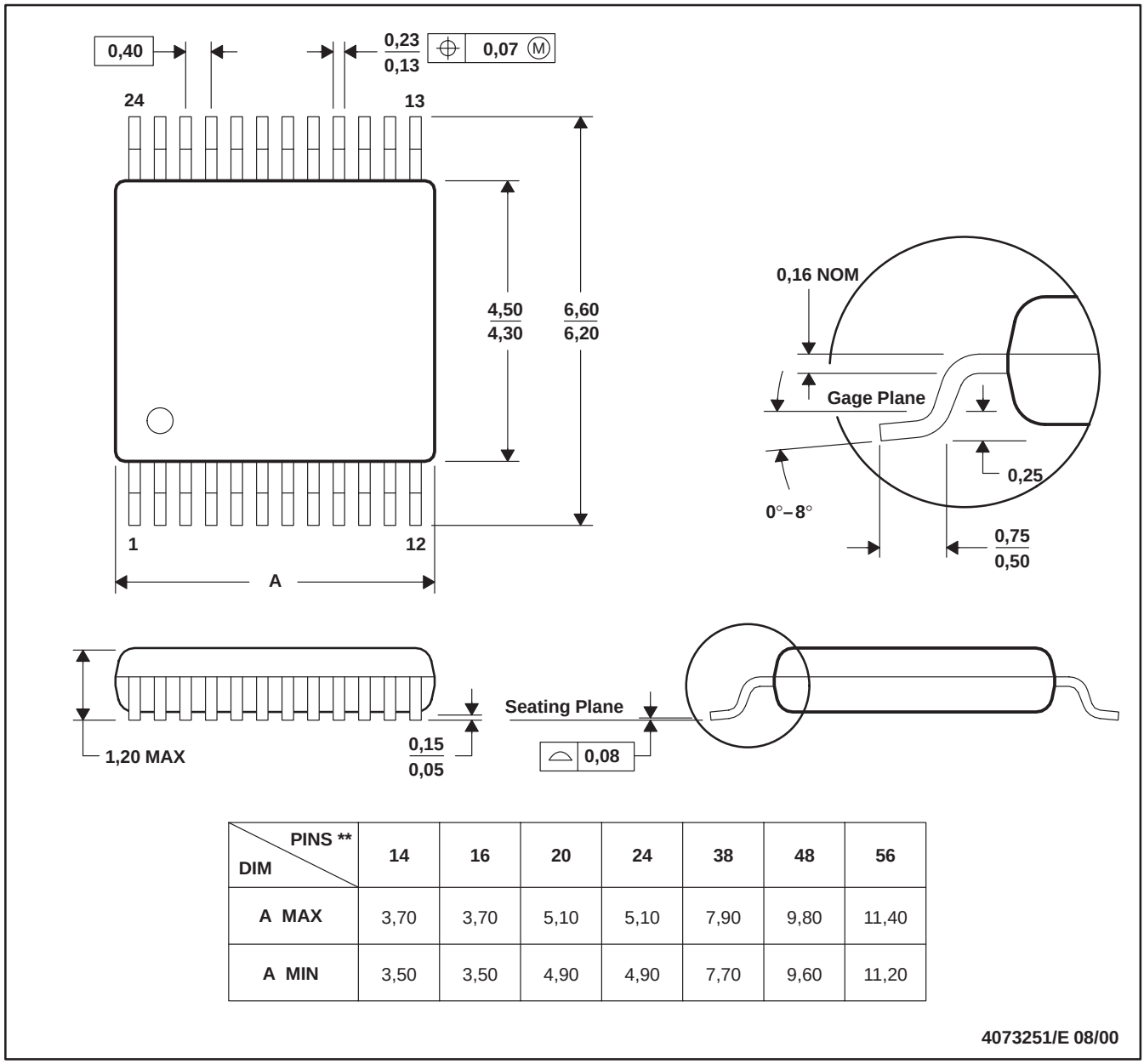



4040049/E 12/2002

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

**DGV (R-PDSO-G**)** **PLASTIC SMALL-OUTLINE**

**24 PINS SHOWN**

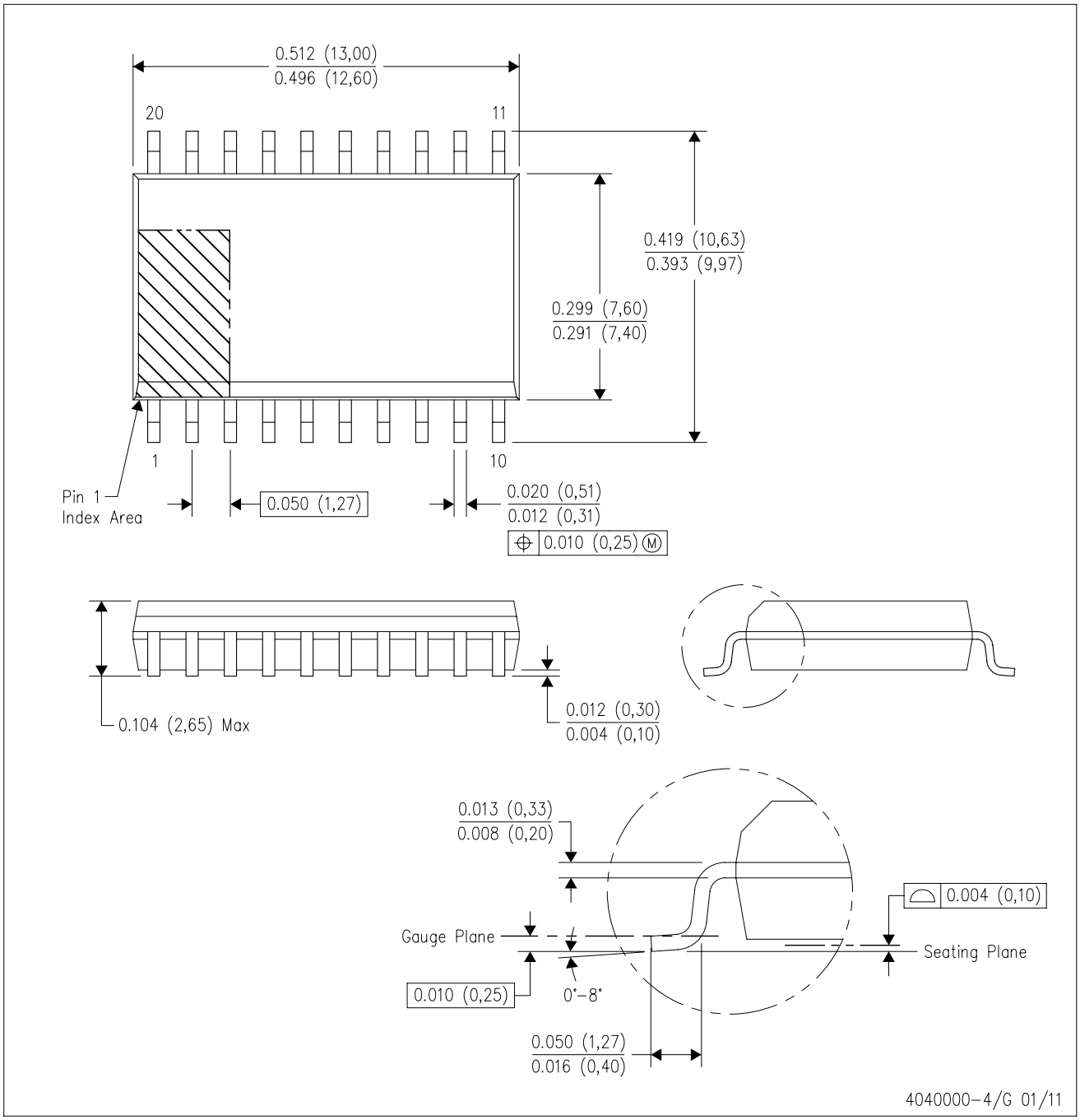



| DIM \ PINS ** | 14 | 16 | 20 | 24 | 38 | 48 | 56 |
|---|---|---|---|---|---|---|---|
| A MAX | 3,70 | 3,70 | 5,10 | 5,10 | 7,90 | 9,80 | 11,40 |
| A MIN | 3,50 | 3,50 | 4,90 | 4,90 | 7,70 | 9,60 | 11,20 |

**4073251/E 08/00**

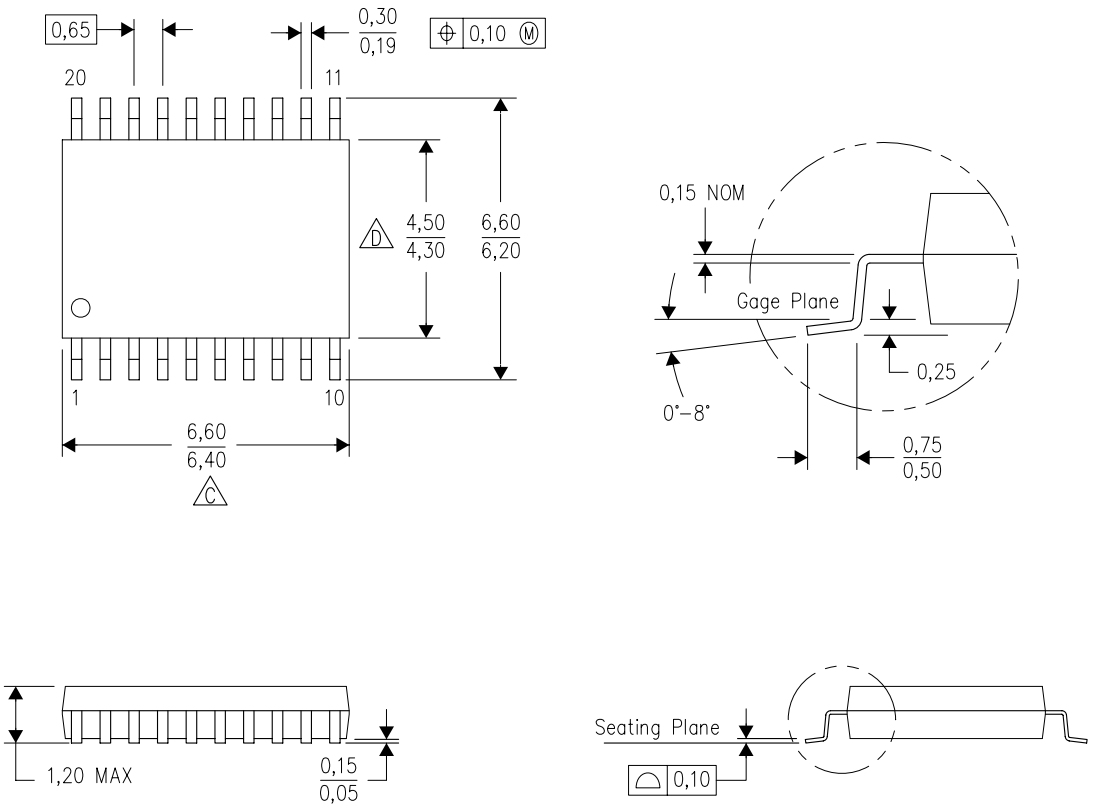
NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.
D. Falls within JEDEC: 24/48 Pins – MO-153
14/16/20/56 Pins – MO-194

DW (R–PDSO–G20) PLASTIC SMALL OUTLINE




NOTES:
A. All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
D. Falls within JEDEC MS–013 variation AC.

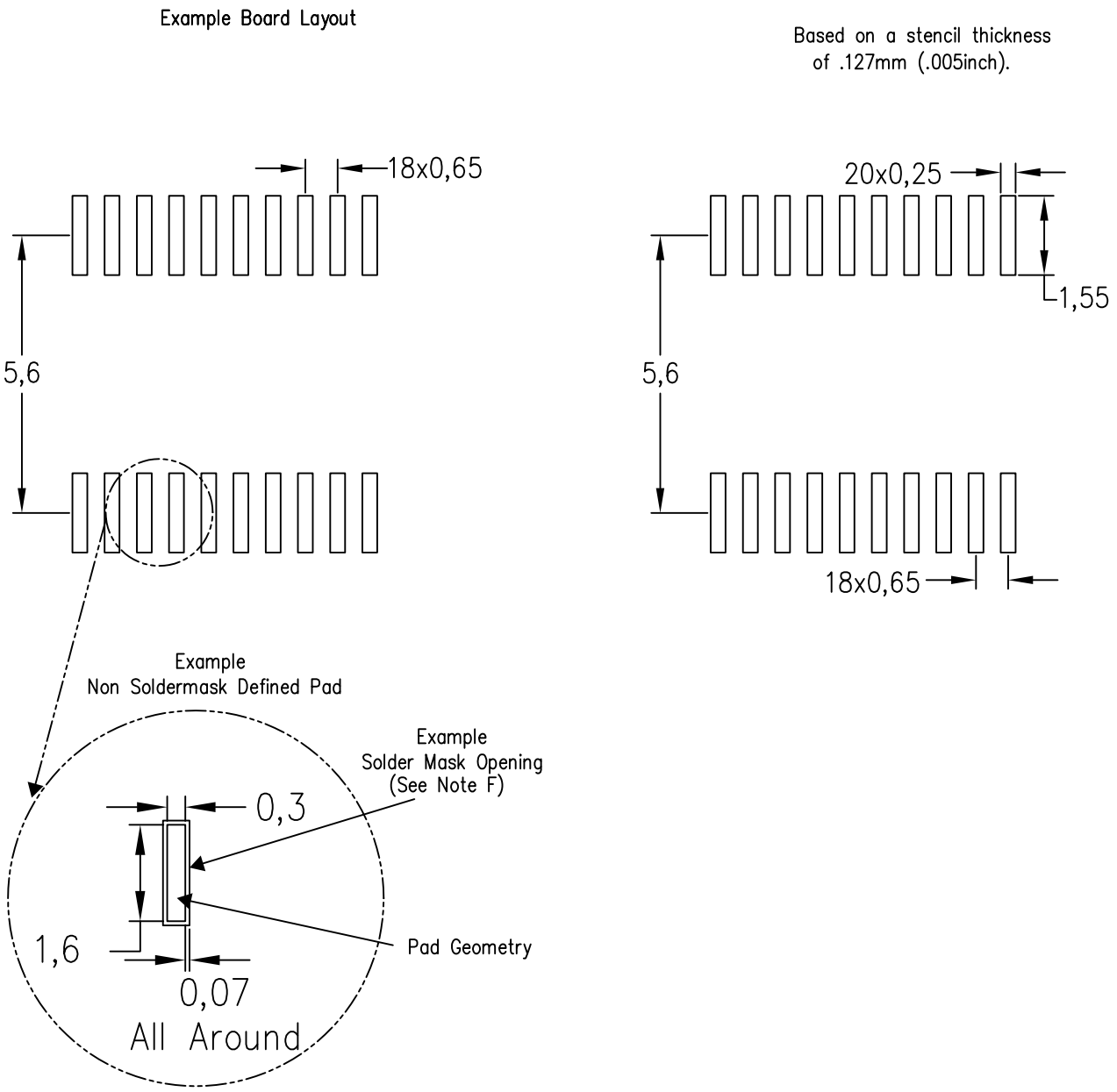
PW (R–PDSO–G20) PLASTIC SMALL OUTLINE




4040064–5/G 02/11

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
E. Falls within JEDEC MO–153

PW (R–PDSO–G20) PLASTIC SMALL OUTLINE




NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate design.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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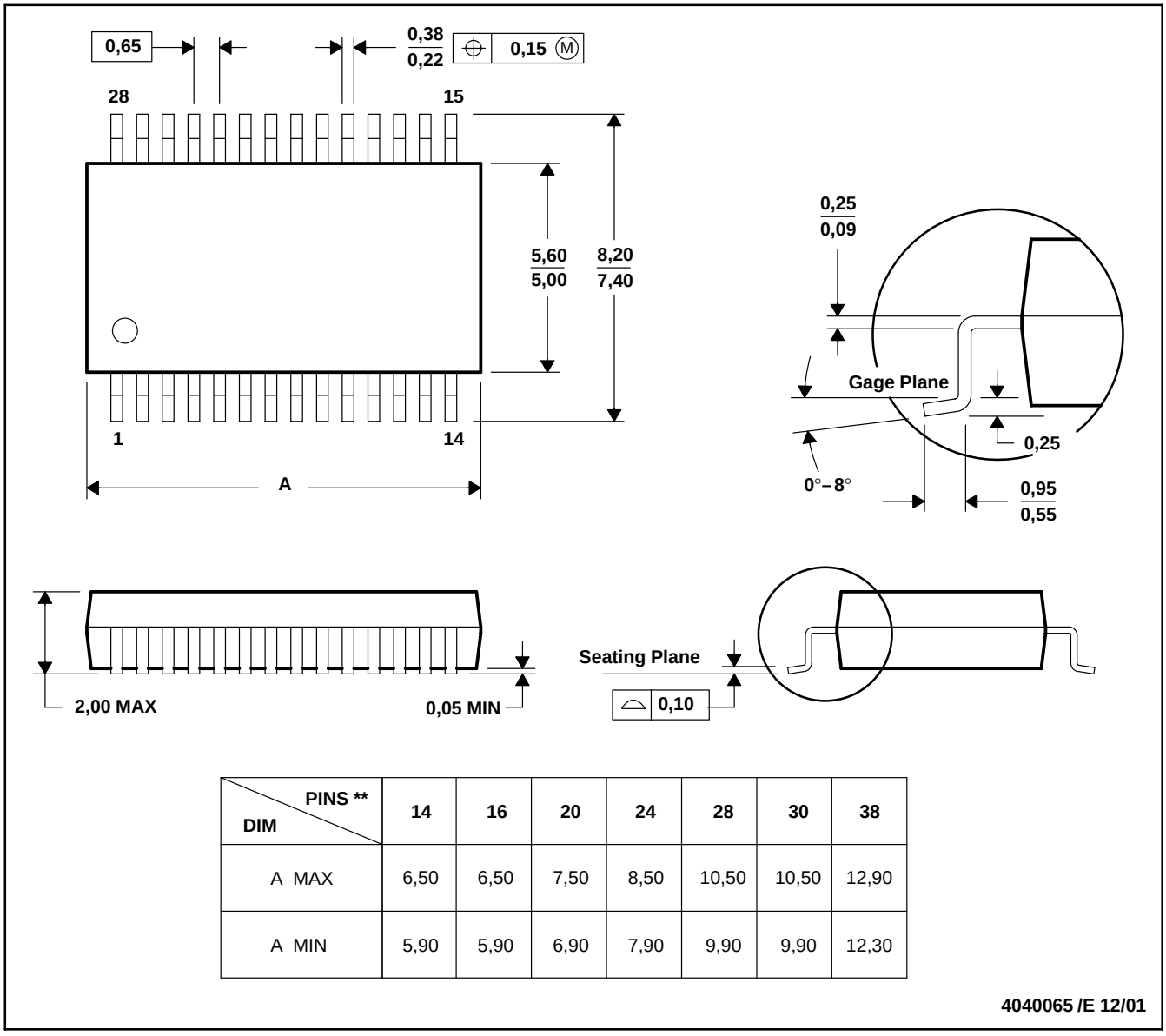
**DB (R-PDSO-G**)** **PLASTIC SMALL-OUTLINE**

**28 PINS SHOWN**

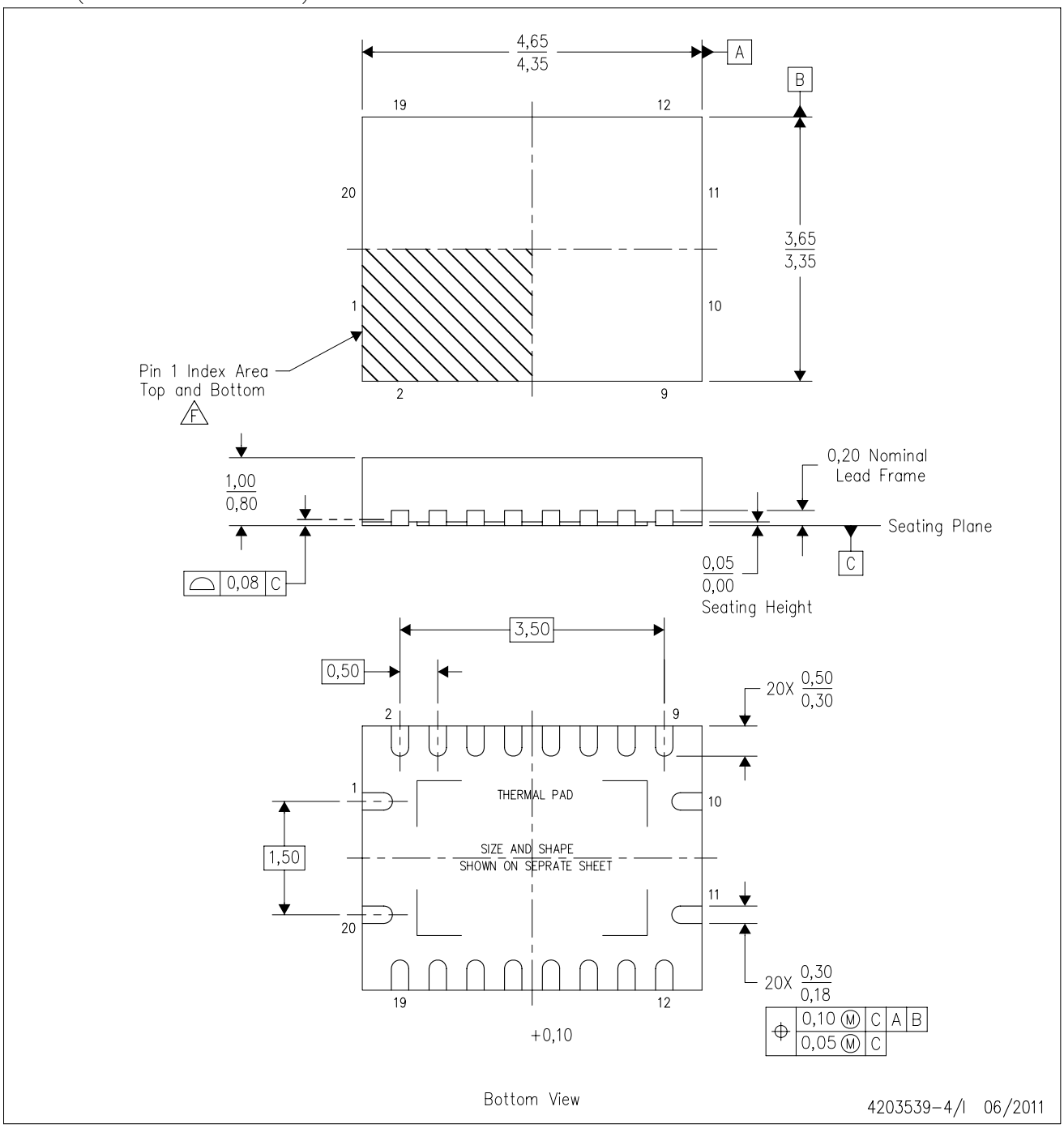



| DIM \ PINS ** | 14 | 16 | 20 | 24 | 28 | 30 | 38 |
|---|---|---|---|---|---|---|---|
| A MAX | 6,50 | 6,50 | 7,50 | 8,50 | 10,50 | 10,50 | 12,90 |
| A MIN | 5,90 | 5,90 | 6,90 | 7,90 | 9,90 | 9,90 | 12,30 |

**4040065 /E 12/01**

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. Falls within JEDEC MO-150

RGY (R–PVQFN–N20) PLASTIC QUAD FLATPACK NO–LEAD




NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. QFN (Quad Flatpack No–Lead) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Pin 1 identifiers are located on both top and bottom of the package and within the zone indicated. The Pin 1 identifiers are either a molded, marked, or metal feature.
G. Package complies to JEDEC MO–241 variation BA.

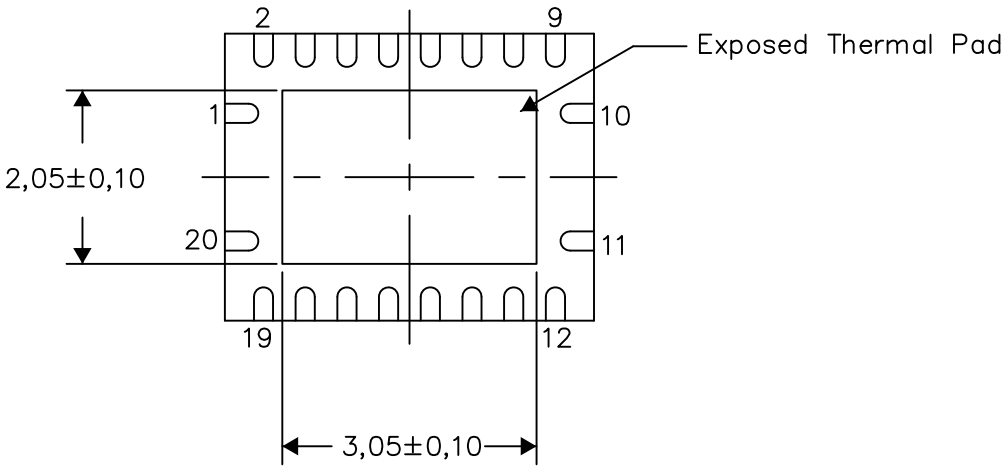
RGY (R–PVQFN–N20) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



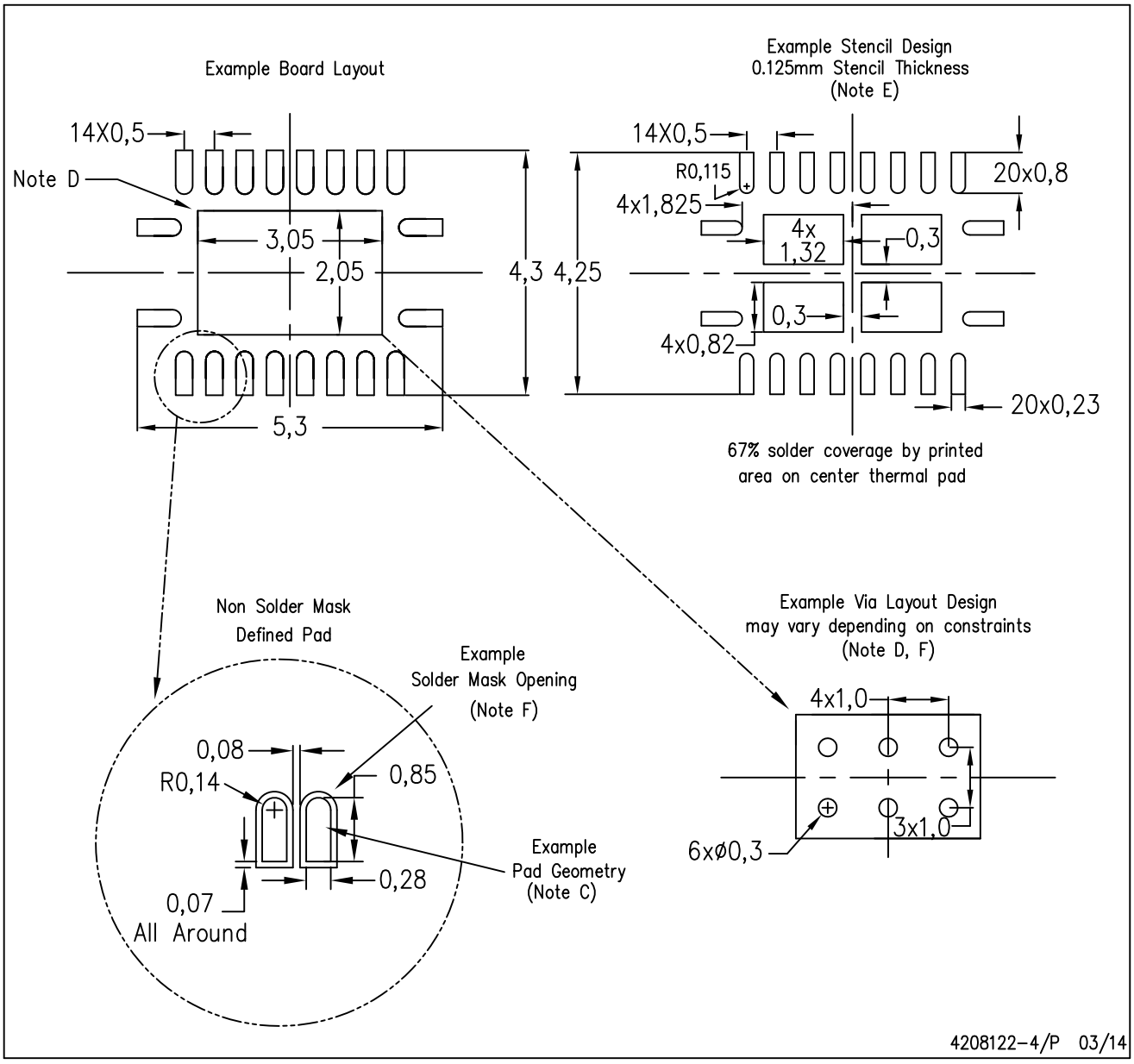

Bottom View

Exposed Thermal Pad Dimensions

4206353–4/P 03/14

NOTE: All linear dimensions are in millimeters

RGY (R–PVQFN–N20) PLASTIC QUAD FLATPACK NO–LEAD

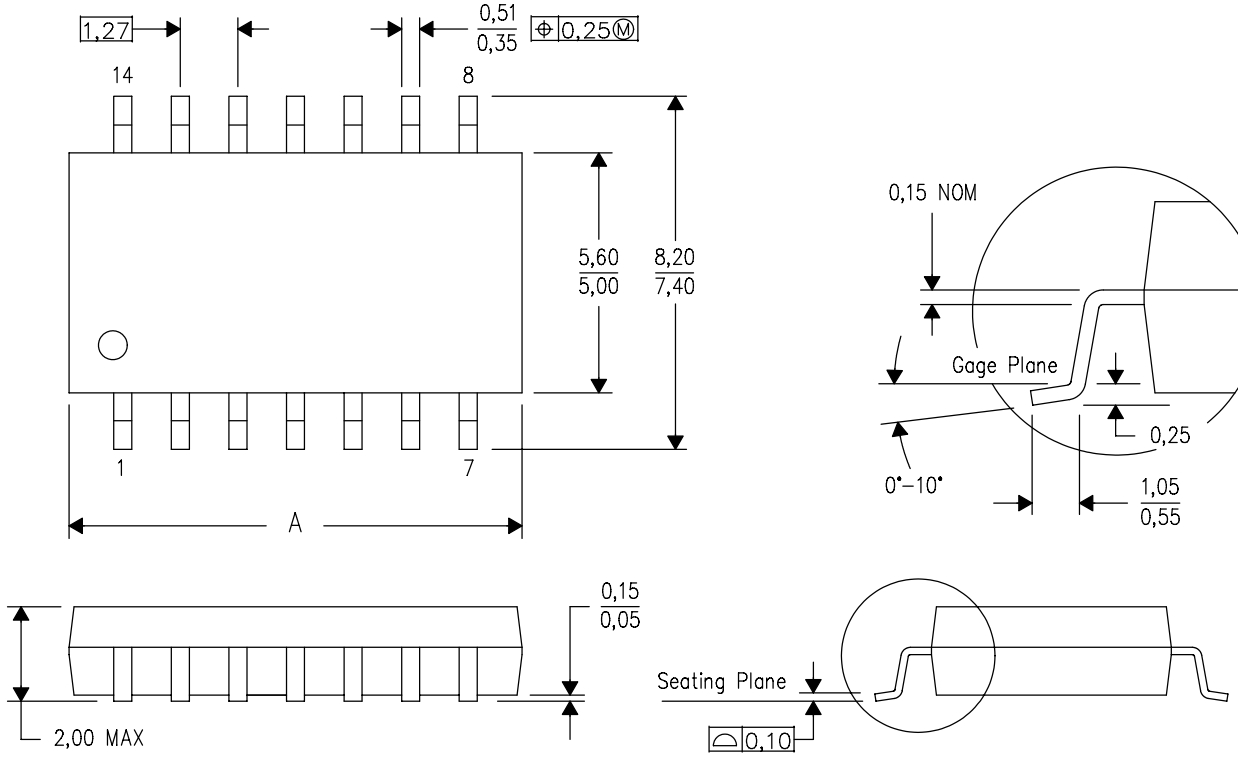



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http: //www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.

## MECHANICAL DATA

**NS (R-PDSO-G**)** **PLASTIC SMALL-OUTLINE PACKAGE**

**14-PINS SHOWN**




| DIM \ PINS ** | 14 | 16 | 20 | 24 |
|---|---|---|---|---|
| A MAX | 10,50 | 10,50 | 12,90 | 15,30 |
| A MIN | 9,90 | 9,90 | 12,30 | 14,70 |

4040062/C 03/03

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

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