

LME49721

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# LME49721 High-Performance, High-Fidelity Rail-to-Rail Input/Output Audio Operational Amplifier

Check for Samples: LME49721

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# FEATURES

- Rail-to-Rail Input and Output
- Easily Drives 10kΩ Loads to Within 10mV of Each Power Supply Voltage
- Optimized for Superior Audio Signal Fidelity
- Output Short Circuit Protection

# **APPLICATIONS**

- Ultra High-Quality Portable Audio Amplification
- High-Fidelity Preamplifiers
- High-Fidelity Multimedia
- State-of-the-Art Phono Pre Amps
- High-Performance Professional Audio
- High-Fidelity Equalization and Crossover Networks
- High-Performance Line Drivers
- High-Performance Line Receivers
- High-Fidelity Active Filters
- DAC I–V Converter
- ADC Front-End Signal Conditioning

### **KEY SPECIFICATIONS**

- Power Supply Voltage Range: 2.2V to 5.5V
- Quiescent Current: 2.15mA (typ)
- THD+N (A<sub>V</sub> = 2, V<sub>OUT</sub> =  $4V_{p-p}$ , f <sub>IN</sub> = 1kHz)
  - $R_{L} = 2k\Omega: 0.00008\%$  (typ)
  - $R_L = 600\Omega$ : 0.0001% (typ)
- Input Noise Density: 4nV/√Hz (typ), @ 1kHz
- Slew Rate: ±8.5V/µs (typ)
- Gain Bandwidth Product: 20MHz (typ)
- Open Loop Gain ( $R_L = 600\Omega$ ): 118dB (typ)
- Input Bias Current: 40fA (typ)
- Input Offset Voltage: 0.3mV (typ)
- PSRR: 103dB (typ)

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# DESCRIPTION

The LME49721 is a low-distortion, low-noise Rail-to-Rail Input/Output operational amplifier optimized and fully specified for high-performance, high-fidelity applications. Combining advanced leading-edge technology with state-of-the-art circuit process design, the LME49721 Rail-to-Rail Input/Output operational amplifier delivers superior signal amplification for outstanding performance. The LME49721 combines a very high slew rate with low THD+N to easily satisfy demanding applications. To ensure that the most challenging loads are driven without compromise, the LME49721 has a high slew rate of ±8.5V/µs and an output current capability of ±9.7mA. Further, dynamic range is maximized by an output stage that drives  $10k\Omega$  loads to within 10mV of either power supply voltage.

The LME49721 has a wide supply range of 2.2V to 5.5V. Over this supply range the LME49721's input circuitry maintains excellent common-mode and power supply rejection, as well as maintaining its low input bias current. The LME49721 is unity gain stable.

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# TYPICAL CONNECTION AND PINOUT





Figure 1. Buffer Amplifier



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

### ABSOLUTE MAXIMUM RATINGS<sup>(1)(2)(3)</sup>

Power Supply Voltage ( $V_S = V^+ - V^-$ )	6V
Storage Temperature	−65°C to 150°C
Input Voltage	(V-) - 0.7V to (V+) + 0.7V
Output Short Circuit <sup>(4)</sup>	Continuous
Power Dissipation	Internally Limited
ESD Rating <sup>(5)</sup>	2000V
ESD Rating <sup>(6)</sup>	200V
Junction Temperature	150°C
Thermal Resistance, $\theta_{JA}$ (SOIC)	165°C/W
Temperature Range, $T_{MIN} \le T_A \le T_{MAX}$	$-40^{\circ}C \le T_{A} \le 85^{\circ}C$
Supply Voltage Range	$2.2V \le V_{\rm S} \le 5.5V$

(1) "Absolute Maximum Ratings" indicate limits beyond which damage to the device may occur, including inoperability and degradation of device reliability and/or performance. Functional operation of the device and/or non-degradation at the Absolute Maximum Ratings or other conditions beyond those indicated in the Recommended Operating Conditions is not implied. The Recommended Operating Conditions indicate conditions at which the device is functional and the device should not be operated beyond such conditions. All voltages are measured with respect to the ground pin, unless otherwise specified

(2) The Electrical Characteristics table lists ensured specifications under the listed Recommended Operating Conditions except as otherwise modified or specified by the Electrical Characteristics Conditions and/or Notes. Typical specifications are estimations only and are not ensured.

- (3) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/Distributors for availability and specifications.
- (4) The maximum power dissipation must be derated at elevated temperatures and is dictated by T<sub>JMAX</sub>, θ<sub>JA</sub>, and the ambient temperature, T<sub>A</sub>. The maximum allowable power dissipation is P<sub>DMAX</sub> = (T<sub>JMAX</sub> T<sub>A</sub>) / θ<sub>JA</sub> or the number given in Absolute Maximum Ratings, whichever is lower.
- (5) Human body model, applicable std. JESD22-A114C.
- (6) Machine model, applicable std. JESD22-A115-A.



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# **ELECTRICAL CHARACTERISTICS FOR THE LME49721**

The following specifications apply for the circuit shown in Figure 1.  $V_S = 5V$ ,  $R_L = 10k\Omega$ ,  $R_{SOURCE} = 10\Omega$ ,  $f_{IN} = 1kHz$ , and  $T_A = 25^{\circ}C$ , unless otherwise specified.

Symbol	Parameter	Conditions	LME4	Units		
Oymbol	i aranieter	Conditions	Typical <sup>(1)</sup>	Limit <sup>(2)</sup>	(Limits)	
THD+N	Total Harmonic Distortion + Noise	$ \begin{array}{l} A_V = +1,  V_{OUT} = 2 V_{p\text{-}p}, \\ R_L = 2 k \Omega \\ R_L = 600 \Omega \end{array} $	0.0002 0.0002	0.001	% (max)	
IMD	Intermodulation Distortion	$A_V = +1$ , $V_{OUT} = 2V_{p-p}$ , Two-tone, 60Hz & 7kHz 4:1	0.0004		%	
GBWP	Gain Bandwidth Product		20	15	MHz (min)	
SR	Slew Rate	A <sub>V</sub> = +1	8.5		V/µs (min)	
FPBW	Full Power Bandwidth	$V_{OUT} = 1V_{P-P}, -3dB$ referenced to output magnitude at f = 1kHz	2.2		MHz	
t <sub>s</sub>	Settling time	A <sub>V</sub> = 1, 4V step 0.1% error range	800		ns	
2	Equivalent Input Noise Voltage	f <sub>BW</sub> = 20Hz to 20kHz, A-weighted	.707	1.13	μV <sub>P-P</sub> (max)	
e <sub>n</sub>	Equivalent Input Noise Density	f = 1kHz A-weighted	4	6	nV <b>/</b> √Hz (max)	
l <sub>n</sub>	Current Noise Density	f = 10kHz	4.0		fA <b>/</b> √Hz	
V <sub>OS</sub>	Offset Voltage		0.3	1.5	mV (max)	
$\Delta V_{OS} / \Delta Temp$	Average Input Offset Voltage Drift vs Temperature	40°C ≤ T <sub>A</sub> ≤ 85°C	1.1		µV/°C	
PSRR	Average Input Offset Voltage Shift vs Power Supply Voltage		103	85	dB (min)	
ISO <sub>CH-CH</sub>	Channel-to-Channel Isolation	f <sub>IN</sub> = 1kHz	117		dB	
I <sub>B</sub>	Input Bias Current	$V_{CM} = V_S/2$	40		fA	
ΔI <sub>OS</sub> /ΔTemp	Input Bias Current Drift vs Temperature	–40°C ≤ T <sub>A</sub> ≤ 85°C	48		fA/°C	
l <sub>os</sub>	Input Offset Current	$V_{CM} = V_S/2$	60		fA	
V <sub>IN-CM</sub>	Common-Mode Input Voltage Range			(V+) – 0.1 (V-) + 0.1	V (min)	
CMRR	Common-Mode Rejection	$V_{SS}$ - 100mV < $V_{CM}$ < $V_{DD}$ + 100mV	93	70	dB (min)	
	1/f Corner Frequency		2000		Hz	
		$V_{SS}$ - 200mV < $V_{OUT}$ < $V_{DD}$ + 200mV				
Δ	Open Loop Voltage Gain	$R_L = 600\Omega$	118	100	dB (min)	
A <sub>VOL</sub>	Open Loop Voltage Gain	$R_L = 2k\Omega$	122		dB (min)	
		$R_L = 10k\Omega$	130	115	dB (min)	
		$R_1 = 600\Omega$	$V_{DD} - 30 mV$	$V_{DD} - 80 mV$	V (min)	
M	Output Voltage Swing		$V_{SS}$ + 30mV	V <sub>SS</sub> + 80mV	V (min)	
V <sub>OUTMIN</sub>	Culput voltage Swing	$R_{L} = 10k\Omega, V_{S} = 5.0V$	$V_{DD} - 10 mV$	$V_{DD} - 20mV$	V (min)	
		11 - 10022, Vg - 5.0V	V <sub>SS</sub> + 10mV	V <sub>SS</sub> + 20mV	V (min)	
I <sub>OUT</sub>	Output Current	$R_L=250\Omega,  V_S=5.0V$	9.7	9.3	mA (min)	
I <sub>OUT-SC</sub>	Short Circuit Current		100		mA	
R <sub>OUT</sub>	Output Impedance	f <sub>IN</sub> = 10kHz Closed-Loop Open-Loop	0.01 46		Ω	
I <sub>S</sub>	Quiescent Current per Amplifier	I <sub>OUT</sub> = 0mA	2.15	3.25	mA (max)	

(1) Typical values represent most likely parametric norms at  $T_A = +25^{\circ}C$ , and at the Recommended Operation Conditions at the time of product characterization and are not ensured.

(2) Datasheet min/max specification limits are ensured by test or statistical analysis.

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#### TYPICAL PERFORMANCE CHARACTERISTICS

Graphs were taken in dual supply configuration.





4

2k

20k

FREQUENCY (Hz) Figure 8.

200

0.00001 L

20



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#### TYPICAL PERFORMANCE CHARACTERISTICS (continued)

Graphs were taken in dual supply configuration.





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## TYPICAL PERFORMANCE CHARACTERISTICS (continued)

Graphs were taken in dual supply configuration.





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0.1





TTH

2k

10k 20k

10k 20k

2k

10k 20k

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#### **TYPICAL PERFORMANCE CHARACTERISTICS (continued)**

2k



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# TYPICAL PERFORMANCE CHARACTERISTICS (continued)







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#### **TYPICAL PERFORMANCE CHARACTERISTICS (continued)**

Graphs were taken in dual supply configuration.













Output Voltage Swing Neg vs Power Supply  $R_L = 2k\Omega$ 







#### **TYPICAL PERFORMANCE CHARACTERISTICS (continued)**

Graphs were taken in dual supply configuration.

Output Voltage Swing Pos vs Power Supply  $R_L = 2k\Omega$ 



#### Figure 63.





Figure 65.

Supply Current per amplifier vs Power Supply  $R_L = 10k\Omega$ , Dual Supply





#### Figure 64.

Supply Current per amplifier vs Power Supply  $R_L = 2k\Omega$ , Dual Supply



#### Figure 66.

Supply Current per amplifier vs Power Supply  $R_L = 600\Omega$ , Dual Supply





## **APPLICATION INFORMATION**

#### DISTORTION MEASUREMENTS

The vanishingly low residual distortion produced by LME49721 is below the capabilities of all commercially available equipment. This makes distortion measurements just slightly more difficult than simply connecting a distortion meter to the amplifier's inputs and outputs. The solution. however, is quite simple: an additional resistor. Adding this resistor extends the resolution of the distortion measurement equipment.

The LME49721's low residual is an input referred internal error. As shown in Figure 69, adding the  $10\Omega$  resistor connected between a the amplifier's inverting and non-inverting inputs changes the amplifier's noise gain. The result is that the error signal (distortion) is amplified by a factor of 101. Although the amplifier's closed-loop gain is unaltered, the feedback available to correct distortion errors is reduced by 101. To ensure minimum effects on distortion measurements, keep the value of R1 low as shown in Figure 69.

This technique is verified by duplicating the measurements with high closed-loop gain and/or making the measurements at high frequencies. Doing so, produces distortion components that are within equipments capabilities. This datasheet's THD+N and IMD values were generated using the above described circuit connected to an Audio Precision System Two Cascade.



Figure 69. THD+N and IMD Distortion Test Circuit with  $A_V = 2$ 

#### OPERATING RATINGS AND BASIC DESIGN GUIDELINES

The LME49721 has a supply voltage range from  $\pm 2.2V$  to  $\pm 5.5V$  single supply or  $\pm 1.1$  to  $\pm 2.75V$  dual supply.

Bypassed capacitors for the supplies should be placed as close to the amplifier as possible. This will help minimize any inductance between the power supply and the supply pins. In addition to a  $10\mu$ F capacitor, a  $0.1\mu$ F capacitor is also recommended in CMOS amplifiers.

The amplifier's inputs lead lengths should also be as short as possible. If the op amp does not have a bypass capacitor, it may oscillate.

#### **BASIC AMPLIFIER CONFIGURATIONS**

The LME49721 may be operated with either a single supply or dual supplies. Figure 70 shows the typical connection for a single supply inverting amplifier. The output voltage for a single supply amplifier will be centered around the common-mode voltage Vcm. Note: the voltage applied to the Vcm insures the output stays above ground. Typically, the Vcm should be equal to  $V_{DD}/2$ . This is done by putting a resistor divider ckt at this node, see Figure 70.







Figure 70. Single-Supply Inverting Op Amp

Figure 71 shows the typical connection for a dual supply inverting amplifier. The output voltage is centered on zero.



Figure 71. Dual-Supply Inverting Op Amp

Figure 72 shows the typical connection for the Buffer Amplifier or also called a Voltage Follower. A Buffer Amplifier can be used to solve impedance matching problems, to reduce power consumption in the source, or to drive heavy loads. The input impedance of the op amp is very high. Therefore, the input of the op amp does not load down the source. The output impedance on the other hand is very low. It allows the load to either supply or absorb energy to a circuit while a secondary voltage source dissipates energy from a circuit. The Buffer is a unity stable amplifier, 1V/V. Although the feedback loop is tied from the output of the amplifier to the inverting input, the gain is still positive. Note: if a positive feedback is used, the amplifier will most likely drive to either rail at the output.



Figure 72. Buffer



#### **TYPICAL APPLICATIONS**



 $\begin{array}{l} A_V = 34.5 \\ F = 1 \ kHz \\ E_n = 0.38 \ \mu V \\ A \ Weighted \end{array}$ 

Figure 73. ANAB Preamp



Figure 74. NAB Preamp Voltage Gain vs Frequency



 $V_0 = V1 - V2$ 

Figure 75. Balanced to Single-Ended Converter



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$$V_0 = V1 + V2 - V3 - V4$$

Figure 76. Adder/Subtracter



 $f_0 = \frac{1}{2\pi RC}$ 





if C1 = C2 = C

$$R1 = \frac{\sqrt{2}}{2\omega_0 C}$$

 $R_2 = 2 \cdot R_1$ Illustration is  $f_0 = 1 \text{ kHz}$ 

Figure 78. Second-Order High-Pass Filter (Butterworth)





if R1 = R2 = R

$$C1 = \frac{\sqrt{2}}{\omega_0 R}$$
$$C2 = \frac{C1}{2}$$

Illustration is  $f_0 = 1 \text{ kHz}$ 





$$\begin{split} &f_{0}=\frac{1}{2\pi C1R1}, Q=\frac{1}{2}\left(1+\frac{R2}{R0}+\frac{R2}{RG}\right), A_{BP}=QA_{LP}=QA_{LH}=\frac{R2}{RG} \\ &IIIustration is \ f_{0}=1 \ kHz, \ Q=10, \ A_{BP}=1 \end{split}$$







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Figure 83. Line Driver











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Figure 86. Balanced Input Mic Amp



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A. See Table 1.

Figure 87. 10-Band Graphic Equalizer

Table 1. C <sub>1</sub> , C <sub>2</sub> , R <sub>1</sub> , and R <sub>2</sub> Values for Figure 87 <sup>(1)</sup>									
fo (Hz)	C <sub>1</sub>	C <sub>2</sub>	R <sub>1</sub>	R <sub>2</sub>					
32	0.12µF	4.7µF	75kΩ	500Ω					
64	0.056µF	3.3µF	68kΩ	510Ω					
125	0.033µF	1.5µF	62kΩ	510Ω					
250	0.015µF	0.82µF	68kΩ	470Ω					
500	8200pF	0.39µF	62kΩ	470Ω					
1k	3900pF	0.22µF	68kΩ	470Ω					
2k	2000pF	0.1µF	68kΩ	470Ω					
4k	1100pF	0.056µF	62kΩ	470Ω					

0.022µF

0.012µF

68kΩ

51kΩ

510Ω

510Ω

(1) At volume of change =  $\pm 12 \text{ dB}$  Q = 1.7

510pF

330pF

8k

16k



# **REVISION HISTORY**

Rev	Date	Description
1.0	09/26/07	Initial release.
1.1	10/01/07	Input more info under the Buffer Amplifier.
1.2	04/21/10	Added the Ordering Information table.
С	04/04/13	Changed layout of National Data Sheet to TI format.



12-Oct-2014

# **PACKAGING INFORMATION**

Orderable Device	Status	Package Type	Package	Pins	Package	Eco Plan	Lead/Ball Finish	MSL Peak Temp	Op Temp (°C)	Device Marking	Samples
	(1)		Drawing		Qty	(2)	(6)	(3)		(4/5)	
LME49721MA/NOPB	ACTIVE	SOIC	D	8	95	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	L49721 MA	Samples
LME49721MAX/NOPB	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	L49721 MA	Samples

<sup>(1)</sup> The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW**: Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

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the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

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<sup>(3)</sup> MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

<sup>(4)</sup> There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

<sup>(5)</sup> Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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# PACKAGE MATERIALS INFORMATION

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## TAPE AND REEL INFORMATION





# QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal	
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Device	Package Type	Package Drawing			Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LME49721MAX/NOPB	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1

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# PACKAGE MATERIALS INFORMATION

4-May-2017



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LME49721MAX/NOPB	SOIC	D	8	2500	367.0	367.0	35.0

D (R-PDSO-G8)

PLASTIC SMALL OUTLINE



NOTES: A. All linear dimensions are in inches (millimeters).

- B. This drawing is subject to change without notice.
- Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
- Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
- E. Reference JEDEC MS-012 variation AA.



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Designer will fully indemnify TI and its representatives against any damages, costs, losses, and/or liabilities arising out of Designer's noncompliance with the terms and provisions of this Notice.

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