

TPS3808Gxx-Q1 Low-Quiescent-Current Programmable-Delay Supervisory Circuit

1 Features

- Qualified for Automotive Applications
- Power-On Reset Generator With Adjustable Delay Time: 1.25 ms to 10 s
- Very Low Quiescent Current: 2.4 μ A Typical
- High Threshold Accuracy: 0.5% Typical
- Fixed Threshold Voltages for Standard Voltage Rails From 1.2 V to 5 V and Adjustable Voltage Down to 0.4 V Are Available
- Manual Reset ($\overline{\text{MR}}$) Input
- Open-Drain $\overline{\text{RESET}}$ Output
- Temperature Range: -40°C to $+125^{\circ}\text{C}$
- Small SOT-23 Package and WSON Package (TPS3808G01QDRVRQ1 only)

2 Applications

- DSP or Microcontroller Applications
- FPGA and ASIC Applications
- Automotive Vision
- Automotive Radar

3 Description

The TPS3808Gxx-Q1 microprocessor supervisory circuits monitor system voltages from 0.4 V to 5 V, asserting an open-drain $\overline{\text{RESET}}$ signal when the SENSE voltage drops below a preset threshold or when the manual reset ($\overline{\text{MR}}$) pin drops to a logic low. The $\overline{\text{RESET}}$ output remains low for the user-adjustable delay time after the SENSE voltage and $\overline{\text{MR}}$ return above their thresholds.

The TPS3808Gxx-Q1 device uses a precision reference to achieve 0.5% threshold accuracy for $V_{\text{IT}} \leq 3.3$ V. The reset delay time can be set to 20 ms by disconnecting the C_{T} pin, 300 ms by connecting the C_{T} pin to V_{DD} using a resistor, or can be user-adjusted from 1.25 ms to 10 s by connecting the C_{T} pin to an external capacitor. The TPS3808Gxx-Q1 has a very low typical quiescent current of 2.4 μ A, so it is well suited for battery-powered applications. The device is available in a small SOT-23 package (one option available in WSON) and is fully specified over a temperature range of -40°C to $+125^{\circ}\text{C}$ (T_{J}).

For more information about TI's voltage supervisor portfolio, visit the [Supervisor and Reset IC Overview Page](#).

Device Information⁽¹⁾

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPS3808Gxx-Q1	SOT-23 (6)	2.90 mm x 1.60 mm
	WSON (6)	2.00 mm x 2.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Typical Application Schematic

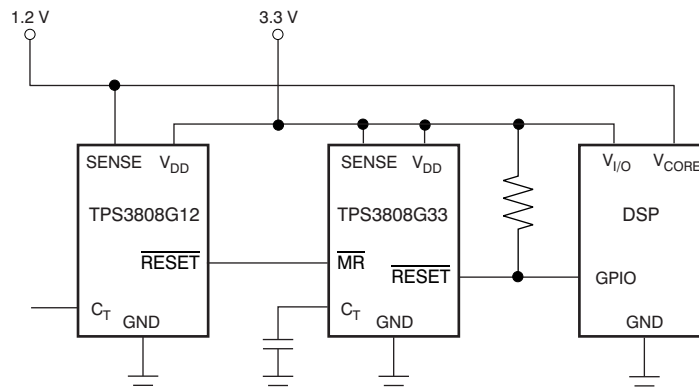


Table of Contents

1 Features	1	8.3 Feature Description	9
2 Applications	1	8.4 Device Functional Modes	11
3 Description	1	9 Applications and Implementation	12
4 Revision History	2	9.1 Application Information	12
5 Device Comparison Table	3	9.2 Typical Application	12
6 Pin Configuration and Functions	3	10 Power Supply Recommendations	14
7 Specifications	4	11 Layout	14
7.1 Absolute Maximum Ratings	4	11.1 Layout Guidelines	14
7.2 ESD Ratings	4	11.2 Layout Example	14
7.3 Recommended Operating Conditions	4	12 Device and Documentation Support	15
7.4 Thermal Information	5	12.1 Related Links	15
7.5 Electrical Characteristics	5	12.2 Receiving Notification of Documentation Updates	15
7.6 Timing Requirements	6	12.3 Community Resources	15
7.7 Typical Characteristics	7	12.4 Trademarks	15
8 Detailed Description	8	12.5 Electrostatic Discharge Caution	15
8.1 Overview	8	12.6 Glossary	15
8.2 Functional Block Diagrams	8	13 Mechanical, Packaging, and Orderable Information	15

4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision I (June 2015) to Revision J	Page
• Added column for WSON pins	3
• Changed unit for last row of t_d row in <i>Timing Requirements</i> from "ms" to "s" and "TYP" to "NOM" in middle unit column ...	6

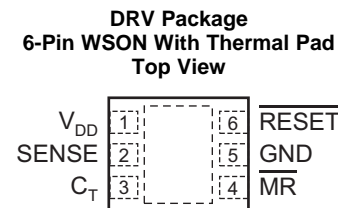
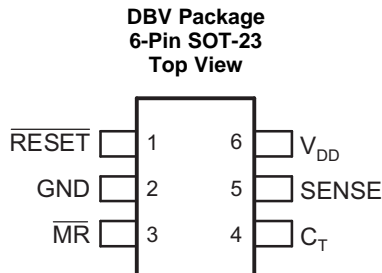
Changes from Revision H (June 2012) to Revision I	Page
• Added <i>ESD Ratings</i> table, <i>Feature Description</i> section, <i>Device Functional Modes</i> , <i>Application and Implementation</i> section, <i>Power Supply Recommendations</i> section, <i>Layout</i> section, <i>Device and Documentation Support</i> section, and <i>Mechanical, Packaging, and Orderable Information</i> section	1

Changes from Revision G (November, 2010) to Revision H	Page
• Changed I_{SENSE} from μA to nA	5

5 Device Comparison Table

ORDERABLE PART NUMBER	NOMINAL SUPPLY VOLTAGE	THRESHOLD VOLTAGE (V_{IT})
TPS3808G01QDRVRQ1	Adjustable	0.405 V
TPS3808G01QDBVRQ1		
TPS3808G12QDBVRQ1	1.2 V	1.12 V
TPS3808G125QDBVRQ1	1.25 V	1.16 V
TPS3808G15QDBVRQ1	1.5 V	1.4 V
TPS3808G18QDBVRQ1	1.8 V	1.67 V
TPS3808G30QDBVRQ1	3 V	2.79 V
TPS3808G33QDBVRQ1	3.3 V	3.07 V
TPS3808G50QDBVRQ1	5 V	4.65 V

6 Pin Configuration and Functions



Pin Functions

NAME	PIN		I/O	DESCRIPTION
	SOT-23	WSON		
C_T	4	3	I	Reset period programming pin. Connecting this pin to V_{DD} through a 40-k Ω to 200-k Ω resistor or leaving it open results in fixed delay times (see Electrical Characteristics). Connecting this pin to a ground referenced capacitor ≥ 100 pF gives user-programmable delay time. See the Selecting the Reset Delay Time for more information.
GND	2	5	—	Ground
\overline{MR}	3	4	I	Manual reset. Driving this pin low asserts \overline{RESET} . \overline{MR} is internally tied to V_{DD} by a 90-k Ω pullup resistor.
\overline{RESET}	1	6	O	Reset. This is an open-drain output that is driven to a low impedance state when \overline{RESET} is asserted (either the SENSE input is lower than the threshold voltage (V_{IT}) or the MR pin is set to a logic low). \overline{RESET} remains low (asserted) for the reset period after both SENSE is above V_{IT} and \overline{MR} is set to a logic high. A pullup resistor from 10 k Ω to 1 M Ω must be used on this pin and allows the reset pin to attain voltages higher than V_{DD} .
SENSE	5	2	I	Voltage sense. This pin is connected to the voltage to be monitored. If the voltage at this terminal drops below the threshold voltage (V_{IT}), \overline{RESET} is asserted.
V_{DD}	6	1	I	Supply voltage. It is good analog design practice to place a 0.1- μ F ceramic capacitor close to this pin.
Thermal Pad	—	Pad	—	Thermal pad; connect to ground plan to enhance thermal performance of the package.

7 Specifications

7.1 Absolute Maximum Ratings

over operating junction temperature range (unless otherwise noted)⁽¹⁾

		MIN	MAX	UNIT
V _{DD}	Input voltage	-0.3	7	V
V _{CT}	C _T voltage	-0.3	(V _{DD} + 0.3)	V
V _{MR} , V _{RESET} , V _{SENSE}	$\overline{\text{MR}}$, $\overline{\text{RESET}}$, SENSE voltage	-0.3	7	V
I _{RESET}	$\overline{\text{RESET}}$ pin current		5	mA
T _J	Operating junction temperature ⁽²⁾	-40	150	°C
T _{stg}	Storage temperature	-65	150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under the *Electric Characteristics* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) Due to the low dissipated power in this device, it is assumed that T_J = T_A.

7.2 ESD Ratings

		VALUE	UNIT
TPS3808G125QDBVRQ1 IN SOT-23 PACKAGE			
V _(ESD)	Electrostatic discharge	Human body model (HBM), per AEC Q100-002 ⁽¹⁾	±2000
		Charged device model (CDM), per AEC Q100-011	±1000
		Machine Model (MM)	±50
TPS3808GXX-Q1 IN SOT-23 PACKAGE			
V _(ESD)	Electrostatic discharge	Human body model (HBM), per AEC Q100-002 ⁽¹⁾	±2000
		Charged device model (CDM), per AEC Q100-011	±500
TPS3808G01QDRVRQ1 IN SON PACKAGE			
V _(ESD)	Electrostatic discharge	Human body model (HBM), per AEC Q100-002 ⁽¹⁾	±2000
		Charged device model (CDM), per AEC Q100-011	±500
		Machine Model (MM)	±50

- (1) AEC Q100-002 indicates HBM stressing is done in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

	MIN	NOM	MAX	UNIT
V _{DD} input supply	1.8		6.5	V
V _{SENSE} SENSE pin voltage	0		V _{DD}	V
$\overline{\text{MR}}$ Manual reset pin voltage	0		V _{DD}	V

7.4 Thermal Information

THERMAL METRIC ⁽¹⁾		TPS3808Gxx-Q1		UNIT
		DBV (SOT-23)	DRV (WSON)	
		6 PINS	6 PINS	
R _{θJA}	Junction-to-ambient thermal resistance	180.9	178.1	°C/W
R _{θJC(top)}	Junction-to-case (top) thermal resistance	117.8	95.6	°C/W
R _{θJB}	Junction-to-board thermal resistance	27.8	135	°C/W
ψ _{JT}	Junction-to-top characterization parameter	18.9	6.3	°C/W
ψ _{JB}	Junction-to-board characterization parameter	27.3	136.6	°C/W
R _{θJC(bot)}	Junction-to-case (bottom) thermal resistance	N/A	7.3	°C/W

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

7.5 Electrical Characteristics

1.8 V ≤ V_{DD} ≤ 6.5 V, R_{LRESET} = 100 kΩ, C_{LRESET} = 50 pF, over operating temperature range (T_J = –40°C to +125°C) (unless otherwise noted), typical values at T_J = 25°C

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT		
V _{DD}	Input supply range	1.8		6.5	V		
I _{DD}	Supply current (into V _{DD} pin)	V _{DD} = 3.3 V, $\overline{\text{RESET}}$ not asserted, MR, $\overline{\text{RESET}}$, C _T open		2.4	5	μA	
		V _{DD} = 6.5 V, $\overline{\text{RESET}}$ not asserted, MR, $\overline{\text{RESET}}$, C _T open		2.7	6		
V _{OL}	Low-level output voltage	1.3 V ≤ V _{DD} < 1.8 V, I _{OL} = 0.4 mA			0.3	V	
		1.8 V ≤ V _{DD} ≤ 6.5 V, I _{OL} = 1 mA			0.4		
	Power-up reset voltage ⁽¹⁾	V _{OL} (max) = 0.2 V, I _{$\overline{\text{RESET}}$} = 15 μA			0.8	V	
V _{IT}	Negative-going input threshold accuracy	TPS3808G01-Q1		–2%	±1%	2%	
		V _{IT} ≤ 3.3 V		–1.5%	±0.5%	1.5%	
		3.3 V < V _{IT} ≤ 5 V		–2%	±1%	2%	
		–40°C < T _J < 85°C		–1.25%	±0.5%	1.25%	
V _{HYS}	Hysteresis on V _{IT} pin	TPS3808G01-Q1			1.5	3	%V _{IT}
		–40°C < T _J < 85°C			1	2	
					1	2.5	
R _{$\overline{\text{MR}}$}	$\overline{\text{MR}}$ internal pullup resistance	V _{SENSE} = V _{IT}		70	90	kΩ	
I _{SENSE}	Input current at SENSE pin	TPS3808G01-Q1		–25	25	nA	
		V _{SENSE} = 6.5 V			1.7	μA	
I _{OH}	$\overline{\text{RESET}}$ leakage current	V _{$\overline{\text{RESET}}$} = 6.5 V, $\overline{\text{RESET}}$ not asserted			300	nA	
C _{IN}	Input capacitance, any pin	C _T pin	V _{IN} = 0 V to V _{DD}		5	pF	
		Other pins	V _{IN} = 0 V to 6.5 V		5		
V _{IL}	$\overline{\text{MR}}$ logic low input				0	0.3 V _{DD}	V
V _{IH}	$\overline{\text{MR}}$ logic high input				0.7 V _{DD}	V _{DD}	V

(1) Power-up reset voltage is the lowest supply voltage (V_{DD}) at which $\overline{\text{RESET}}$ becomes active (t_{rise(VDD)} ≥ 15 μs/V).

7.6 Timing Requirements

				MIN	NOM	MAX	UNIT
t_d	$\overline{\text{RESET}}$ delay time	$C_T = \text{Open}$	See Figure 1	12	20	28	ms
		$C_T = V_{DD}$		180	300	420	
		$C_T = 100 \text{ pF}$		0.75	1.25	1.75	
		$C_T = 180 \text{ nF}$		0.7	1.2	1.7	s
t_{pHL}	Propagation delay	$\overline{\text{MR}}$ to $\overline{\text{RESET}}$	$V_{IH} = 0.7 V_{DD}, V_{IL} = 0.3 V_{DD}$	150			ns
	High-level to low-level $\overline{\text{RESET}}$ delay	$\overline{\text{SENSE}}$ to $\overline{\text{RESET}}$	$V_{IH} = 1.05 V_{IT}, V_{IL} = 0.95 V_{IT}$	20			μs
t_w	Maximum transient duration	$\overline{\text{SENSE}}$	$V_{IH} = 1.05 V_{IT}, V_{IL} = 0.95 V_{IT}$	20			μs
		$\overline{\text{MR}}$	$V_{IH} = 0.7 V_{DD}, V_{IL} = 0.3 V_{DD}$	0.001			

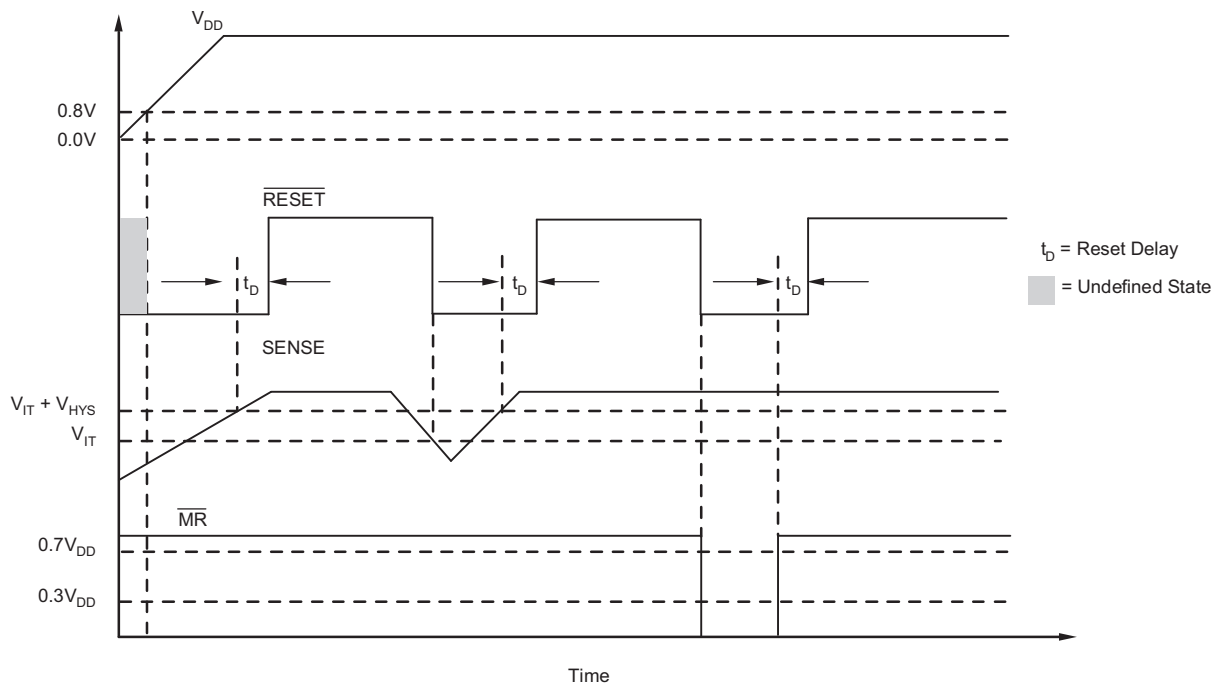


Figure 1. $\overline{\text{MR}}$ and $\overline{\text{SENSE}}$ Reset Timing Diagram

7.7 Typical Characteristics

At $T_J = 25^\circ\text{C}$, $V_{DD} = 3.3\text{ V}$, $R_{L\text{RESET}} = 100\text{ k}\Omega$, and $C_{L\text{RESET}} = 50\text{ pF}$ (unless otherwise noted)

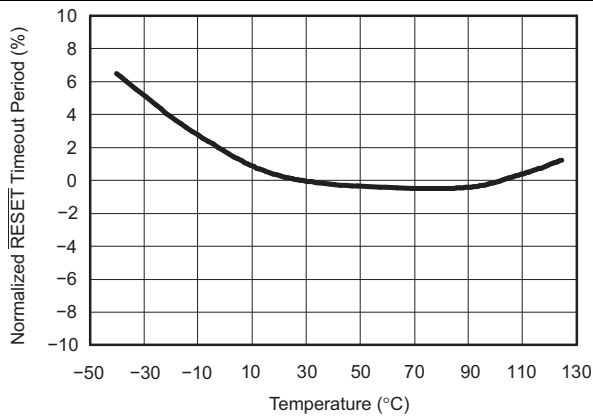


Figure 2. Normalized $\overline{\text{RESET}}$ Time-out Period vs Temperature ($C_T = \text{Open}$, $C_T = V_{DD}$, $C_T = \text{Any}$)

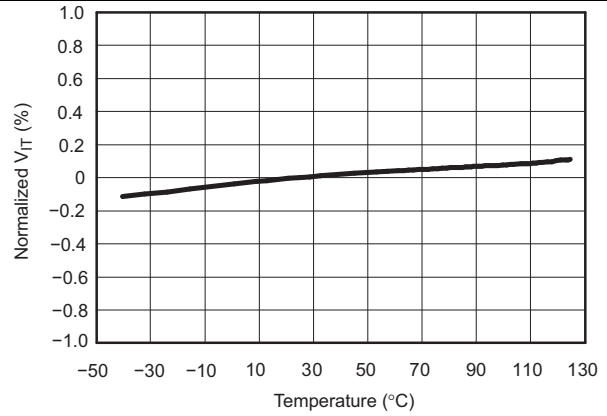


Figure 3. Normalized Sense Threshold Voltage (V_{IT}) vs Temperature

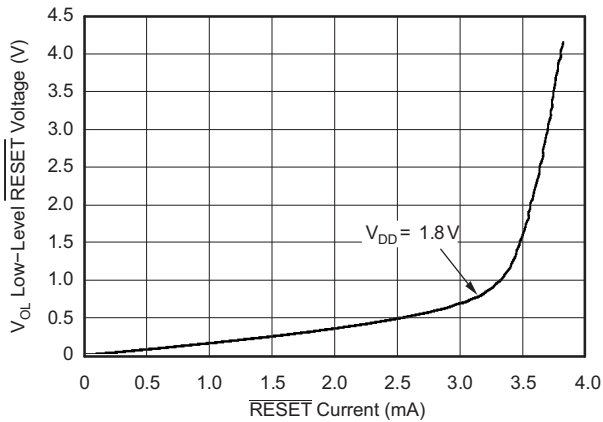


Figure 4. Low-Level $\overline{\text{RESET}}$ Voltage vs $\overline{\text{RESET}}$ Current

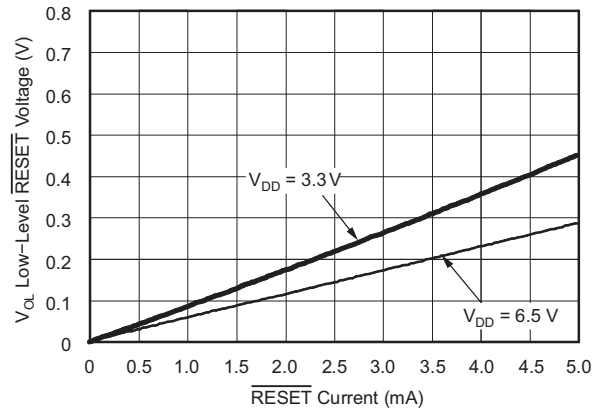


Figure 5. Low-Level $\overline{\text{RESET}}$ Voltage vs $\overline{\text{RESET}}$ Current

8 Detailed Description

8.1 Overview

The TPS3808Gxx-Q1 devices are low-current supervisory circuits used to monitor system voltages ranging from 0.4 V to 5 V. The devices assert an active low, open-drain $\overline{\text{RESET}}$ signal when the $\overline{\text{SENSE}}$ voltage drops below a preset threshold or when the manual reset ($\overline{\text{MR}}$) pin is asserted to a logic low. The $\overline{\text{RESET}}$ output remains low for the user-adjustable delay time after the $\overline{\text{SENSE}}$ voltage and $\overline{\text{MR}}$ return above their thresholds. The devices are also designed to be immune to short negative transients on the $\overline{\text{SENSE}}$ pin. The reset delay time can be configured by using the C_T pin. The delay can be configured to 20 ms by leaving the C_T pin floating, it can be configured to 300 ms by connecting the C_T pin to V_{DD} using a resistor, or can be configured from 1.25 ms to 10 s by connecting the C_T pin to an external capacitor.

8.2 Functional Block Diagrams

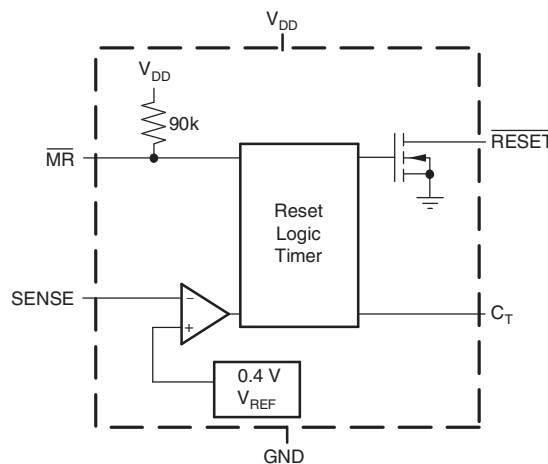


Figure 6. Adjustable-Voltage Version

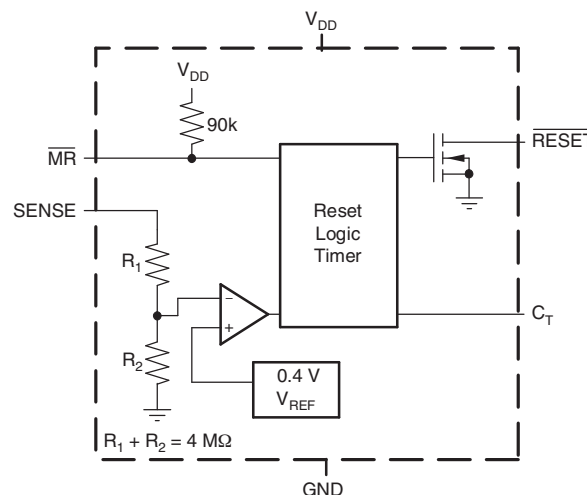


Figure 7. Fixed-Voltage Version

8.3 Feature Description

8.3.1 Immunity to SENSE Pin Voltage Transients

The TPS3808Gxx-Q1 is relatively immune to short negative transients on the SENSE pin. Sensitivity to transients is dependent on threshold overdrive, as shown in the *Maximum Transient Duration at Sense vs Sense Threshold Overdrive Voltage* graph (Figure 9). This graph shows the duration that the transient is below V_{IT} compared to the magnitude of the voltage drop below V_{IT} , or overdrive voltage. The overdrive voltage is expressed as a percentage of the V_{IT} threshold value. Any combination of transient duration and overdrive voltage that lies above the curve results in $\overline{\text{RESET}}$ being asserted low. Any transient that lies below the curve is ignored by the device.

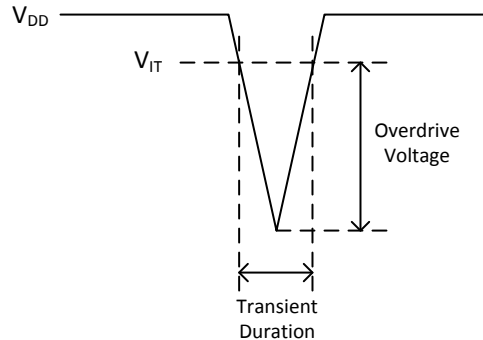


Figure 8. Threshold Overdrive Voltage

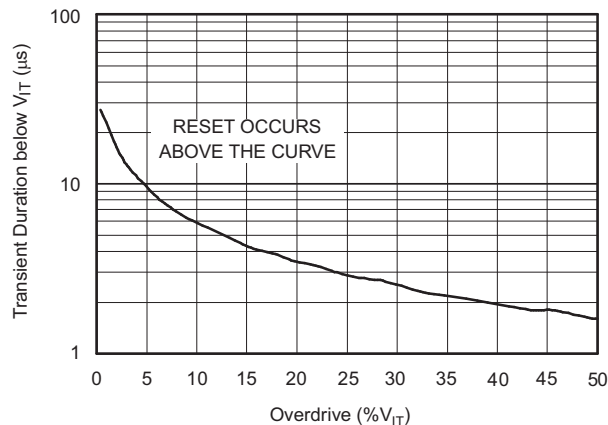


Figure 9. Maximum Transient Duration at Sense vs Sense Threshold Overdrive Voltage

8.3.2 SENSE Input

The SENSE input provides a terminal at which any system voltage can be monitored. If the voltage on this pin drops below V_{IT} , $\overline{\text{RESET}}$ is asserted low. The comparator has a built-in hysteresis to ensure smooth $\overline{\text{RESET}}$ assertions and deassertions. It is good analog design practice to put a 1-nF to 10-nF bypass capacitor on the SENSE input to reduce sensitivity to transients and layout parasitics.

Feature Description (continued)

The TPS3808G01-Q1 can be used to monitor any voltage rail down to 0.405 V using the circuit shown in Figure 10.

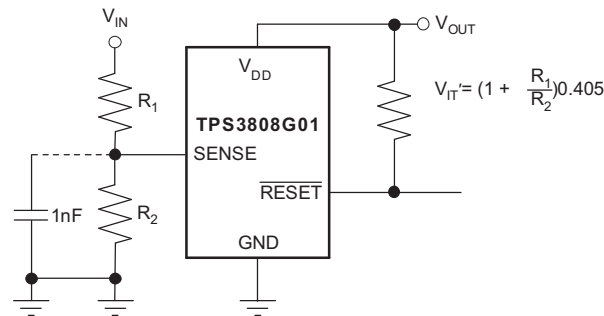


Figure 10. Using the TPS3808G01-Q1 to Monitor a User-Defined Threshold Voltage

8.3.3 Manual Reset (\overline{MR}) Input

The manual reset (\overline{MR}) input allows a processor or other logic circuits to initiate a reset. A logic low ($0.3 V_{DD}$) on \overline{MR} causes \overline{RESET} to assert low. After \overline{MR} returns to a logic high and SENSE is above its reset threshold, \overline{RESET} is deasserted high after the user-defined reset delay expires. \overline{MR} is internally tied to V_{DD} using a 90-k Ω resistor, so this pin can be left unconnected if \overline{MR} is not used.

See Figure 11 for how \overline{MR} can be used to monitor multiple system voltages. If the logic signal driving \overline{MR} does not go fully to V_{DD} , there will be some additional current draw into V_{DD} as a result of the internal pullup resistor on \overline{MR} . To minimize current draw, a logic-level FET can be used as shown in Figure 12.

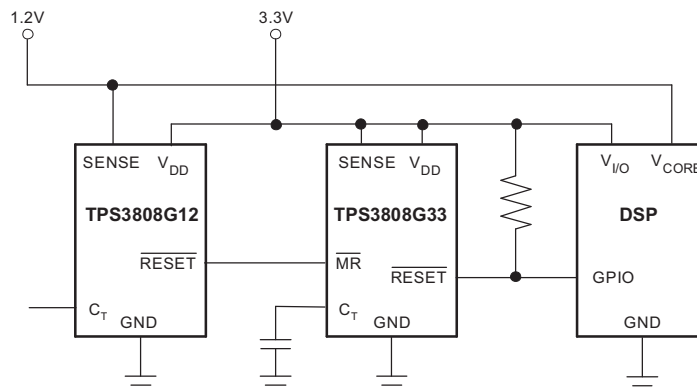


Figure 11. Using \overline{MR} to Monitor Multiple System Voltages

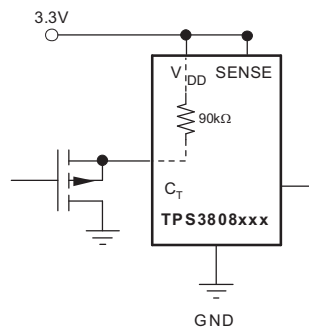


Figure 12. Using an External MOSFET to Minimize I_{DD} When \overline{MR} Signal Does Not Go to V_{DD}

Feature Description (continued)

8.3.4 Selecting the Reset Delay Time

The TPS3808Gxx-Q1 device has three options for setting the $\overline{\text{RESET}}$ delay time as shown in Figure 13. Figure 13 (a) shows the configuration for a fixed 300-ms typical delay time by tying C_T to V_{DD} ; a resistor from 40 k Ω to 200 k Ω must be used. Supply current is not affected by the choice of resistor. Figure 13 (b) shows a fixed 20-ms delay time by leaving the C_T pin open. Figure 13 (c) shows a ground referenced capacitor connected to C_T for a user-defined program time from 1.25 ms to 10 s.

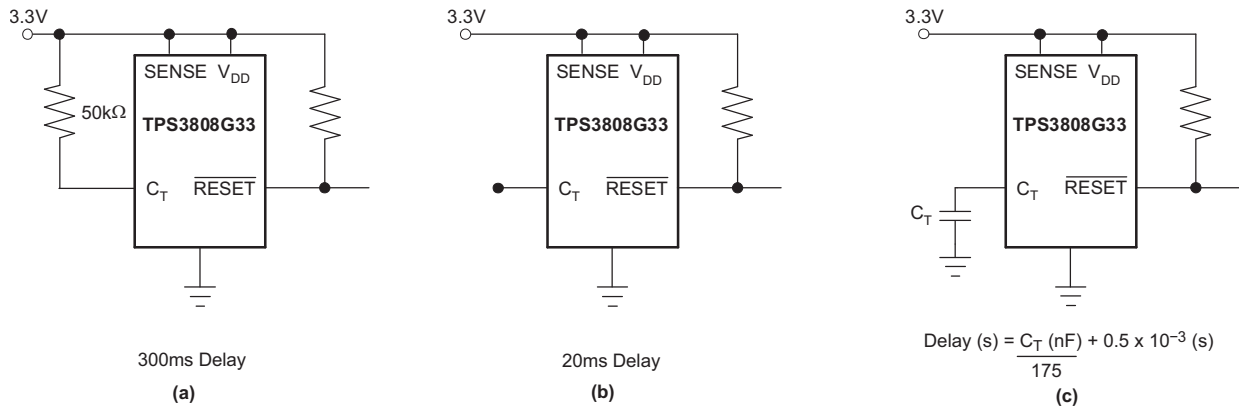


Figure 13. Configuration Used to Set the $\overline{\text{RESET}}$ Delay Time

The capacitor C_T should be ≥ 100 pF nominal value for the TPS3808Gxx-Q1 to recognize the capacitor is present. Use Equation 1 to calculate the capacitor value for a given delay time.

$$C_T \text{ (nF)} = \left[t_D \text{ (s)} - 0.5 \times 10^{-3} \text{ (s)} \right] \times 175 \quad (1)$$

The reset delay time is determined by the time it takes an on-chip precision 220-nA current source to charge the external capacitor to 1.23 V. When $\overline{\text{RESET}}$ asserts low, the capacitor is discharged. When the $\overline{\text{RESET}}$ conditions are cleared, the internal current source is enabled and begins to charge the external capacitor. When the voltage on this capacitor reaches 1.23 V, $\overline{\text{RESET}}$ deasserts. A low-leakage type capacitor such as a ceramic should be used and that stray capacitance around this pin may cause errors in the reset delay time.

8.4 Device Functional Modes

Whenever $\overline{\text{MR}}$ pin is set to a logic high and the SENSE input pin is higher than V_{IT} , the open-drain $\overline{\text{RESET}}$ signal is deasserted high. If $\overline{\text{MR}}$ pin is set to a logic low or the SENSE input pin falls lower than V_{IT} , then $\overline{\text{RESET}}$ is asserted low. Table 1 is a truth table that describes these operating modes.

Table 1. Truth Table

$\overline{\text{MR}}$	SENSE > V_{IT}	$\overline{\text{RESET}}$
L	0	L
L	1	L
H	0	L
H	1	H

9 Applications and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The TPS3808Gxx-Q1 microprocessor supervisory product family is designed to assert a $\overline{\text{RESET}}$ signal when either the SENSE pin voltage drops below V_{IT} or the manual reset ($\overline{\text{MR}}$) is driven low. The $\overline{\text{RESET}}$ output remains asserted for a user-adjustable time after both the manual reset ($\overline{\text{MR}}$) and SENSE voltages return above the respective thresholds. A broad range of voltage threshold and reset delay time adjustments are available, allowing these devices to be used in a variety of applications. Reset threshold voltages can be factory-set from 0.82 V to 3.3 V or from 4.4 V to 5 V, while the TPS3808G01-Q1 can be set to any voltage above 0.405 V using an external resistor divider. Two preset delay times are also user-selectable: connecting the C_T pin to V_{DD} results in a 300-ms reset delay, while leaving the C_T pin open yields a 20-ms reset delay. Additionally, connecting a capacitor between C_T and GND allows the designer to select any reset delay period from 1.25 ms to 10 s.

9.2 Typical Application

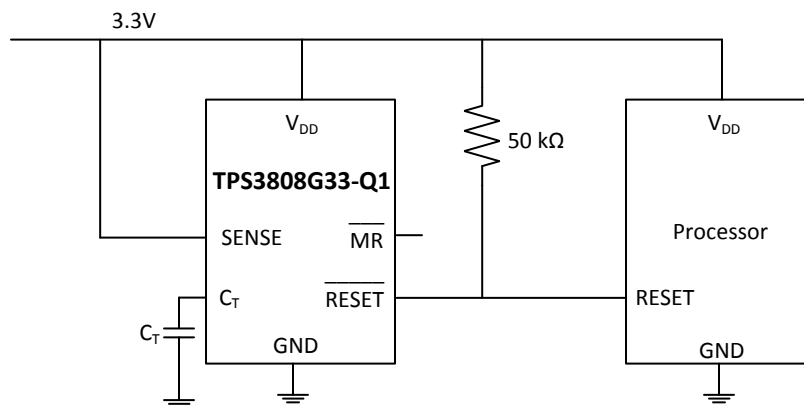


Figure 14. TPS3808G33-Q1 Typical Application

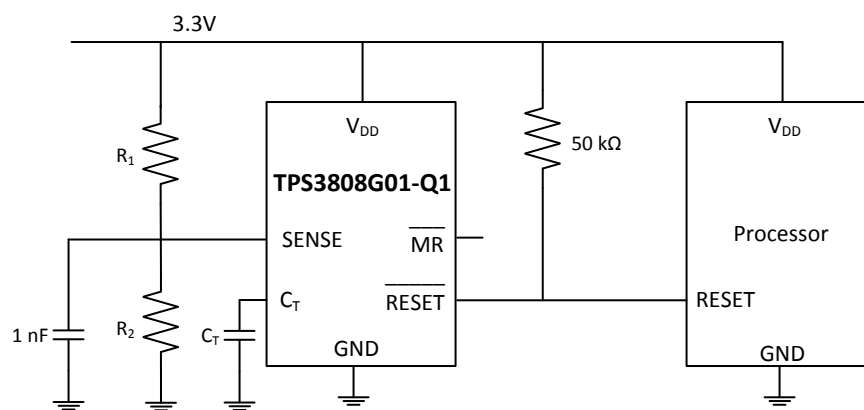


Figure 15. TPS3808G01-Q1 Typical Application

Typical Application (continued)

9.2.1 Design Requirements

The TPS3808Gxx-Q1 device must monitor a 3.3-V input voltage, and drive an active-low reset to the processor when the input voltage drops below the recommended operating voltage of the processor.

9.2.2 Detailed Design Procedure

To monitor the 3.3-V input voltage, TPS3808G33-Q1 is used and the 3.3-V supply is connected directly to the SENSE pin. The open-drain RESET output is connected to V_{DD} through a 50-kΩ resistor. To select the output delay on the RESET pin, connect the C_T pin to V_{DD}, left floating, or connect through a capacitor to GND. For more details on selecting this delay, see [Selecting the Reset Delay Time](#).

When using TPS3808G01-Q1, select R1 and R2 resistor values to select the threshold voltage based on the following equation: $V_{IT} = (1 + R1 / R2) \times 0.405$.

9.2.3 Application Curves

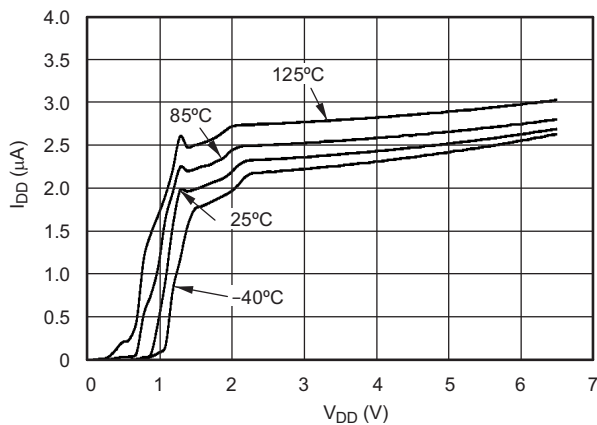


Figure 16. Supply Current vs Supply Voltage

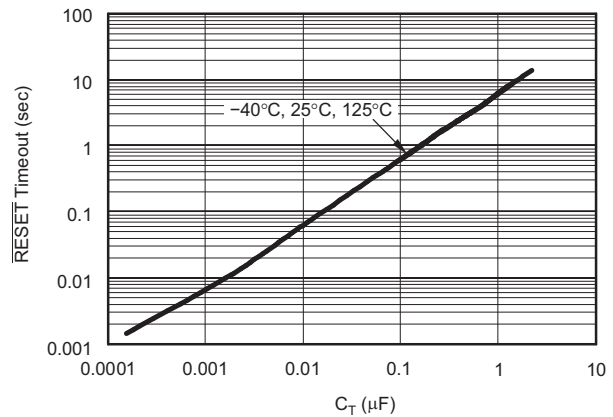


Figure 17. RESET Time-out Period vs C_T

10 Power Supply Recommendations

The TPS3808Gxx-Q1 devices are designed to operate from an input supply from 1.8 V to 6.5 V. TI recommends placing a 0.1- μ F capacitor near the V_{DD} pin.

11 Layout

11.1 Layout Guidelines

TI recommends placing the 0.1- μ F decoupling capacitor close to the V_{DD} pin. The V_{DD} trace should be able to carry 6 μ A without a significant drop in voltage.

11.2 Layout Example

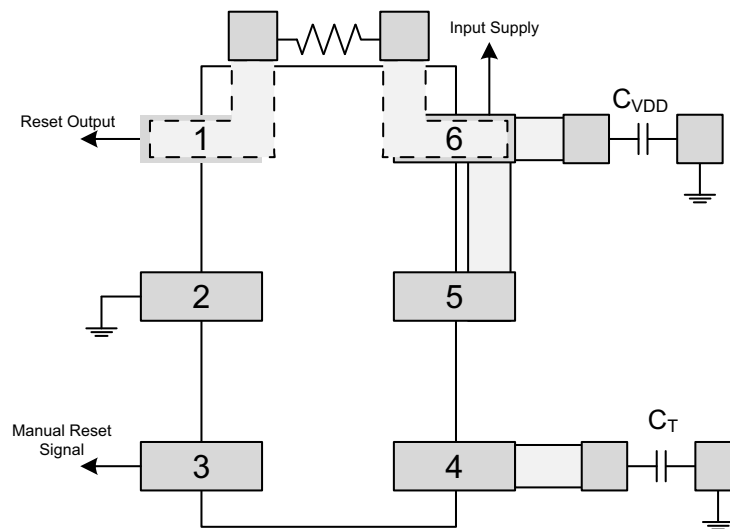


Figure 18. Recommended Layout

12 Device and Documentation Support

12.1 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 2. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
TPS3808G01-Q1	Click here	Click here	Click here	Click here	Click here
TPS3808G12-Q1	Click here	Click here	Click here	Click here	Click here
TPS3808G125-Q1	Click here	Click here	Click here	Click here	Click here
TPS3808G15-Q1	Click here	Click here	Click here	Click here	Click here
TPS3808G18-Q1	Click here	Click here	Click here	Click here	Click here
TPS3808G30-Q1	Click here	Click here	Click here	Click here	Click here
TPS3808G33-Q1	Click here	Click here	Click here	Click here	Click here
TPS3808G50-Q1	Click here	Click here	Click here	Click here	Click here

12.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

TI E2E™ Online Community *TI's Engineer-to-Engineer (E2E) Community*. Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.4 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

12.5 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS3808G01QDBVRQ1	ACTIVE	SOT-23	DBV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	BAZ	Samples
TPS3808G01QDRVRQ1	ACTIVE	WSON	DRV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PSJQ	Samples
TPS3808G125QDBVRQ1	ACTIVE	SOT-23	DBV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	QWZ	Samples
TPS3808G12QDBVRQ1	ACTIVE	SOT-23	DBV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	CEM	Samples
TPS3808G15QDBVRQ1	ACTIVE	SOT-23	DBV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	OFV	Samples
TPS3808G18QDBVRQ1	ACTIVE	SOT-23	DBV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	OBZ	Samples
TPS3808G30QDBVRQ1	ACTIVE	SOT-23	DBV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	AVP	Samples
TPS3808G33QDBVRQ1	ACTIVE	SOT-23	DBV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	AVQ	Samples
TPS3808G50QDBVRQ1	ACTIVE	SOT-23	DBV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	CEL	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer:The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF TPS3808-Q1 :

- Catalog: [TPS3808](#)
- Enhanced Product: [TPS3808-EP](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Enhanced Product - Supports Defense, Aerospace and Medical Applications

TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS3808G01QDBVRQ1	SOT-23	DBV	6	3000	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS3808G01QDRVRQ1	WSON	DRV	6	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
TPS3808G125QDBVRQ1	SOT-23	DBV	6	3000	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS3808G12QDBVRQ1	SOT-23	DBV	6	3000	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS3808G15QDBVRQ1	SOT-23	DBV	6	3000	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS3808G18QDBVRQ1	SOT-23	DBV	6	3000	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS3808G30QDBVRQ1	SOT-23	DBV	6	3000	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS3808G33QDBVRQ1	SOT-23	DBV	6	3000	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS3808G50QDBVRQ1	SOT-23	DBV	6	3000	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS

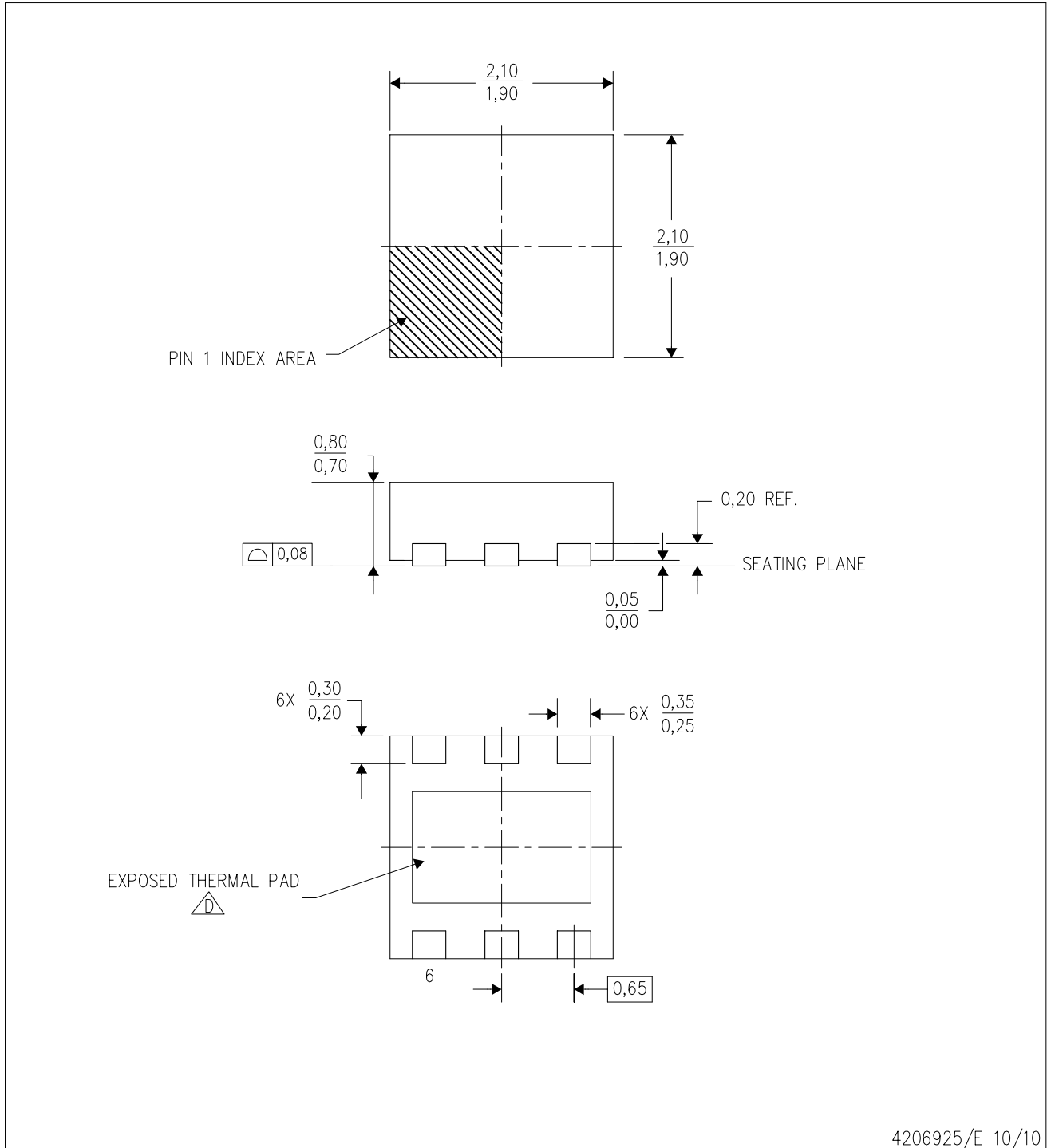

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS3808G01QDBVRQ1	SOT-23	DBV	6	3000	203.0	203.0	35.0
TPS3808G01QDRVRQ1	WSON	DRV	6	3000	210.0	185.0	35.0
TPS3808G125QDBVRQ1	SOT-23	DBV	6	3000	203.0	203.0	35.0
TPS3808G12QDBVRQ1	SOT-23	DBV	6	3000	203.0	203.0	35.0
TPS3808G15QDBVRQ1	SOT-23	DBV	6	3000	203.0	203.0	35.0
TPS3808G18QDBVRQ1	SOT-23	DBV	6	3000	203.0	203.0	35.0
TPS3808G30QDBVRQ1	SOT-23	DBV	6	3000	203.0	203.0	35.0
TPS3808G33QDBVRQ1	SOT-23	DBV	6	3000	203.0	203.0	35.0
TPS3808G50QDBVRQ1	SOT-23	DBV	6	3000	203.0	203.0	35.0

MECHANICAL DATA

DRV (S-PWSON-N6)

PLASTIC SMALL OUTLINE NO-LEAD



4206925/E 10/10

- NOTES:
- All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - This drawing is subject to change without notice.
 - Small Outline No-Lead (SON) package configuration.
- D** The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.

THERMAL PAD MECHANICAL DATA

DRV (S-PWSON-N6)

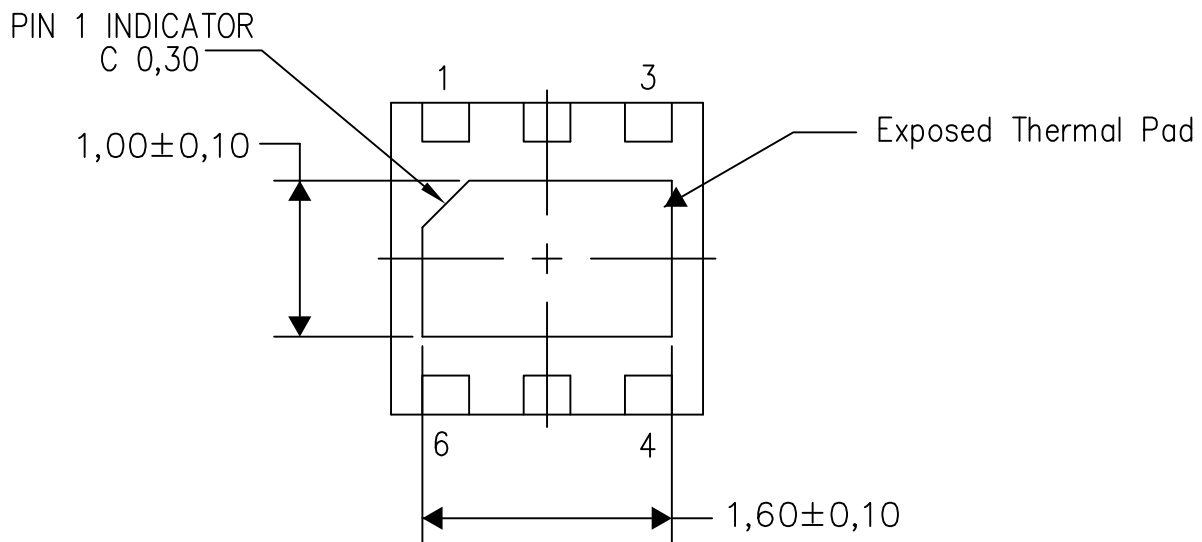
PLASTIC SMALL OUTLINE NO-LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Bottom View

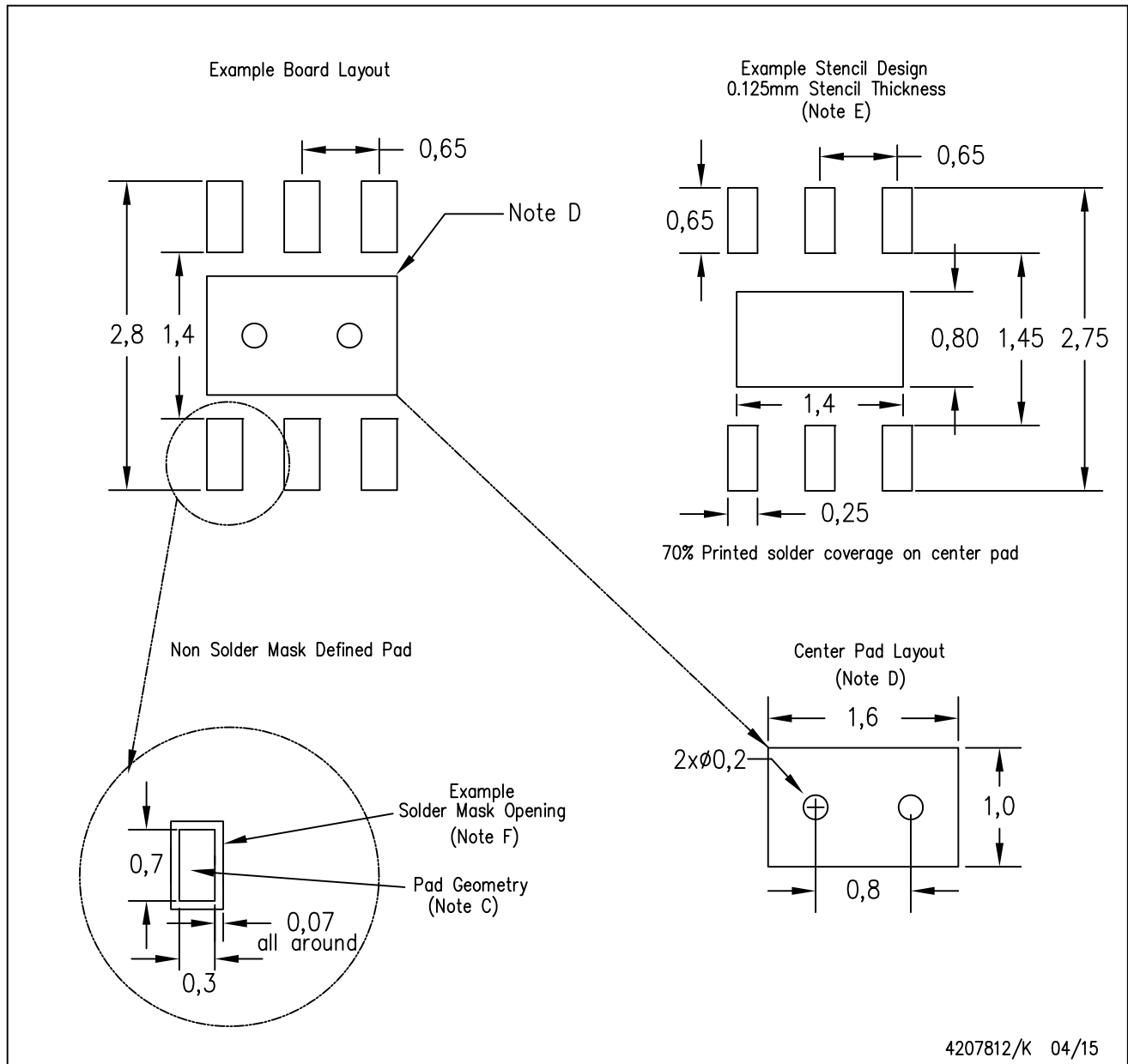
Exposed Thermal Pad Dimensions

4206926/Q 04/15

NOTE: All linear dimensions are in millimeters

DRV (S-PWSON-N6)

PLASTIC SMALL OUTLINE NO-LEAD

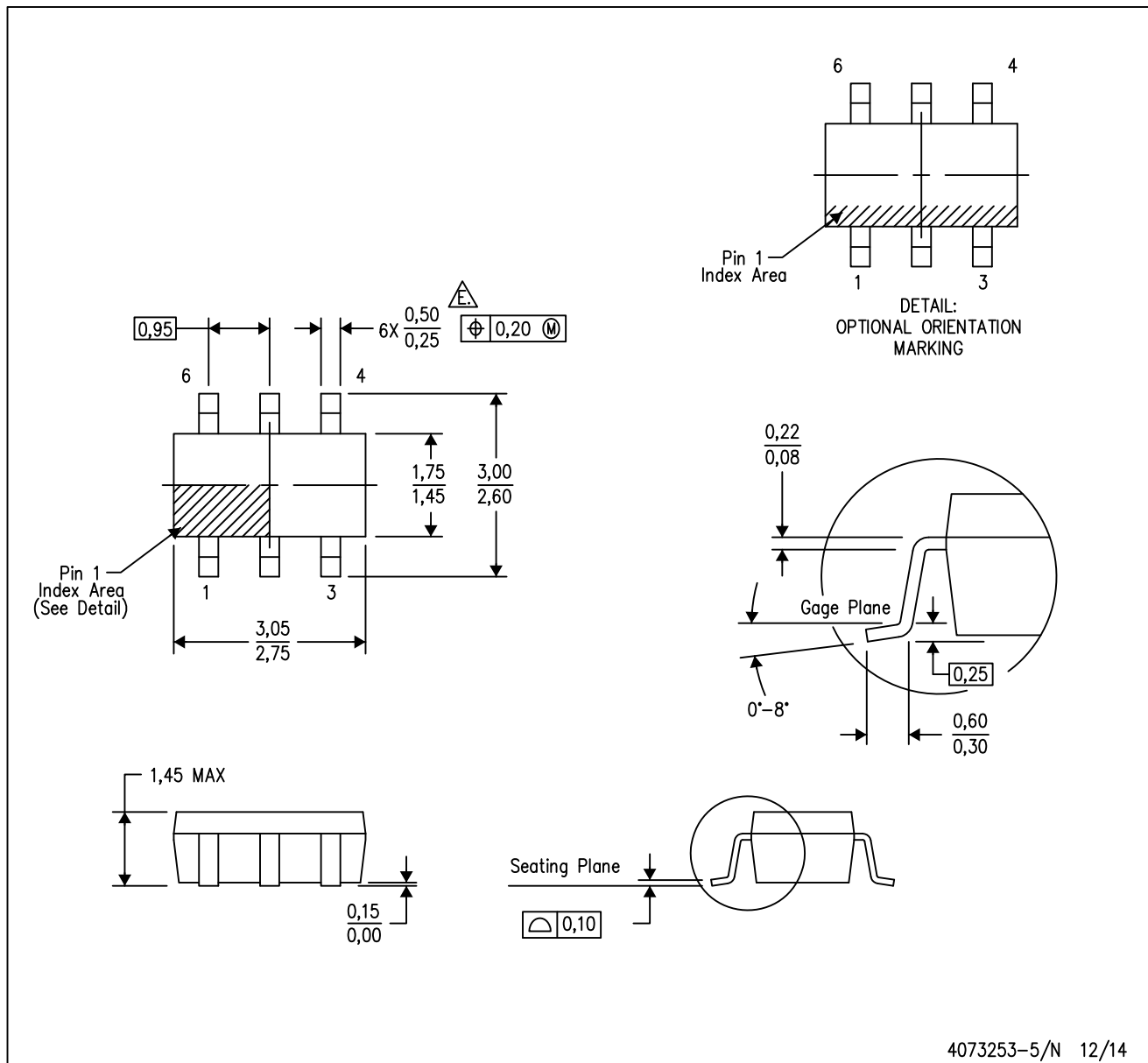



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate designs.
 - D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <<http://www.ti.com>>.
 - E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
 - F. Customers should contact their board fabrication site for solder mask tolerances.

MECHANICAL DATA

DBV (R-PDSO-G6)

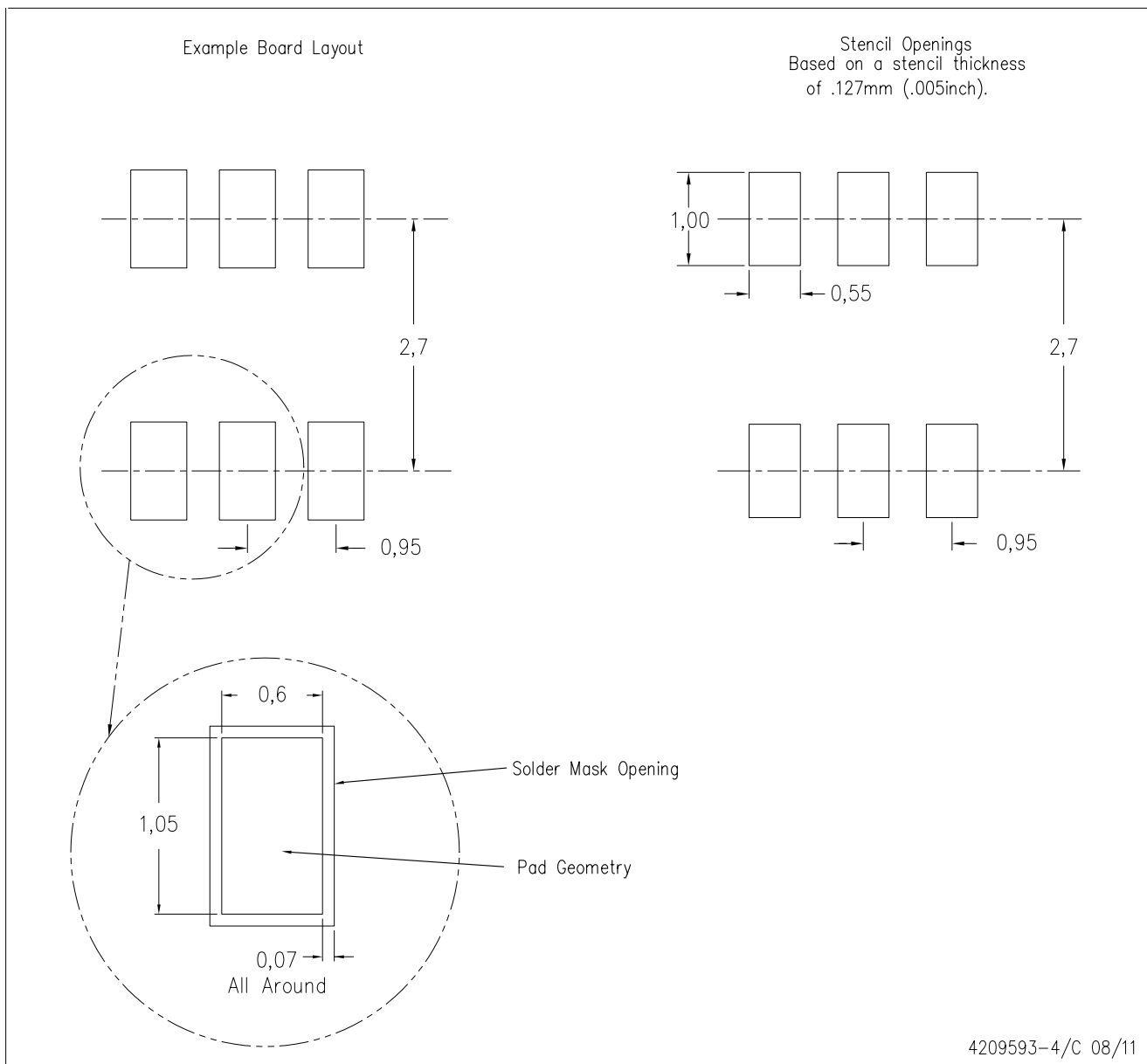
PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
 - D. Leads 1,2,3 may be wider than leads 4,5,6 for package orientation.
-  Falls within JEDEC MO-178 Variation AB, except minimum lead width.

DBV (R-PDSO-G6)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
 - D. Publication IPC-7351 is recommended for alternate designs.
 - E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.

IMPORTANT NOTICE

Texas Instruments Incorporated (TI) reserves the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete.

TI's published terms of sale for semiconductor products (<http://www.ti.com/sc/docs/stdterms.htm>) apply to the sale of packaged integrated circuit products that TI has qualified and released to market. Additional terms may apply to the use or sale of other types of TI products and services.

Reproduction of significant portions of TI information in TI data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such reproduced documentation. Information of third parties may be subject to additional restrictions. Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyers and others who are developing systems that incorporate TI products (collectively, "Designers") understand and agree that Designers remain responsible for using their independent analysis, evaluation and judgment in designing their applications and that Designers have full and exclusive responsibility to assure the safety of Designers' applications and compliance of their applications (and of all TI products used in or for Designers' applications) with all applicable regulations, laws and other applicable requirements. Designer represents that, with respect to their applications, Designer has all the necessary expertise to create and implement safeguards that (1) anticipate dangerous consequences of failures, (2) monitor failures and their consequences, and (3) lessen the likelihood of failures that might cause harm and take appropriate actions. Designer agrees that prior to using or distributing any applications that include TI products, Designer will thoroughly test such applications and the functionality of such TI products as used in such applications.

TI's provision of technical, application or other design advice, quality characterization, reliability data or other services or information, including, but not limited to, reference designs and materials relating to evaluation modules, (collectively, "TI Resources") are intended to assist designers who are developing applications that incorporate TI products; by downloading, accessing or using TI Resources in any way, Designer (individually or, if Designer is acting on behalf of a company, Designer's company) agrees to use any particular TI Resource solely for this purpose and subject to the terms of this Notice.

TI's provision of TI Resources does not expand or otherwise alter TI's applicable published warranties or warranty disclaimers for TI products, and no additional obligations or liabilities arise from TI providing such TI Resources. TI reserves the right to make corrections, enhancements, improvements and other changes to its TI Resources. TI has not conducted any testing other than that specifically described in the published documentation for a particular TI Resource.

Designer is authorized to use, copy and modify any individual TI Resource only in connection with the development of applications that include the TI product(s) identified in such TI Resource. NO OTHER LICENSE, EXPRESS OR IMPLIED, BY ESTOPPEL OR OTHERWISE TO ANY OTHER TI INTELLECTUAL PROPERTY RIGHT, AND NO LICENSE TO ANY TECHNOLOGY OR INTELLECTUAL PROPERTY RIGHT OF TI OR ANY THIRD PARTY IS GRANTED HEREIN, including but not limited to any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information regarding or referencing third-party products or services does not constitute a license to use such products or services, or a warranty or endorsement thereof. Use of TI Resources may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

TI RESOURCES ARE PROVIDED "AS IS" AND WITH ALL FAULTS. TI DISCLAIMS ALL OTHER WARRANTIES OR REPRESENTATIONS, EXPRESS OR IMPLIED, REGARDING RESOURCES OR USE THEREOF, INCLUDING BUT NOT LIMITED TO ACCURACY OR COMPLETENESS, TITLE, ANY EPIDEMIC FAILURE WARRANTY AND ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, AND NON-INFRINGEMENT OF ANY THIRD PARTY INTELLECTUAL PROPERTY RIGHTS. TI SHALL NOT BE LIABLE FOR AND SHALL NOT DEFEND OR INDEMNIFY DESIGNER AGAINST ANY CLAIM, INCLUDING BUT NOT LIMITED TO ANY INFRINGEMENT CLAIM THAT RELATES TO OR IS BASED ON ANY COMBINATION OF PRODUCTS EVEN IF DESCRIBED IN TI RESOURCES OR OTHERWISE. IN NO EVENT SHALL TI BE LIABLE FOR ANY ACTUAL, DIRECT, SPECIAL, COLLATERAL, INDIRECT, PUNITIVE, INCIDENTAL, CONSEQUENTIAL OR EXEMPLARY DAMAGES IN CONNECTION WITH OR ARISING OUT OF TI RESOURCES OR USE THEREOF, AND REGARDLESS OF WHETHER TI HAS BEEN ADVISED OF THE POSSIBILITY OF SUCH DAMAGES.

Unless TI has explicitly designated an individual product as meeting the requirements of a particular industry standard (e.g., ISO/TS 16949 and ISO 26262), TI is not responsible for any failure to meet such industry standard requirements.

Where TI specifically promotes products as facilitating functional safety or as compliant with industry functional safety standards, such products are intended to help enable customers to design and create their own applications that meet applicable functional safety standards and requirements. Using products in an application does not by itself establish any safety features in the application. Designers must ensure compliance with safety-related requirements and standards applicable to their applications. Designer may not use any TI products in life-critical medical equipment unless authorized officers of the parties have executed a special contract specifically governing such use. Life-critical medical equipment is medical equipment where failure of such equipment would cause serious bodily injury or death (e.g., life support, pacemakers, defibrillators, heart pumps, neurostimulators, and implantables). Such equipment includes, without limitation, all medical devices identified by the U.S. Food and Drug Administration as Class III devices and equivalent classifications outside the U.S.

TI may expressly designate certain products as completing a particular qualification (e.g., Q100, Military Grade, or Enhanced Product). Designers agree that it has the necessary expertise to select the product with the appropriate qualification designation for their applications and that proper product selection is at Designers' own risk. Designers are solely responsible for compliance with all legal and regulatory requirements in connection with such selection.

Designer will fully indemnify TI and its representatives against any damages, costs, losses, and/or liabilities arising out of Designer's non-compliance with the terms and provisions of this Notice.