适合便携式设备的双通道、200mA、低 I_Q 、低压降稳压器

特性

- 超低的压降:
  - **150mV**（在 I_{OUT} =200mA 和 V_{OUT} = 2.8V 时）
  - **75mV**（在 I_{OUT} =100mA 和 V_{OUT} = 2.8V时）
  - **40mV**（在 I_{OUT} =50mA 和 V_{OUT} = 2.8V时）
- 在整个温度范围内可提供 **2%** 的准确度
- 低I_Q：每个稳压器为 **35µA**
- 可提供多种固定输出电压组合：**1.2V**至**4.8V**
- 高**PSRR**：**70dB**（在 **1kHz** 频率下）
- 可在采用 **0.1µF** 的有效电容时保持稳定(1)
- 过流和热保护
- 用于每个输出的专用 V_{REF} 最大限度地降低了串扰
- 采用**1.5mm x 1.5mm SON-6** 封装

(1) 请参见 应用信息部分中的 输入和输出电容器要求

应用

- 无线头戴式耳机、智能手机、**PDA**
- **MP3** 播放器及其他手持式产品

说明

TLV710 和 TLV711 系列双通道、低压降 (LDO) 线性稳压器是具有卓越的线路输入电压及负载瞬态响应性能的低静态电流器件。 这些 LDO 专门针对功耗敏感型应用而设计。 这些器件在整个温度范围内提供了2% 的典型准确度。

TLV711系列提供了一种有源下拉电路，以对输出进行快速放电。

此外，TLV711-D 器件系列还在 EN 引脚上布设了下拉电阻器。 这种设计有助于在信号驱动 EN 引脚处于一种微弱、不确定状态（例如：在启动期间有可能为三态的处理器 GPIO）时停用器件。 该下拉电阻器可将至 EN 引脚的电压拉低至 0V，从而停用器件。

TLV710 和 TLV711系列采用 1.5mm x 1.5mm SON-6 封装，而且非常适合于手持式应用。

TLV710
TLV711
1.5mm x 1.5mm SON-6
(TOP VIEW)

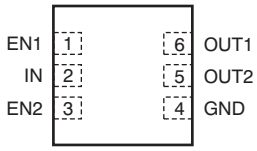
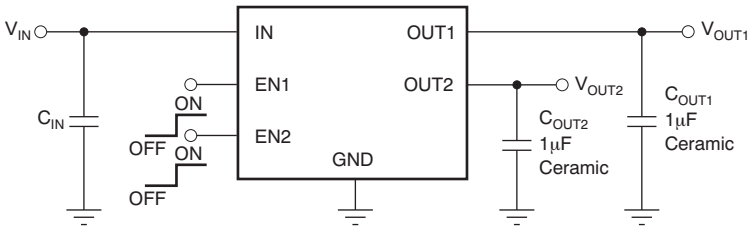


图 **1.** 典型应用电路



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This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ORDERING INFORMATION(1)

PRODUCT	V_{OUT}(2)
TLV710**xxyy**qwwwz TLV711**xxyy**qwwwz	**XX** is nominal output voltage of channel 1 (for example 18 = 1.8V). **YY** is nominal output voltage of channel 2 (for example 28 = 2.8V). **Q** is optional. Use "U" for devices with EN pin pull-up resistor, and "D" for devices with EN pin pull-down resistor. **WWW** is package designator. **Z** is package quantity. Use "R" for reel (3000 pieces), and "T" for tape (250 pieces).

(1) For the most current package and ordering information see the Package Option Addendum at the end of this document, or visit the device product folder on www.ti.com.
(2) Output voltages from 1.2V to 4.8V in 50mV increments are available through the use of innovative factory OTP programming; minimum order quantities may apply. Contact factory for details and availability.

ABSOLUTE MAXIMUM RATINGS(1)

At T_J = –40°C to +125°C (unless otherwise noted).

		VALUE		UNIT
		MIN	MAX	
Voltage(2)	IN	–0.3	+6.0	V
	EN	–0.3	V_{IN} + 0.3	V
	OUT	–0.3	+6.0	V
Current	OUT	Internally limited		A
Output short-circuit duration		Indefinite		s
Temperature	Operating junction, T_J	–55	+150	°C
	Storage, T_{stg}	–55	+150	°C
Electrostatic Discharge Rating	Human body model (HBM) QSS 009-105 (JESD22-A114A)		2	kV
	Charged device model (CDM) QSS 009-147 (JESD22-C101B.01)		500	V

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated is not implied. Exposure to absolute-maximum-rated conditions for extended periods my affect device reliability.
(2) All voltages with respect to ground.

THERMAL INFORMATION(1)

THERMAL METRIC(2)		TLV710, TLV711 DSE 6 PINS	UNITS
ψ_{JT}	Junction-to-top characterization parameter	6	°C/W

(1) See the *Power Dissipation* section for more details.
(2) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

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ELECTRICAL CHARACTERISTICS

At T_J = +25°C, V_{IN} = $V_{OUT(TYP)}$ + 0.5V or 2.0V (whichever is greater), I_{OUT} = 10mA, V_{EN1} = V_{EN2} = 0.9V, and C_{OUT1} = C_{OUT2} = 1µF, unless otherwise noted.

PARAMETER		TEST CONDITIONS		TLV710, TLV711			UNIT
				MIN	TYP	MAX	
V_{IN}	Input voltage range			2.0		5.5	V
V_O	Output voltage range			1.2		4.8	V
V_{OUT}	DC output accuracy	–40°C ≤ T_J ≤ +125°C		–2		+2	%
$\Delta V_O/\Delta V_{IN}$	Line regulation	$V_{OUT(NOM)}$ + 0.5V ≤ V_{IN} ≤ 5.5V			1	5	mV
$\Delta V_O/\Delta I_{OUT}$	Load regulation	0mA ≤ I_{OUT} ≤ 200mA			5	15	mV
V_{DO}	Dropout voltage	V_{IN} = 0.98V × $V_{OUT(NOM)}$, I_{OUT} = 200mA, 2V ≤ V_{OUT} < 2.4V			200	285	mV
		V_{IN} = 0.98V × $V_{OUT(NOM)}$, I_{OUT} = 200mA, 2.4V ≤ V_{OUT} < 2.8V			175	250	mV
		V_{IN} = 0.98V × $V_{OUT(NOM)}$, I_{OUT} = 200mA, 2.8V ≤ V_{OUT} < 3.3V			150	215	mV
		V_{IN} = 0.98V × $V_{OUT(NOM)}$, I_{OUT} = 200mA, 3.3V ≤ V_{OUT} ≤ 4.8V			140	200	mV
I_{CL}	Output current limit	V_{OUT} = 0.9V × $V_{OUT(NOM)}$		220	350	550	mA
I_Q	Quiescent current	V_{EN1} = high, V_{EN2} = low, I_{OUT1} = 0mA			35		µA
		V_{EN1} = low, V_{EN2} = high, I_{OUT2} = 0mA			35		µA
		V_{EN1} = high, V_{EN2} = high, I_{OUT} = 0mA			70	110	µA
I_{GND}	Ground pin current	I_{OUT1} = I_{OUT2} = 200mA			360		µA
$I_{SHUTDOWN}$	Shutdown current	$V_{EN1,2}$ ≤ 0.4V, 2.0V ≤ V_{IN} ≤ 4.5V			2.5	4	µA
PSRR	Power-supply rejection ratio	V_{OUT} = 1.8V	f = 10Hz		80		dB
			f = 100Hz		75		dB
			f = 1kHz		70		dB
			f = 10kHz		70		dB
			f = 100kHz		50		dB
V_N	Output noise voltage	BW = 100Hz to 100kHz, V_{OUT} = 1.8V			48		μV_{RMS}
t_{STR}	Startup time(1)	C_{OUT} = 1.0µF, I_{OUT} = 200mA			100		µs
V_{HI}	Enable high (enabled)			0.9		V_{IN}	V
V_{LO}	Enable low (shutdown)			0		0.4	V
I_{EN}	Enable pin current, enabled	TLV710, TLV711			0.04		µA
		TLV710-D, TLV711-D			6		µA
UVLO	Undervoltage lockout	V_{IN} rising			1.9		V
T_J	Operating junction temperature			–40		+125	°C
T_{SD}	Thermal shutdown temperature	Shutdown, temperature increasing			+165		°C
		Reset, temperature decreasing			+145		°C

(1) Startup time = time from EN assertion to 0.98 x $V_{OUT(NOM)}$.

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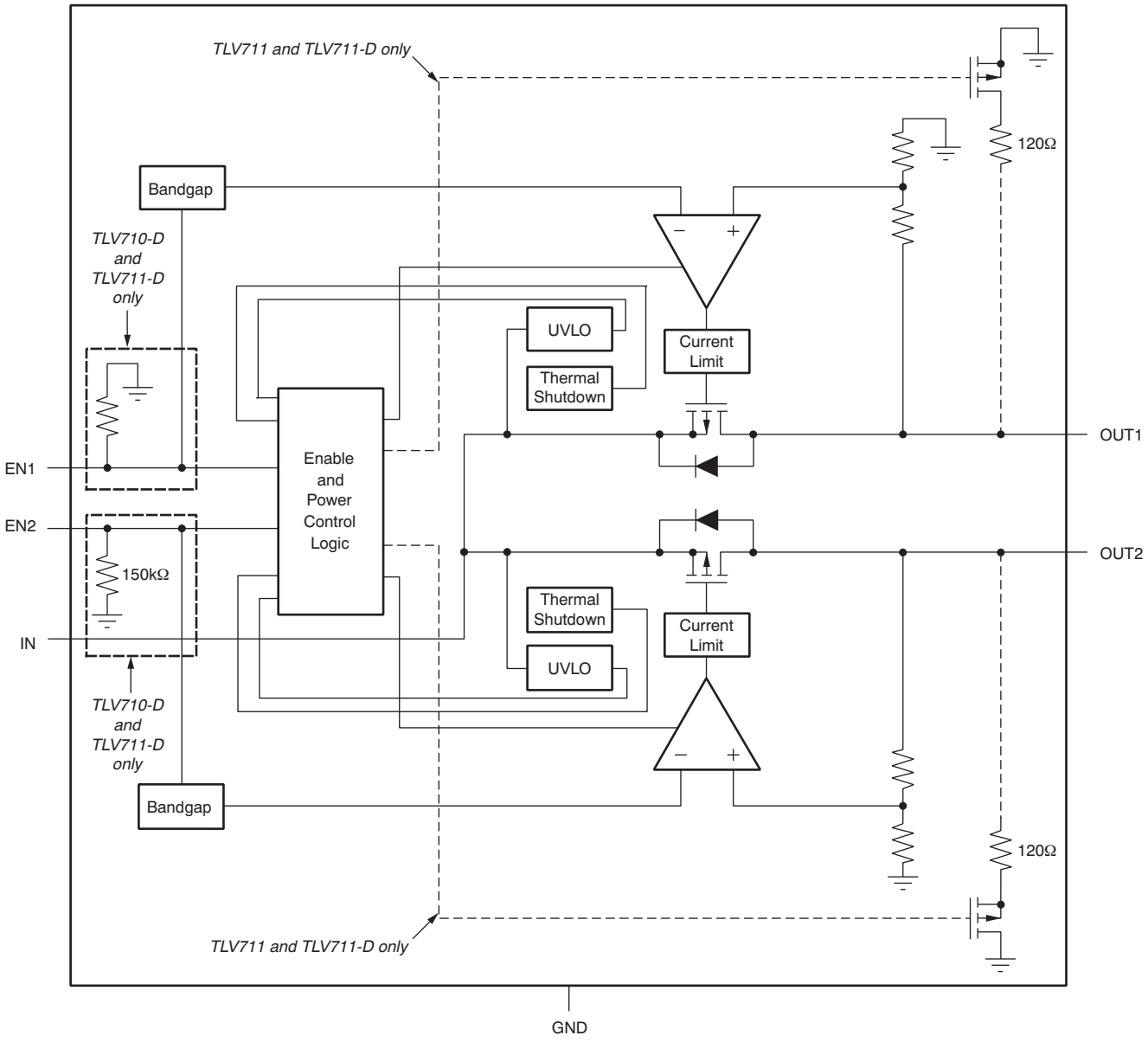
FUNCTIONAL BLOCK DIAGRAM



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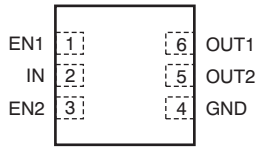
PIN CONFIGURATION

DSE PACKAGE
1.5mm x 1.5mm SON-6
(TOP VIEW)



PIN DESCRIPTIONS

NAME	PIN NO.	DESCRIPTION
EN1	1	Enable pin for regulator 1. Driving EN1 over 0.9V turns on regulator 1. Driving EN below 0.4V puts regulator 1 into shutdown mode.
IN	2	Input pin. A small capacitor is needed from this pin to ground to assure stability. See *Input and Output Capacitor Requirements* in the *Application Information* section for more details.
EN2	3	Enable pin for regulator 2. Driving EN2 over 0.9V turns on regulator 2. Driving EN2 below 0.4V puts regulator2 into shutdown mode.
GND	4	Ground pin.
OUT2	5	Regulated output voltage pin. A small 1μF ceramic capacitor is needed from this pin to ground to assure stability. See *Input and Output Capacitor Requirements* in the *Application Information* section for more details.
OUT1	6	Regulated output voltage pin. A small 1μF ceramic capacitor is needed from this pin to ground to assure stability. See *Input and Output Capacitor Requirements* in the *Application Information* section for more details.

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TYPICAL CHARACTERISTICS

Over operating temperature range of T_J = –40°C to +125°C, $V_{EN1} = V_{EN2} = V_{IN}$, C_{IN} = 1µF, C_{OUT1} = 1µF, and C_{OUT2} = 1µF, unless otherwise noted. Typical values are at T_J = +25°C.

LINE REGULATION: V_{OUT1} (TLV7101828)

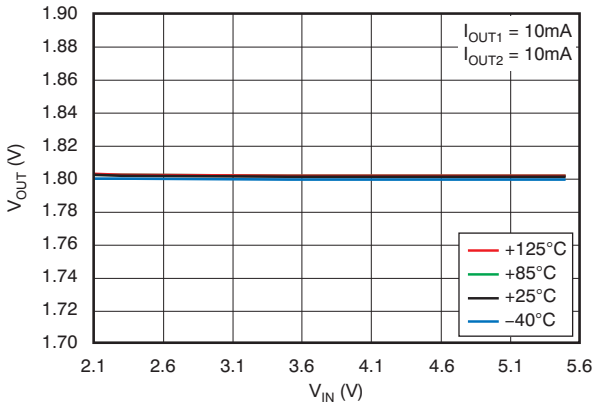

Figure 2.

LINE REGULATION: V_{OUT2} (TLV7101828)

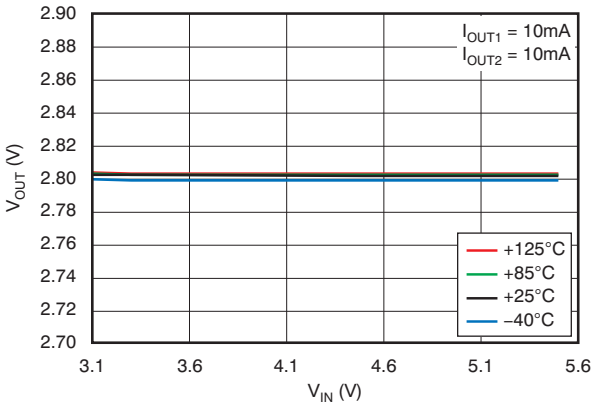

Figure 3.

LINE REGULATION: V_{OUT1} (TLV7101828)

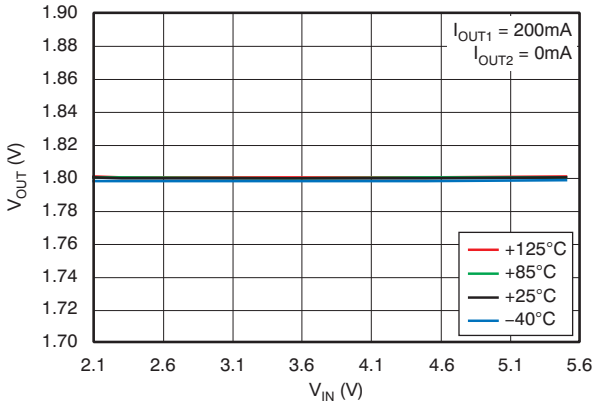

Figure 4.

LINE REGULATION: V_{OUT2} (TLV7101828)

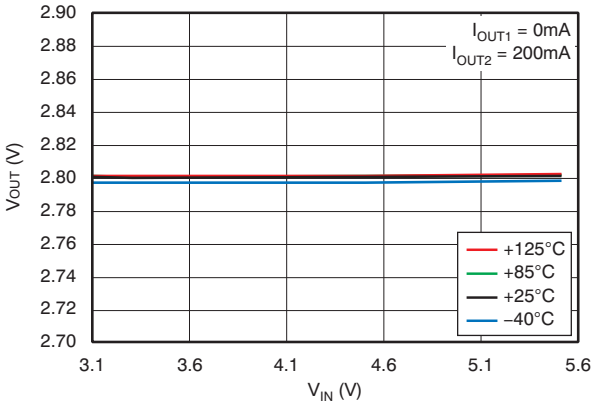

Figure 5.

LINE REGULATION: V_{OUT1} (TLV7103333)

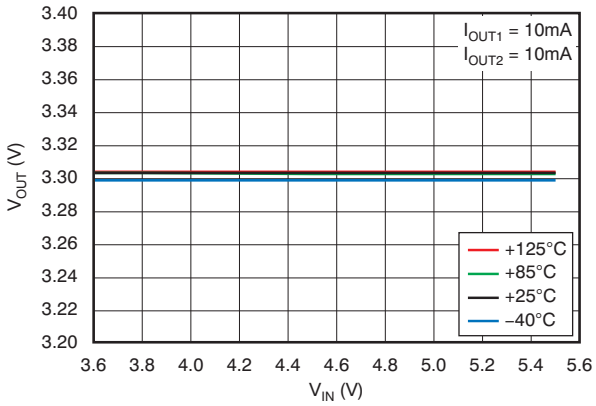

Figure 6.

LINE REGULATION: V_{OUT2} (TLV7103333)

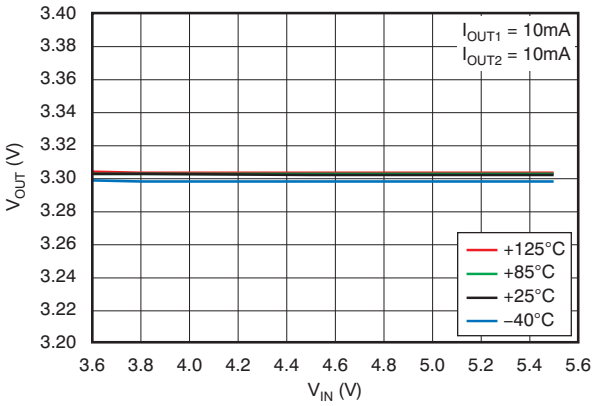

Figure 7.

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TYPICAL CHARACTERISTICS (continued)

Over operating temperature range of T_J = –40°C to +125°C, $V_{EN1} = V_{EN2} = V_{IN}$, C_{IN} = 1µF, C_{OUT1} = 1µF, and C_{OUT2} = 1µF, unless otherwise noted. Typical values are at T_J = +25°C.

LINE REGULATION: V_{OUT1} (TLV7103333)

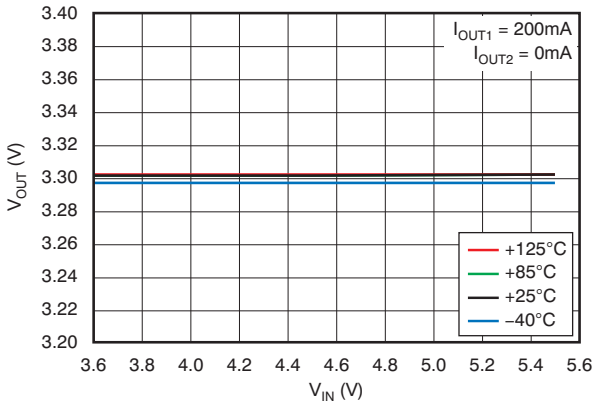

Figure 8.

LINE REGULATION: V_{OUT2} (TLV7103333)

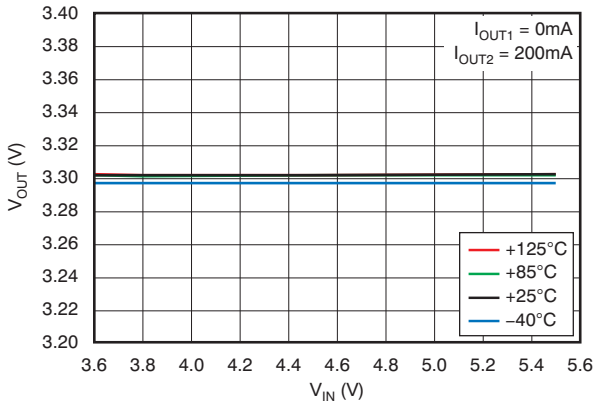

Figure 9.

LINE REGULATION: V_{OUT1} (TLV7111525)

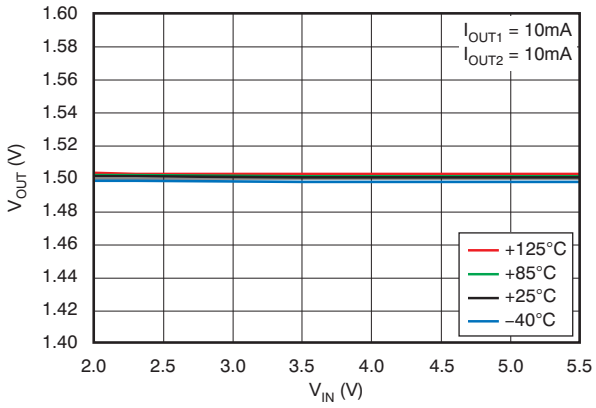

Figure 10.

LINE REGULATION: V_{OUT2} (TLV7111525)

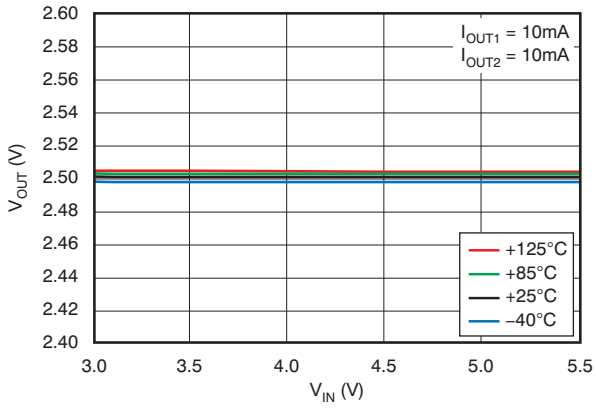

Figure 11.

LINE REGULATION: V_{OUT1} (TLV7111525)

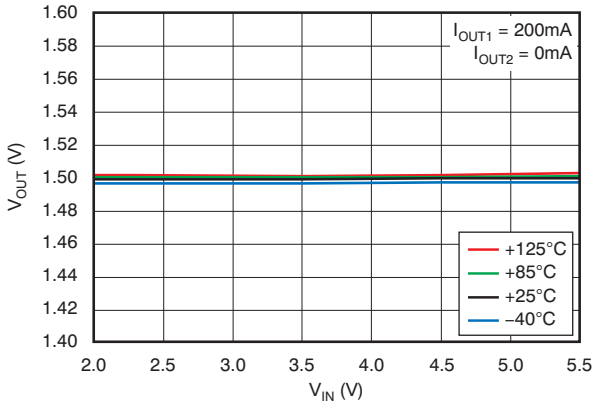

Figure 12.

LINE REGULATION: V_{OUT2} (TLV7111525)

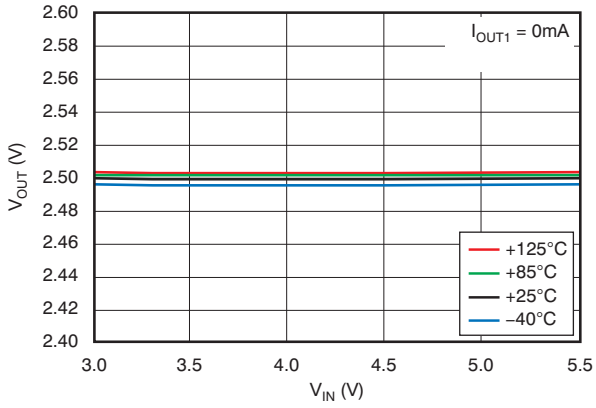

Figure 13.

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TYPICAL CHARACTERISTICS (continued)

Over operating temperature range of T_J = –40°C to +125°C, $V_{EN1} = V_{EN2} = V_{IN}$, C_{IN} = 1µF, C_{OUT1} = 1µF, and C_{OUT2} = 1µF, unless otherwise noted. Typical values are at T_J = +25°C.

LOAD REGULATION: V_{OUT1} (TLV7101828)

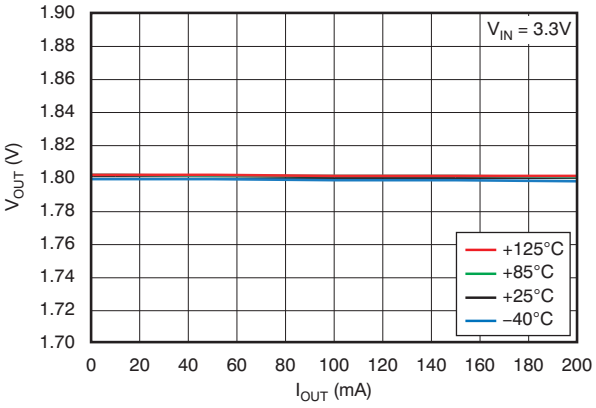

Figure 14.

LOAD REGULATION: V_{OUT2} (TLV7101828)

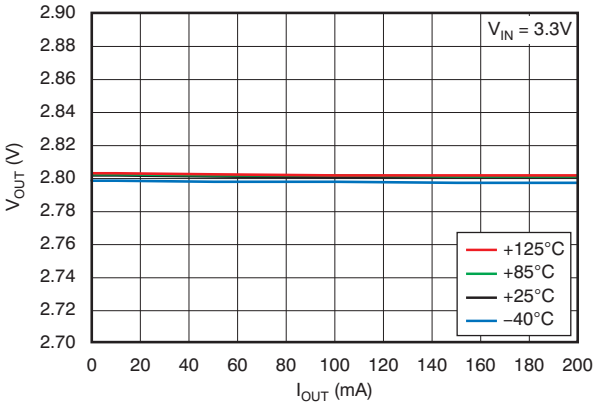

Figure 15.

LOAD REGULATION: V_{OUT1} (TLV7103333)

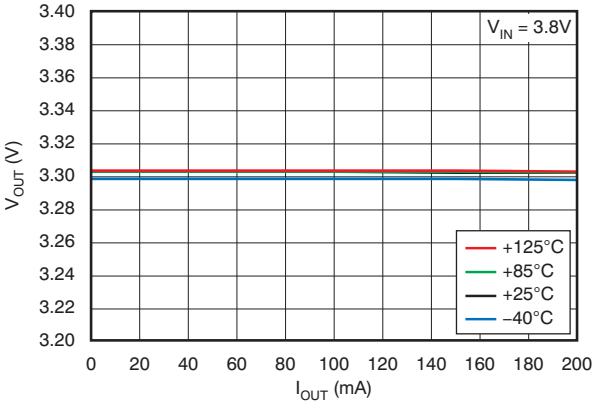

Figure 16.

LOAD REGULATION: V_{OUT2} (TLV7103333)

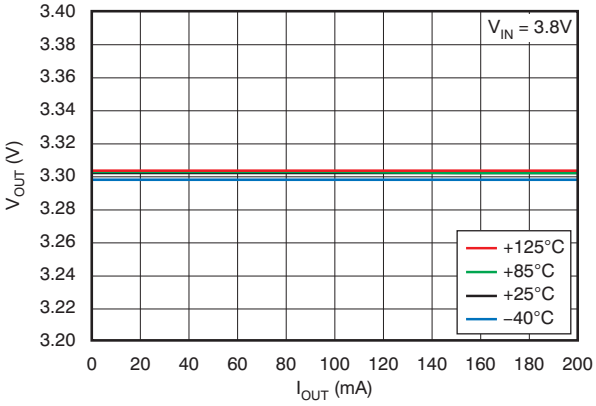

Figure 17.

LOAD REGULATION: V_{OUT1} (TLV7111525)

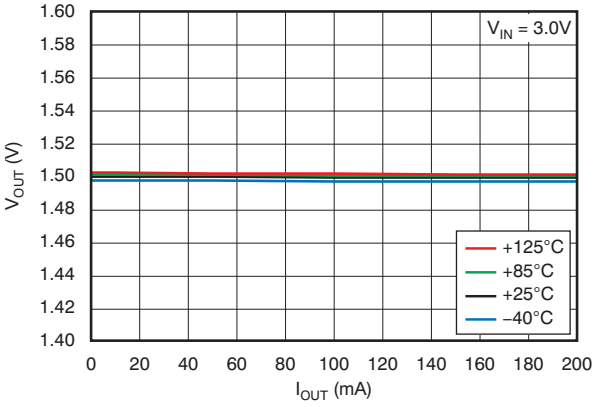

Figure 18.

LOAD REGULATION: V_{OUT2} (TLV7111525)

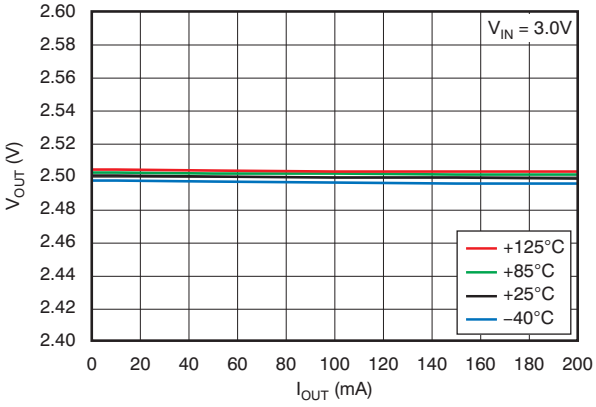

Figure 19.

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TYPICAL CHARACTERISTICS (continued)

Over operating temperature range of T_J = –40°C to +125°C, $V_{EN1} = V_{EN2} = V_{IN}$, C_{IN} = 1µF, C_{OUT1} = 1µF, and C_{OUT2} = 1µF, unless otherwise noted. Typical values are at T_J = +25°C.

DROPOUT VOLTAGE vs INPUT VOLTAGE

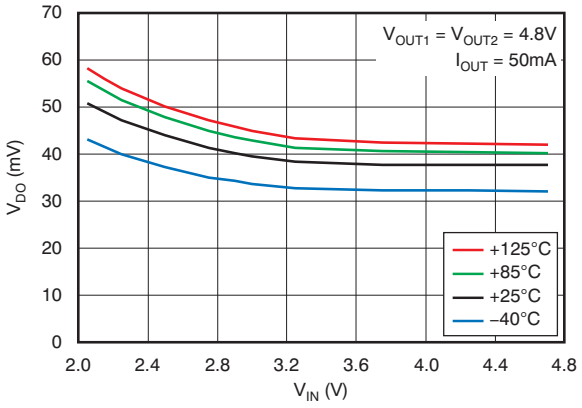

Figure 20.

DROPOUT VOLTAGE vs INPUT VOLTAGE

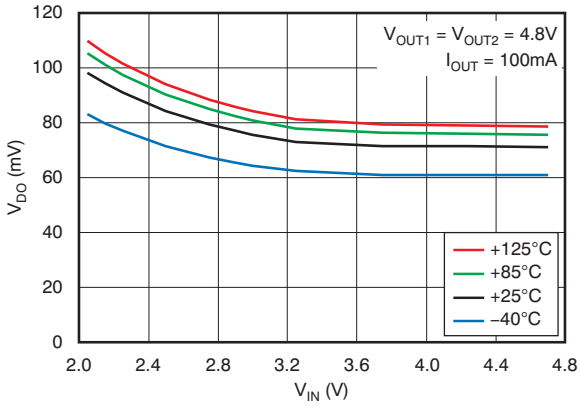

Figure 21.

DROPOUT VOLTAGE vs INPUT VOLTAGE

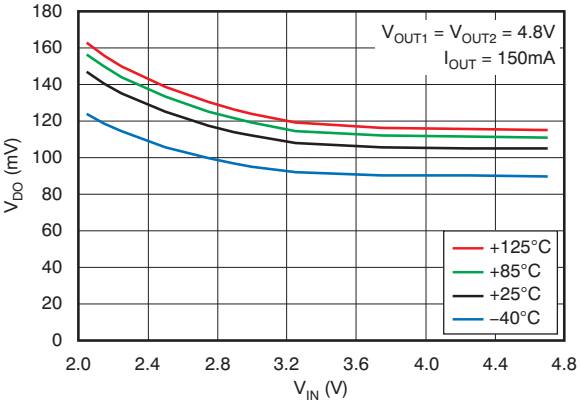

Figure 22.

DROPOUT VOLTAGE vs INPUT VOLTAGE

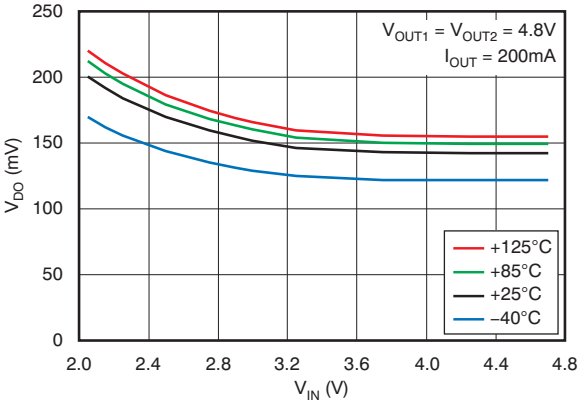

Figure 23.

DROPOUT VOLTAGE vs OUTPUT CURRENT: V_{OUT2} (TLV7101828)

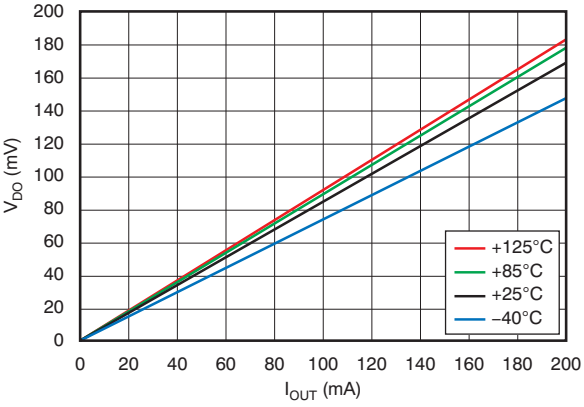

Figure 24.

DROPOUT VOLTAGE vs OUTPUT CURRENT: V_{OUT1}/V_{OUT2} (TLV7103333)

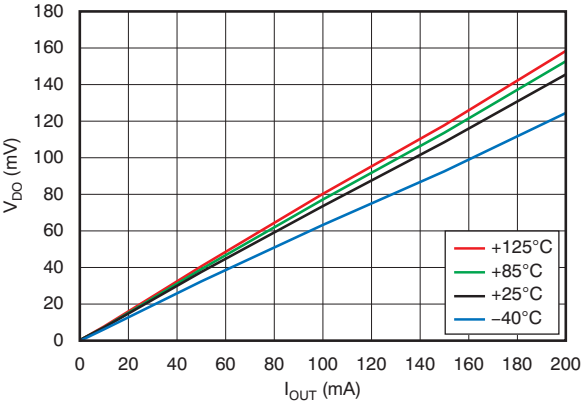

Figure 25.

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TYPICAL CHARACTERISTICS (continued)

Over operating temperature range of T_J = –40°C to +125°C, $V_{EN1} = V_{EN2} = V_{IN}$, C_{IN} = 1µF, C_{OUT1} = 1µF, and C_{OUT2} = 1µF, unless otherwise noted. Typical values are at T_J = +25°C.

DROPOUT VOLTAGE vs OUTPUT CURRENT: V_{OUT2} (TLV7111525)

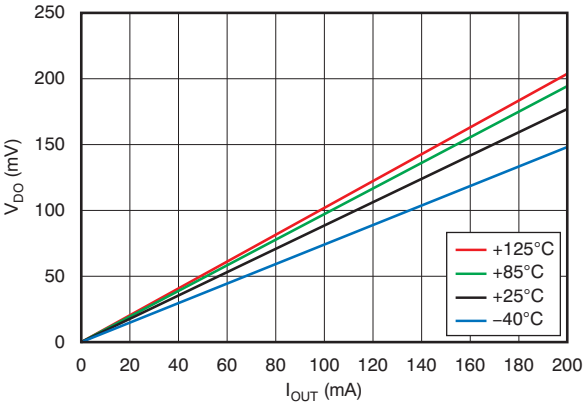

Figure 26.

OUTPUT VOLTAGE vs TEMPERATURE: V_{OUT1} (TLV7101828)

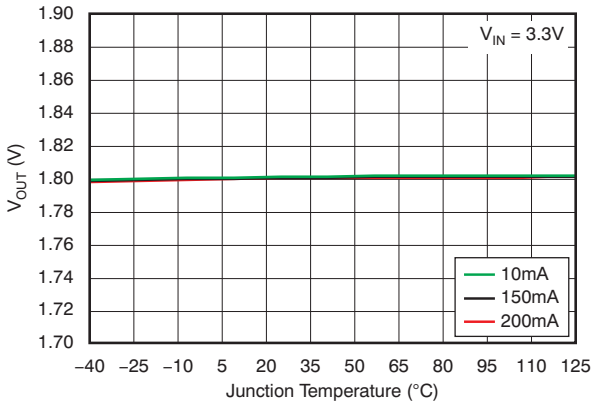

Figure 27.

OUTPUT VOLTAGE vs TEMPERATURE: V_{OUT2} (TLV7101828)

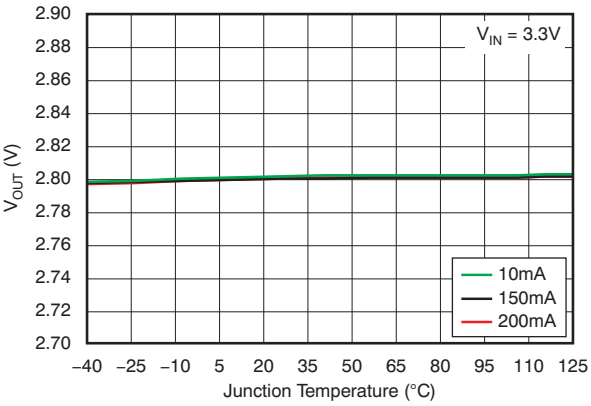

Figure 28.

OUTPUT VOLTAGE vs TEMPERATURE: V_{OUT1} (TLV7103333)

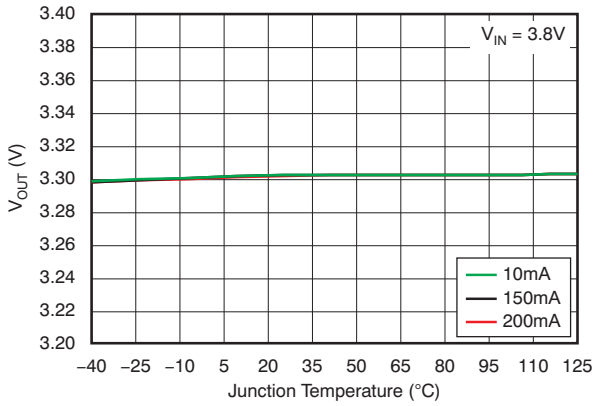

Figure 29.

OUTPUT VOLTAGE vs TEMPERATURE: V_{OUT2} (TLV7103333)

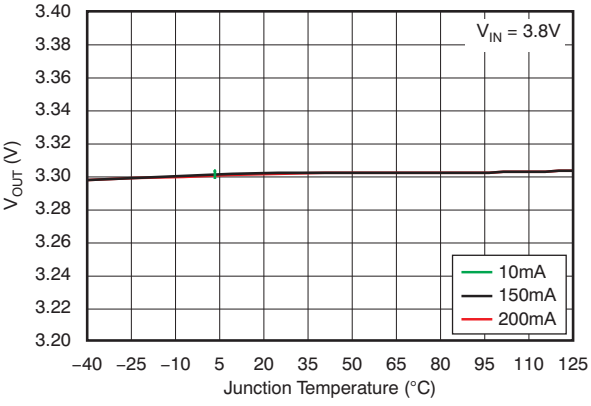

Figure 30.

OUTPUT VOLTAGE vs TEMPERATURE: V_{OUT1} (TLV7111525)

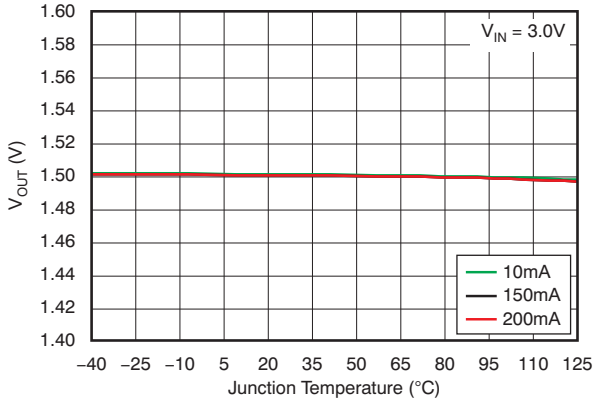

Figure 31.

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TYPICAL CHARACTERISTICS (continued)

Over operating temperature range of T_J = –40°C to +125°C, $V_{EN1} = V_{EN2} = V_{IN}$, C_{IN} = 1µF, C_{OUT1} = 1µF, and C_{OUT2} = 1µF, unless otherwise noted. Typical values are at T_J = +25°C.

OUTPUT VOLTAGE vs TEMPERATURE: V_{OUT2} (TLV7111525)

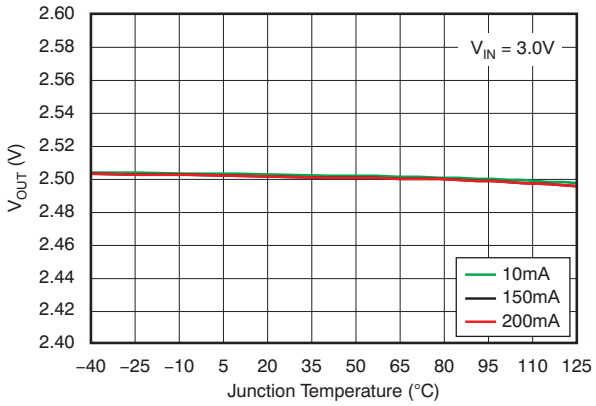

Figure 32.

GROUND PIN CURRENT vs INPUT VOLTAGE: I_{Q1} (TLV7101828)

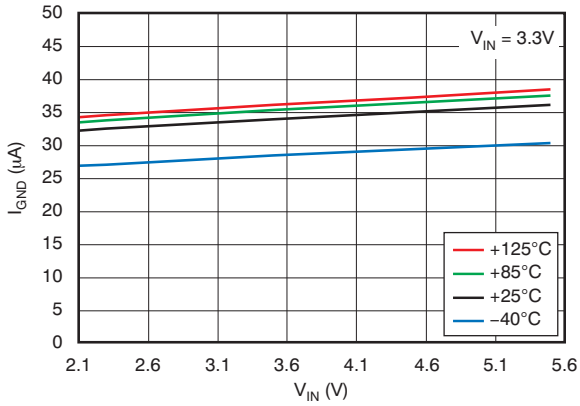

Figure 33.

GROUND PIN CURRENT vs INPUT VOLTAGE: I_{Q2} (TLV7101828)

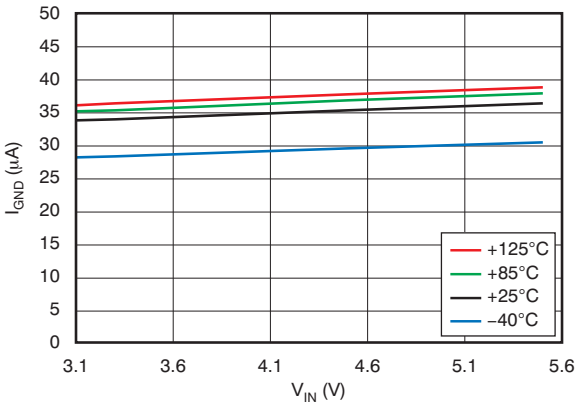

Figure 34.

GROUND PIN CURRENT vs INPUT VOLTAGE: I_{Q1} (TLV7103333)

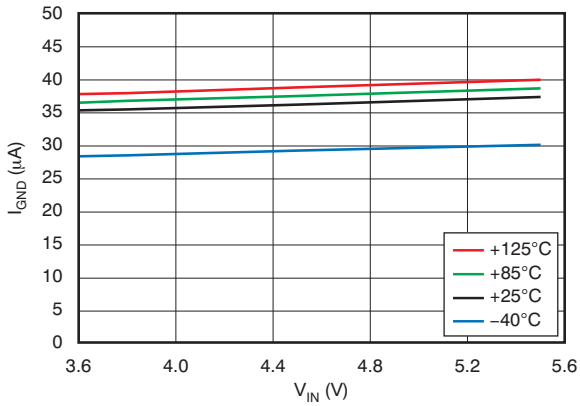

Figure 35.

GROUND PIN CURRENT vs INPUT VOLTAGE: I_{Q2} (TLV7103333)

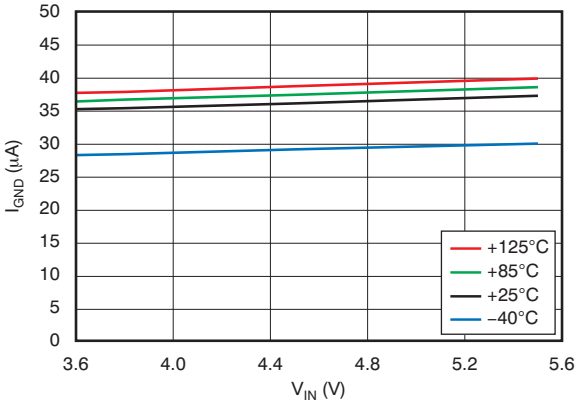

Figure 36.

GROUND PIN CURRENT vs INPUT VOLTAGE: I_{Q1} (TLV7111525)

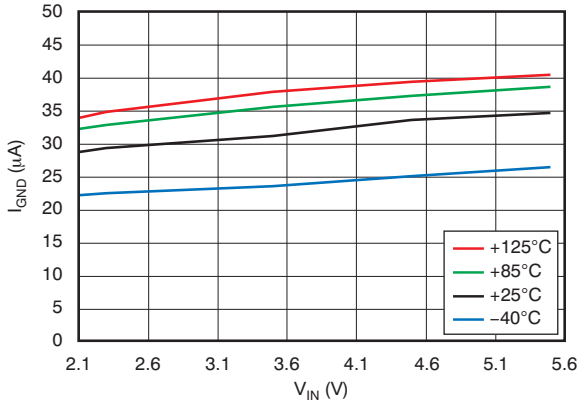

Figure 37.

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TYPICAL CHARACTERISTICS (continued)

Over operating temperature range of T_J = –40°C to +125°C, $V_{EN1} = V_{EN2} = V_{IN}$, C_{IN} = 1µF, C_{OUT1} = 1µF, and C_{OUT2} = 1µF, unless otherwise noted. Typical values are at T_J = +25°C.

GROUND PIN CURRENT vs INPUT VOLTAGE: I_{Q2} (TLV7111525)

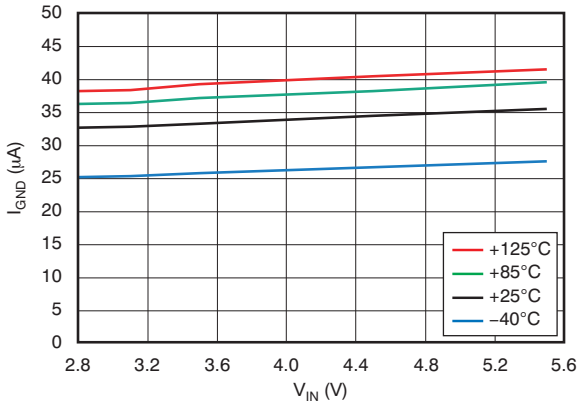

Figure 38.

GROUND PIN CURRENT vs LOAD: I_{Q1} (TLV7101828)

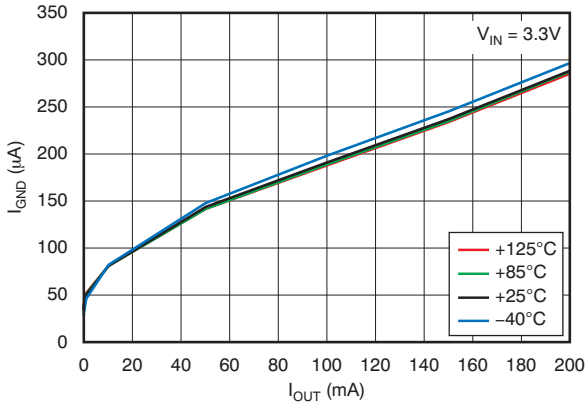

Figure 39.

GROUND PIN CURRENT vs LOAD: I_{Q2} (TLV7103333)

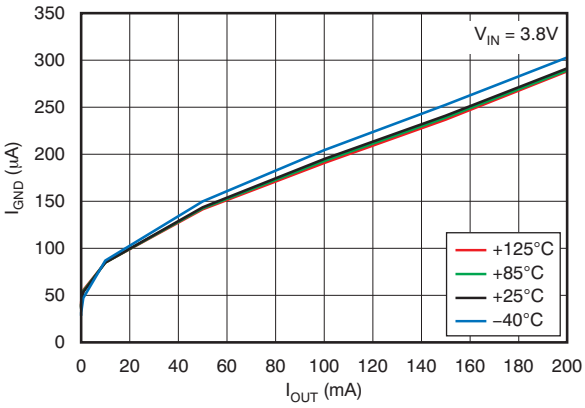

Figure 40.

GROUND PIN CURRENT vs LOAD: I_{Q1} (TLV7111525)

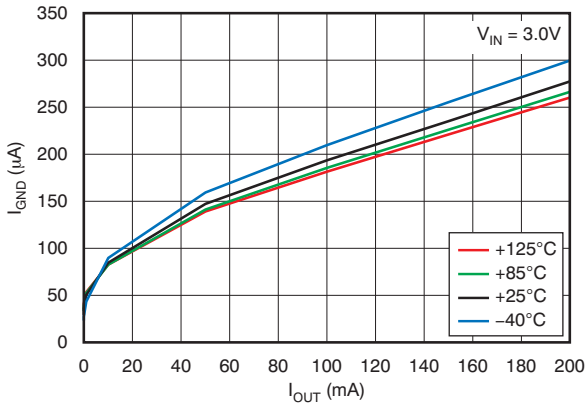

Figure 41.

SHUTDOWN CURRENT vs INPUT VOLTAGE (TLV7101828)

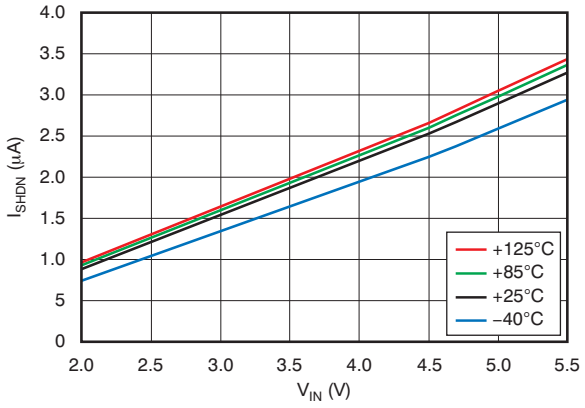

Figure 42.

SHUTDOWN CURRENT vs INPUT VOLTAGE (TLV7103333)

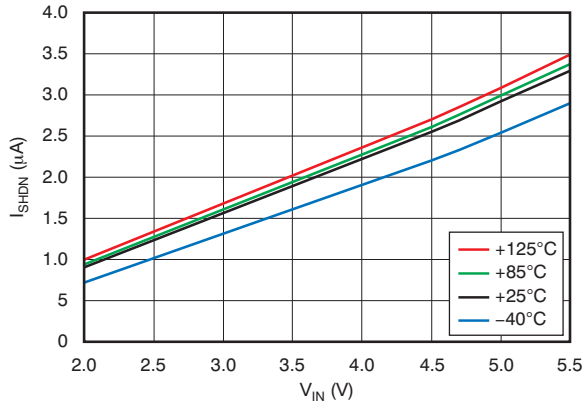

Figure 43.

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TYPICAL CHARACTERISTICS (continued)

Over operating temperature range of T_J = –40°C to +125°C, $V_{EN1} = V_{EN2} = V_{IN}$, C_{IN} = 1µF, C_{OUT1} = 1µF, and C_{OUT2} = 1µF, unless otherwise noted. Typical values are at T_J = +25°C.

SHUTDOWN CURRENT vs INPUT VOLTAGE (TLV7111525)

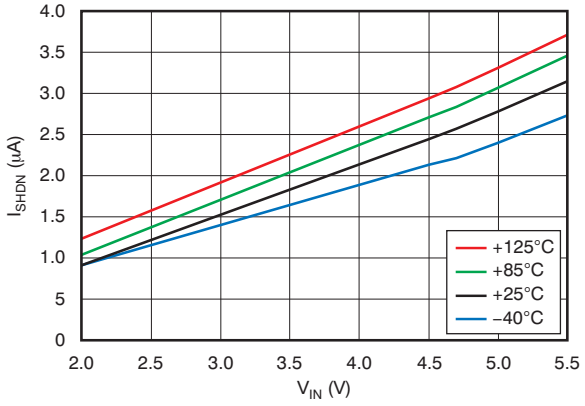

Figure 44.

CURRENT LIMIT vs INPUT VOLTAGE: I_{CL1} (TLV7101828)

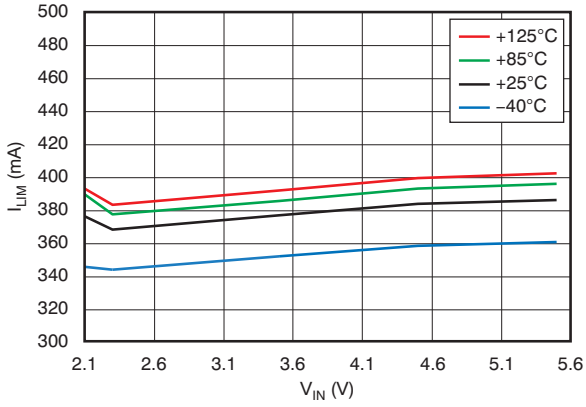

Figure 45.

CURRENT LIMIT vs INPUT VOLTAGE: I_{CL2} (TLV7101828)

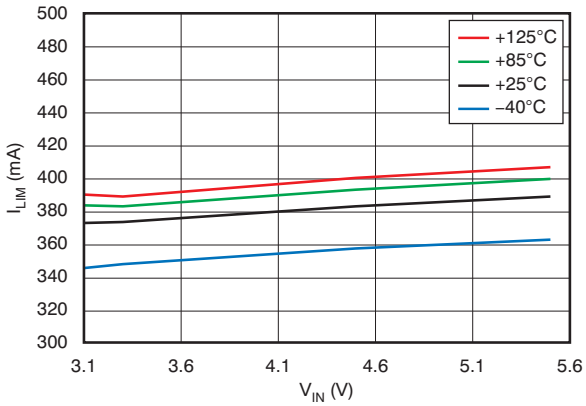

Figure 46.

CURRENT LIMIT vs INPUT VOLTAGE: I_{CL1} (TLV7103333)

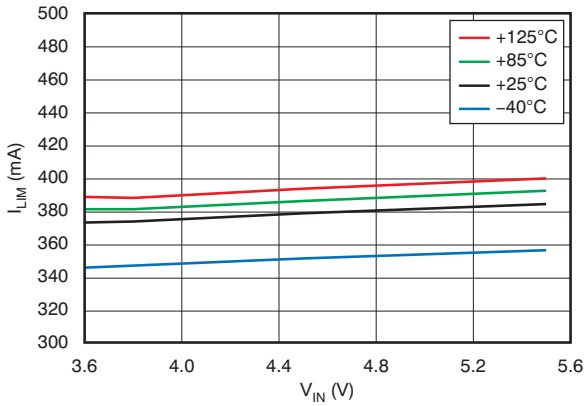

Figure 47.

CURRENT LIMIT vs INPUT VOLTAGE: I_{CL2} (TLV7103333)

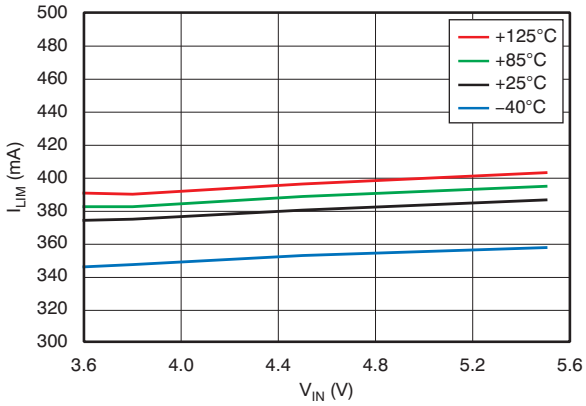

Figure 48.

CURRENT LIMIT vs INPUT VOLTAGE: I_{CL1} (TLV7111525)

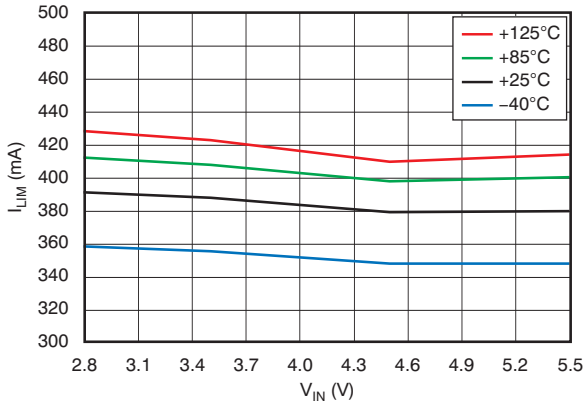

Figure 49.

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TYPICAL CHARACTERISTICS (continued)

Over operating temperature range of T_J = –40°C to +125°C, $V_{EN1} = V_{EN2} = V_{IN}$, C_{IN} = 1µF, C_{OUT1} = 1µF, and C_{OUT2} = 1µF, unless otherwise noted. Typical values are at T_J = +25°C.

CURRENT LIMIT vs INPUT VOLTAGE: I_{CL2} (TLV7111525)

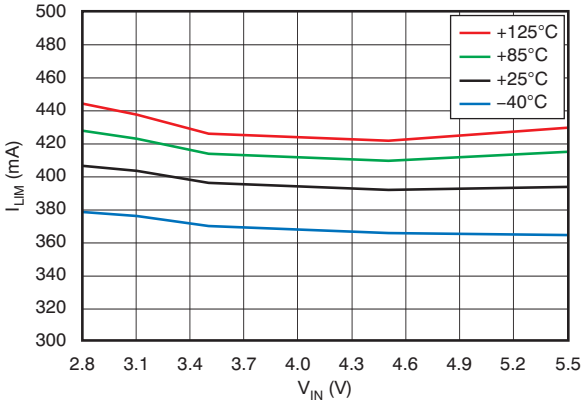

Figure 50.

POWER-SUPPLY RIPPLE REJECTION vs FREQUENCY (TLV7101828)

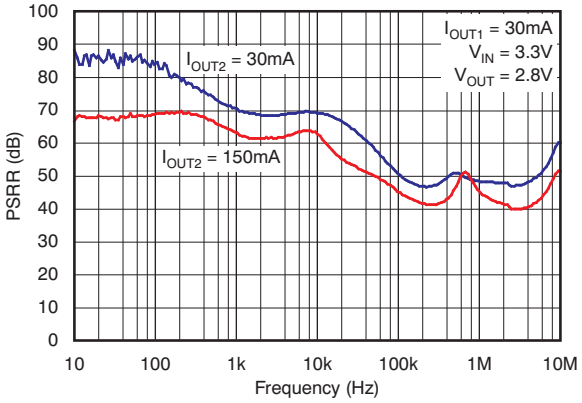

Figure 51.

POWER-SUPPLY RIPPLE REJECTION vs FREQUENCY (TLV7103333)

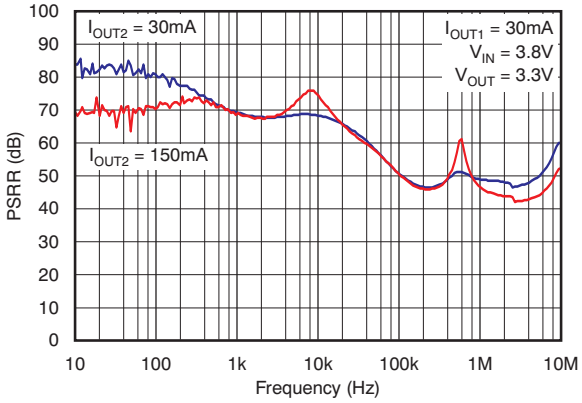

Figure 52.

POWER-SUPPLY RIPPLE REJECTION vs FREQUENCY (TLV7111525)

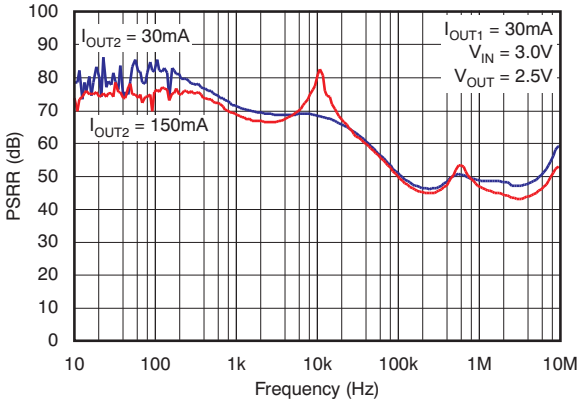

Figure 53.

OUTPUT SPECTRAL NOISE DENSITY vs FREQUENCY (TLV7101828)

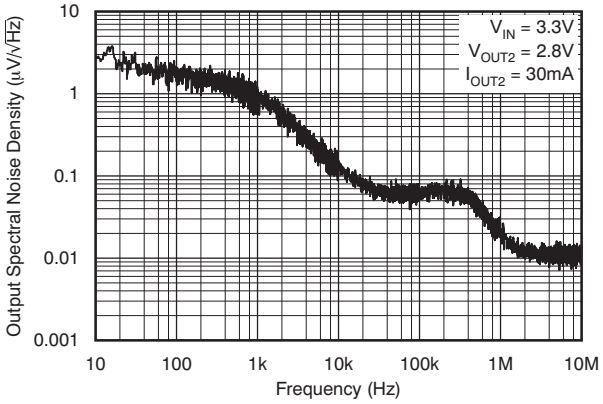

Figure 54.

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TYPICAL CHARACTERISTICS (continued)

Over operating temperature range of T_J = –40°C to +125°C, $V_{EN1} = V_{EN2} = V_{IN}$, C_{IN} = 1µF, C_{OUT1} = 1µF, and C_{OUT2} = 1µF, unless otherwise noted. Typical values are at T_J = +25°C.

OUTPUT SPECTRAL NOISE DENSITY vs FREQUENCY (TLV7103333)

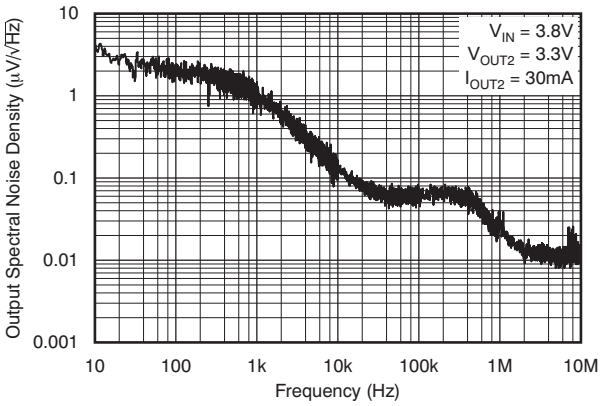

Figure 55.

OUTPUT SPECTRAL NOISE DENSITY vs FREQUENCY (TLV7111525)

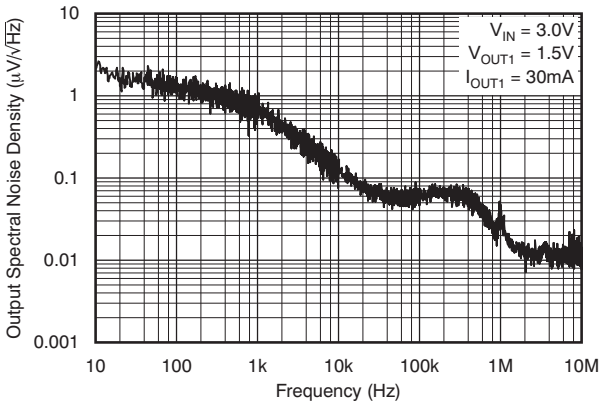

Figure 56.

LINE TRANSIENT RESPONSE V_{OUT1} = 1.2V, V_{OUT2} = 1.2V

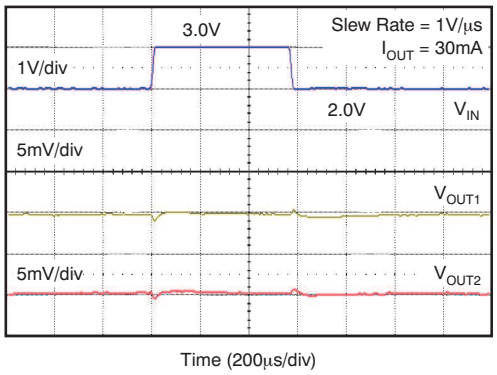

Figure 57.

LINE TRANSIENT RESPONSE V_{OUT1} = 1.2V, V_{OUT2} = 1.2V

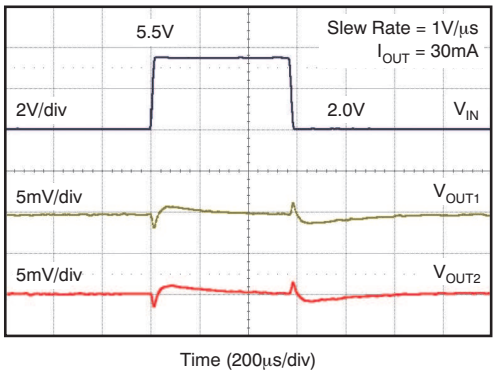

Figure 58.

LINE TRANSIENT RESPONSE V_{OUT1} = 1.8V, V_{OUT2} = 2.8V

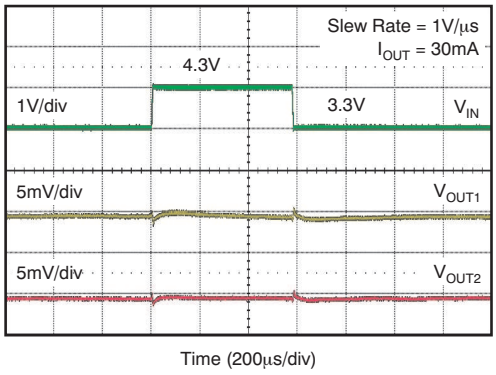

Figure 59.

LINE TRANSIENT RESPONSE V_{OUT1} = 1.8V, V_{OUT2} = 2.8V

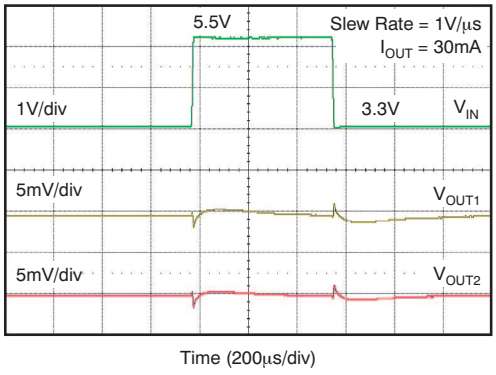

Figure 60.

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TYPICAL CHARACTERISTICS (continued)

Over operating temperature range of T_J = –40°C to +125°C, $V_{EN1} = V_{EN2} = V_{IN}$, C_{IN} = 1µF, C_{OUT1} = 1µF, and C_{OUT2} = 1µF, unless otherwise noted. Typical values are at T_J = +25°C.

LINE TRANSIENT RESPONSE
V_{OUT1} = 4.8V, V_{OUT2} = 4.8V

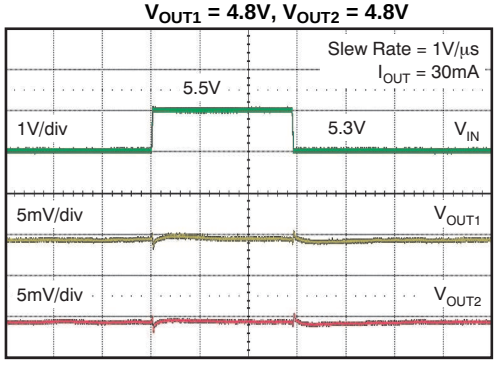

Figure 61.

LOAD TRANSIENT RESPONSE AND CROSSTALK
V_{OUT1} = 1.2V, V_{OUT2} = 1.2V

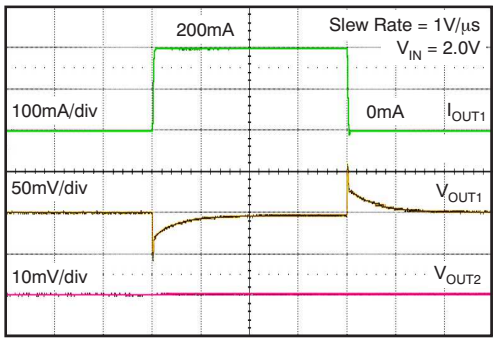

Figure 62.

LOAD TRANSIENT RESPONSE AND CROSSTALK
V_{OUT1} = 1.2V, V_{OUT2} = 1.2V

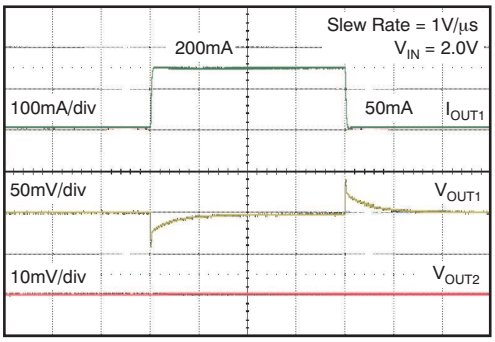

Figure 63.

LOAD TRANSIENT RESPONSE AND CROSSTALK
V_{OUT1} = 1.8V, V_{OUT2} = 2.8V

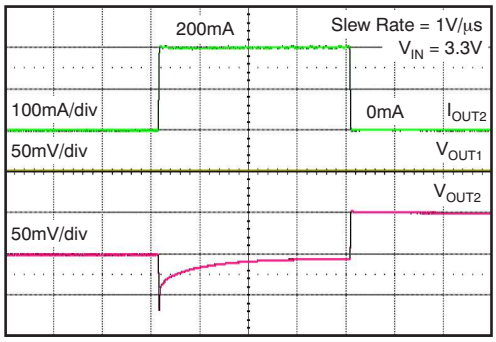

Figure 64.

LOAD TRANSIENT RESPONSE AND CROSSTALK
V_{OUT1} = 1.8V, V_{OUT2} = 2.8V

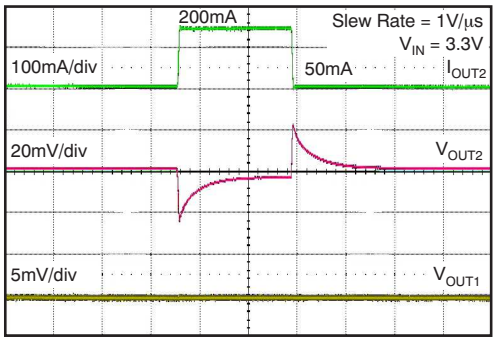

Figure 65.

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TYPICAL CHARACTERISTICS (continued)

Over operating temperature range of T_J = –40°C to +125°C, $V_{EN1} = V_{EN2} = V_{IN}$, C_{IN} = 1µF, C_{OUT1} = 1µF, and C_{OUT2} = 1µF, unless otherwise noted. Typical values are at T_J = +25°C.

LOAD TRANSIENT RESPONSE AND CROSSTALK
V_{OUT1} = 4.8V, V_{OUT2} = 4.8V

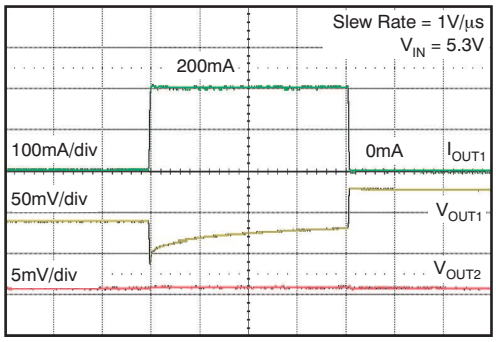

Figure 66.

LOAD TRANSIENT RESPONSE AND CROSSTALK
V_{OUT1} = 4.8V, V_{OUT2} = 4.8V

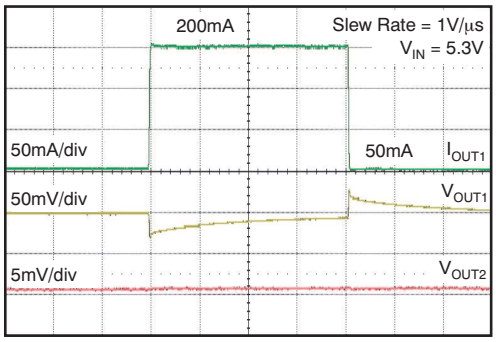

Figure 67.

V_{IN} RAMP UP, RAMP DOWN RESPONSE
V_{OUT1} = 1.2V, V_{OUT2} = 1.2V

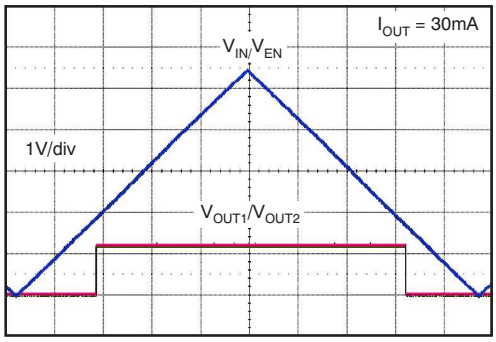

Figure 68.

V_{IN} RAMP UP, RAMP DOWN RESPONSE
V_{OUT1} = 1.8V, V_{OUT2} = 2.8V

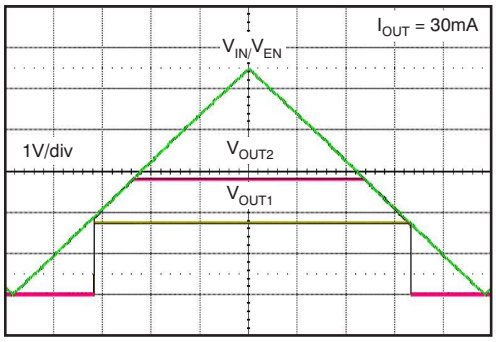

Figure 69.

V_{IN} RAMP UP, RAMP DOWN RESPONSE
V_{OUT1} = 4.8V, V_{OUT2} = 4.8V

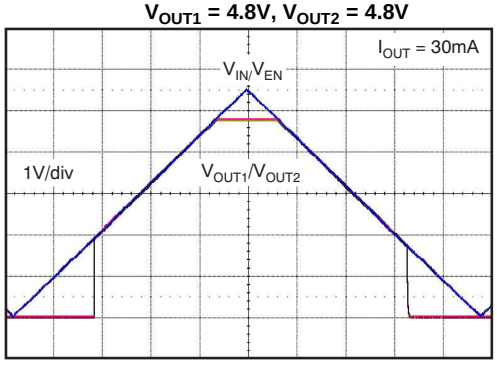

Figure 70.

APPLICATION INFORMATION

The TLV710 and TLV711 series of devices belong to a new family of next generation, value LDO regulators. These devices consume low quiescent current and deliver excellent line and load transient performance. These features, combined with low noise, very good PSRR with little (V_{IN} to V_{OUT}) headroom, make these devices ideal for RF portable applications. This family of LDO regulators offers current limit and thermal protection, and is specified from –40°C to +125°C.

INPUT AND OUTPUT CAPACITOR REQUIREMENTS

1.0µF X5R- and X7R-type ceramic capacitors are recommended because they have minimal variation in value and equivalent series resistance (ESR) over temperature.

However, the TLV710 and TLV711 are designed to be stable with an effective capacitance of 0.1µF or larger at the output. Thus, the device would also be stable with capacitors of other dielectrics, as long as the effective capacitance under operating bias voltage and temperature is greater than 0.1µF. This effective capacitance refers to the capacitance that the device sees under operating bias voltage and temperature conditions (that is, the capacitance after taking bias voltage and temperature derating into consideration.)

In addition to allowing the use of cost-effective dielectrics, these devices also enable using smaller footprint capacitors that have a higher derating in size-constrained applications.

Note that using a 0.1µF rating capacitor at the output of the LDO regulator does not ensure stability because the effective capacitance under operating conditions would be less than 0.1µF. The maximum ESR should be less than 200mΩ.

Although an input capacitor is not required for stability, it is good analog design practice to connect a 0.1µF to 1.0µF low ESR capacitor across the IN and GND pins of the regulator. This capacitor counteracts reactive input sources and improves transient response, noise rejection, and ripple rejection. A higher-value capacitor may be necessary if large, fast-rise-time load transients are anticipated, or if the device is not located near the power source. If source impedance is more than 2Ω, a 0.1µF input capacitor may be necessary to ensure stability.

BOARD LAYOUT RECOMMENDATIONS TO IMPROVE PSRR AND NOISE PERFORMANCE

Input and output capacitors should be placed as close to the device pins as possible. To improve ac performance such as PSRR, output noise, and transient response, it is recommended that the board be designed with separate ground planes for V_{IN} and V_{OUT}, with the ground plane connected only at the GND pin of the device. In addition, the ground connection for the output capacitor should be connected directly to the GND pin of the device. High ESR capacitors may degrade PSRR.

INTERNAL CURRENT LIMIT

The TLV710 and TLV711 internal current limits help protect the regulator during fault conditions. During current limit, the output sources a fixed amount of current that is largely independent of output voltage. In such a case, the output voltage is not regulated, and is $V_{OUT} = I_{LIMIT} \times R_{LOAD}$.

The PMOS pass transistor dissipates $(V_{IN} – V_{OUT}) \times I_{LIMIT}$ until thermal shutdown is triggered and the device is turned off. As the device cools down, it is turned on by the internal thermal shutdown circuit. If the fault condition continues, the device cycles between current limit and thermal shutdown. See the *Thermal Information* section for more details. The PMOS pass element in the TLV710 and TLV711 has a built-in body diode that conducts current when the voltage at OUT exceeds the voltage at IN. This current is not limited, so if extended reverse voltage operation is anticipated, external limiting to 5% of rated output current is recommended.

SHUTDOWN

The enable pin (EN) is active high. The device is enabled when EN pin goes above 0.9V. This relatively lower value of voltage needed to turn the LDO regulator on can be used to enable the device with the GPIO of recent processors whose GPIO voltage is lower than traditional microcontrollers.

The device is turned off when the EN pin is held at less than 0.4V. When shutdown capability is not required, the EN pin can connected to the IN pin.

The TLV711 has internal pull-down circuitry that discharges output with a time constant of:

$$\tau = \frac{120 \cdot R_L}{120 + R_L} \cdot C_{OUT} \quad (1)$$

Where:

R_L = load resistance

C_{OUT} = output capacitor

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DROPOUT VOLTAGE

The TLV710 and TLV711 use a PMOS pass transistor to achieve low dropout. When (V_{IN} – V_{OUT}) is less than the dropout voltage (V_{DO}), the PMOS pass device is in the linear region of operation and the input-to-output resistance is the $R_{DS(ON)}$ of the PMOS pass element. V_{DO} scales approximately with the output current because the PMOS device behaves as a resistor in dropout.

As with any linear regulator, PSRR and transient response are degraded as (V_{IN} – V_{OUT}) approaches dropout.

TRANSIENT RESPONSE

As with any regulator, increasing the size of the output capacitor reduces over/undershoot magnitude but increases duration of the transient response.

The TLV710 and TLV711 each have a dedicated V_{REF}. Consequently, crosstalk from one channel to the other as a result of transients is close to 0V.

UNDERVOLTAGE LOCKOUT (UVLO)

The TLV710 and TLV711 use an undervoltage lockout circuit to keep the output shut off until the internal circuitry is operating properly.

THERMAL INFORMATION

Thermal protection disables the output when the junction temperature rises to approximately +165°C, allowing the device to cool. When the junction temperature cools to approximately +145°C, the output circuitry is again enabled. Depending on power dissipation, thermal resistance, and ambient temperature, the thermal protection circuit may cycle on and off. This cycling limits the dissipation of the regulator, protecting it from damage as a result of overheating.

Any tendency to activate the thermal protection circuit indicates excessive power dissipation or an inadequate heatsink. For reliable operation, junction temperature should be limited to +125°C maximum. To estimate the margin of safety in a complete design (including heatsink), increase the ambient temperature until the thermal protection is triggered; use worst-case loads and signal conditions. For good reliability, thermal protection should trigger at least +35°C above the maximum expected ambient condition of the particular application. This configuration produces a worst-case junction temperature of +125°C at the highest expected ambient temperature and worst-case load.

The internal protection circuitry of the TLV710 and TLV711 has been designed to protect against overload conditions. It was not intended to replace proper heatsinking. Continuously running the TLV710/ TLV711 into thermal shutdown degrades device reliability.

POWER DISSIPATION

The ability to remove heat from a die is different for each package type, presenting different considerations in the printed circuit board (PCB) layout. The PCB area around the device that is free of other components moves the heat from the device to the ambient air.

Performance data for the TLV710 evaluation module (EVM) are shown in Table 1. The EVM is a 2-layer board with 2 ounces of copper per side. The dimension and layout are shown in Figure 71 and Figure 72. Using heavier copper increases the effectiveness of removing heat from the device. The addition of plated through-holes in the heat-dissipating layer also improves the heatsink effectiveness. Power dissipation depends on input voltage and load conditions.

Power dissipation (P_D) is equal to the product of the output current and the voltage drop across the output pass element, as shown in Equation 2:

$$P_D = (V_{IN} – V_{OUT}) \times I_{OUT} \quad (2)$$

PACKAGE MOUNTING

Solder pad footprint recommendations for the TLV710 and TLV711 are available from the Texas Instruments Web site at www.ti.com. The recommended land pattern for the DSE (SON-6) package is shown in Figure 73.

Table 1. TLV710 EVM Dissipation Ratings

PACKAGE	$R_{\theta JA}$	T_A < +25°C	T_A = +70°C	T_A = +85°C
DSE	170°C/W	585mW	320mW	235mW

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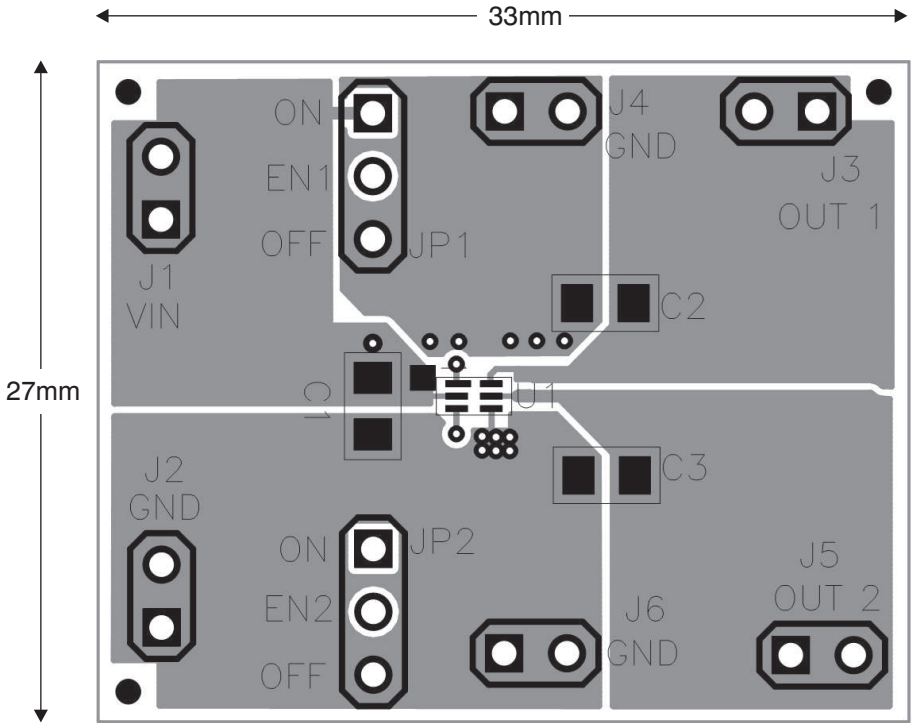

Figure 71. Top Layer

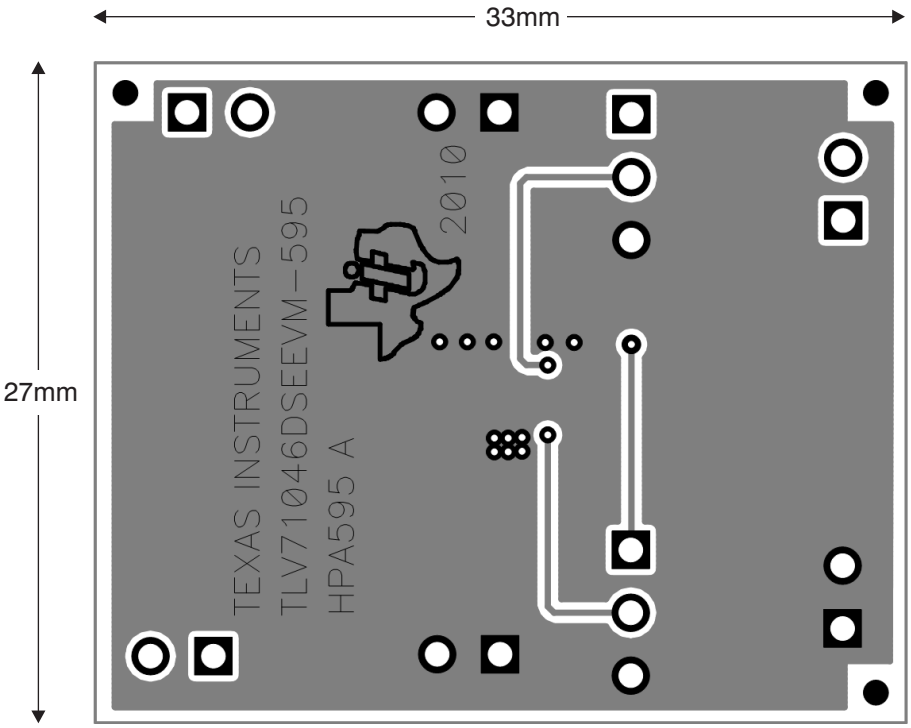

Figure 72. Bottom Layer

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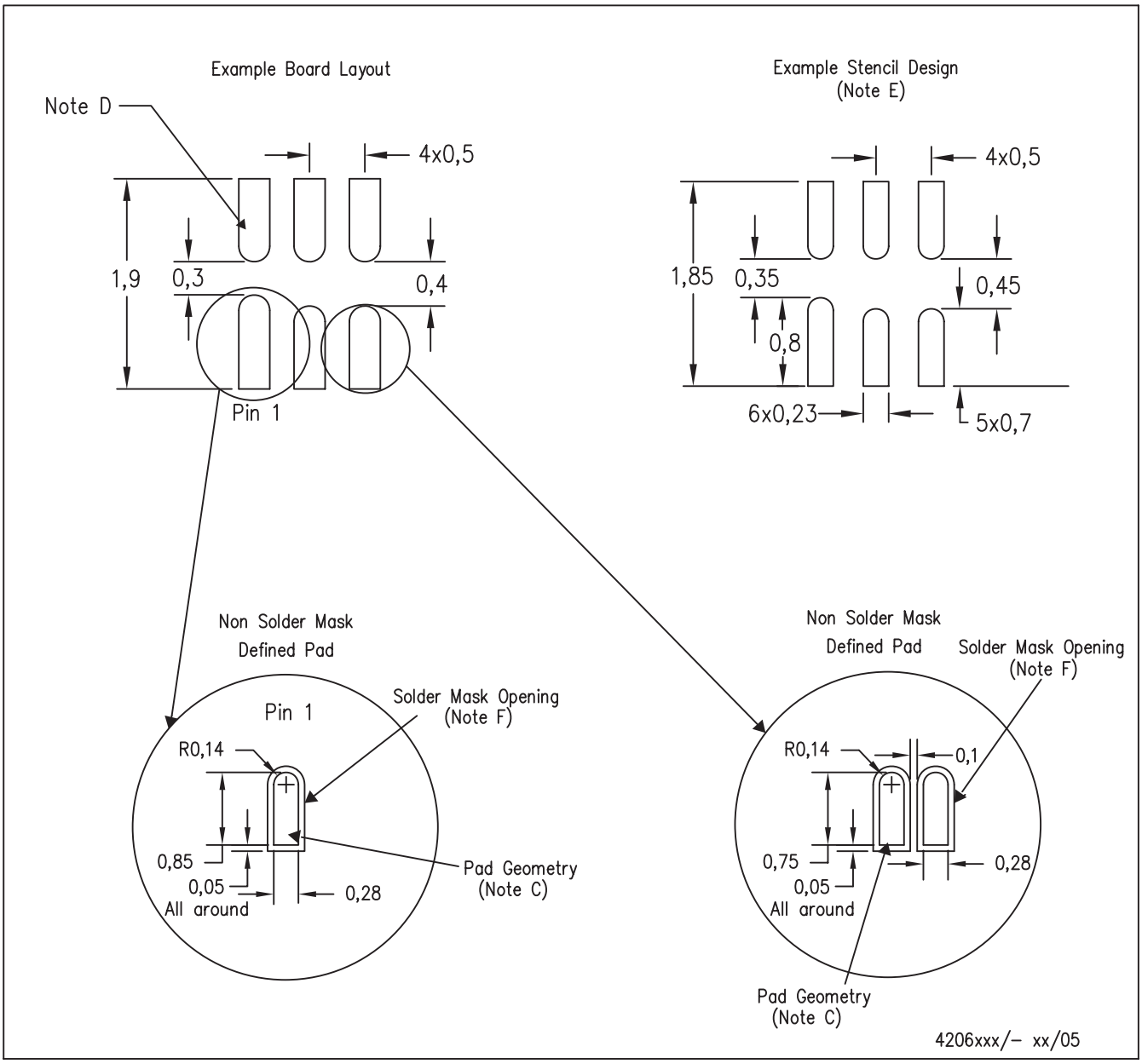
DSE (S–PDSO–N6)



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is a QFN that does not have a thermal pad on the board. Refer to Application Note, Quad Flat–Pack Packages, Texas Instruments Literature No. SCBA017, SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.

Figure 73. Land Pattern Drawing for DSE (SON-6) Package

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TLV7101828DSER	ACTIVE	WSON	DSE	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	QW	Samples
TLV7101828DSET	ACTIVE	WSON	DSE	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	QW	Samples
TLV7103318DSER	ACTIVE	WSON	DSE	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	UE	Samples
TLV7103318DSET	ACTIVE	WSON	DSE	6	250	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	UE	Samples
TLV7111225DSER	ACTIVE	WSON	DSE	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	BT	Samples
TLV7111225DSET	ACTIVE	WSON	DSE	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	BT	Samples
TLV7111233DSER	ACTIVE	WSON	DSE	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	TP	Samples
TLV7111233DSET	ACTIVE	WSON	DSE	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	TP	Samples
TLV7111323DDSER	ACTIVE	WSON	DSE	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	WH	Samples
TLV7111323DDSET	ACTIVE	WSON	DSE	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	WH	Samples
TLV7111333DDSER	ACTIVE	WSON	DSE	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	YY	Samples
TLV7111333DDSET	ACTIVE	WSON	DSE	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	YY	Samples
TLV7111518DDSER	ACTIVE	WSON	DSE	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU | CU NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	UT	Samples
TLV7111518DDSET	ACTIVE	WSON	DSE	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU | CU NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	UT	Samples
TLV7111533DDSER	ACTIVE	WSON	DSE	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	YD	Samples
TLV7111533DDSET	ACTIVE	WSON	DSE	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	YD	Samples
TLV7111812DSER	ACTIVE	WSON	DSE	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	BS	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TLV7111812DSET	ACTIVE	WSON	DSE	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	BS	Samples
TLV7111830DSER	ACTIVE	WSON	DSE	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	GB	Samples
TLV7111830DSET	ACTIVE	WSON	DSE	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	GB	Samples
TLV7111833DDSER	ACTIVE	WSON	DSE	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU | CU NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	UQ	Samples
TLV7111833DDSET	ACTIVE	WSON	DSE	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU | CU NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	UQ	Samples
TLV7111930DSER	ACTIVE	WSON	DSE	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	CV	Samples
TLV7111930DSET	ACTIVE	WSON	DSE	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	CV	Samples
TLV71125125DSER	ACTIVE	WSON	DSE	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	TM	Samples
TLV71125125DSET	ACTIVE	WSON	DSE	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	TM	Samples
TLV7112525DSER	ACTIVE	WSON	DSE	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	SX	Samples
TLV7112525DSET	ACTIVE	WSON	DSE	6	250	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	SX	Samples
TLV71128512DSER	ACTIVE	WSON	DSE	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	9M	Samples
TLV71128512DSET	ACTIVE	WSON	DSE	6	250	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	9M	Samples
TLV71128518DDSER	ACTIVE	WSON	DSE	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU | CU NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	WV	Samples
TLV71128518DDSET	ACTIVE	WSON	DSE	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	WV	Samples
TLV711285285DDSER	ACTIVE	WSON	DSE	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU | CU NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	UU	Samples
TLV711285285DDSET	ACTIVE	WSON	DSE	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU | CU NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	UU	Samples
TLV7113025DSER	ACTIVE	WSON	DSE	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	BR	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TLV7113025DSET	ACTIVE	WSON	DSE	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	BR	Samples
TLV7113030DDSER	ACTIVE	WSON	DSE	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	WS	Samples
TLV7113030DDSET	ACTIVE	WSON	DSE	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	WS	Samples
TLV7113318DDSER	ACTIVE	WSON	DSE	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU | CU NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	VW	Samples
TLV7113318DDSET	ACTIVE	WSON	DSE	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU | CU NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	VW	Samples
TLV71133285DDSER	ACTIVE	WSON	DSE	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU | CU NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	YE	Samples
TLV71133285DDSET	ACTIVE	WSON	DSE	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	YE	Samples
TLV7113330DDSER	ACTIVE	WSON	DSE	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU | CU NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	WZ	Samples
TLV7113330DDSET	ACTIVE	WSON	DSE	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	WZ	Samples
TLV7113333DDSER	ACTIVE	WSON	DSE	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU | CU NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	RV	Samples
TLV7113333DDSET	ACTIVE	WSON	DSE	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU | CU NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	RV	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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OTHER QUALIFIED VERSIONS OF TLV7101828, TLV7103318 :

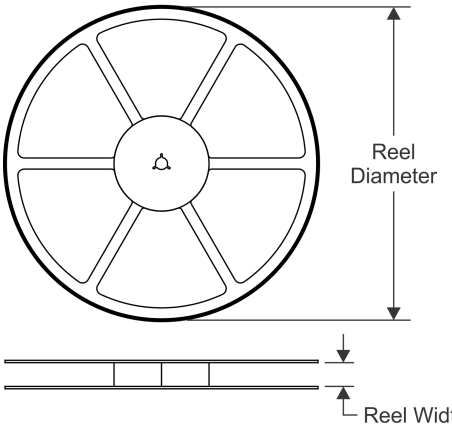
- Automotive: TLV7101828-Q1, TLV7103318-Q1

NOTE: Qualified Version Definitions:

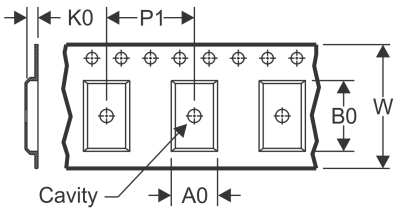
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

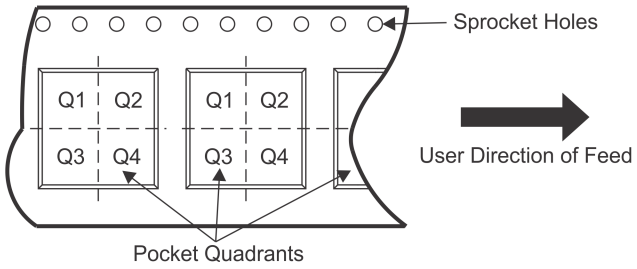


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



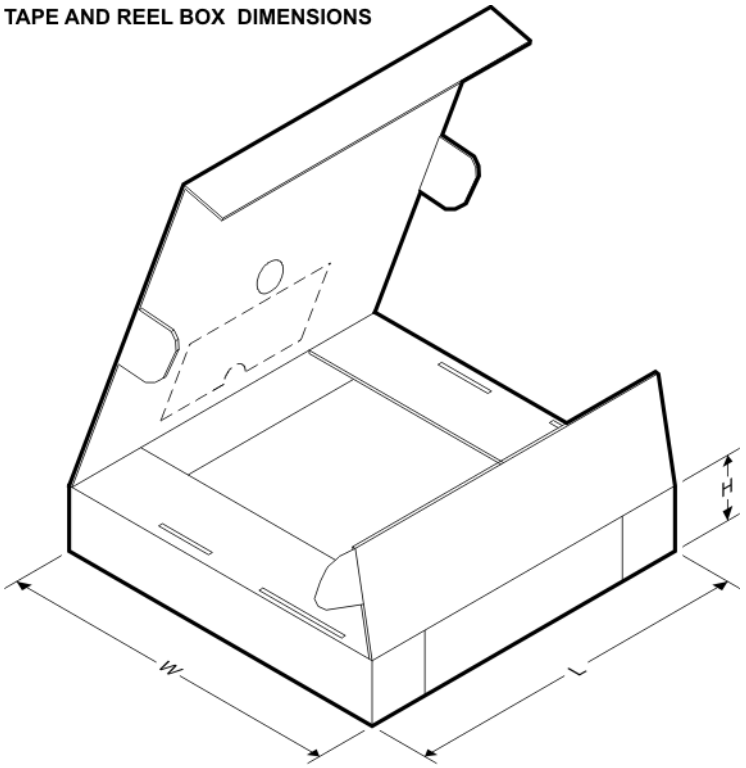
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLV7101828DSER	WSON	DSE	6	3000	179.0	8.4	1.8	1.8	1.0	4.0	8.0	Q2
TLV7101828DSET	WSON	DSE	6	250	179.0	8.4	1.8	1.8	1.0	4.0	8.0	Q2
TLV7103318DSER	WSON	DSE	6	3000	179.0	8.4	1.8	1.8	1.0	4.0	8.0	Q2
TLV7103318DSET	WSON	DSE	6	250	179.0	8.4	1.8	1.8	1.0	4.0	8.0	Q2
TLV7111225DSER	WSON	DSE	6	3000	180.0	8.4	1.83	1.83	0.89	4.0	8.0	Q2
TLV7111225DSET	WSON	DSE	6	250	180.0	8.4	1.83	1.83	0.89	4.0	8.0	Q2
TLV7111233DSER	WSON	DSE	6	3000	180.0	8.4	1.83	1.83	0.89	4.0	8.0	Q2
TLV7111233DSET	WSON	DSE	6	250	180.0	8.4	1.83	1.83	0.89	4.0	8.0	Q2
TLV7111323DDSER	WSON	DSE	6	3000	179.0	8.4	1.8	1.8	1.0	4.0	8.0	Q2
TLV7111323DDSET	WSON	DSE	6	250	179.0	8.4	1.8	1.8	1.0	4.0	8.0	Q2
TLV7111333DDSER	WSON	DSE	6	3000	179.0	8.4	1.8	1.8	1.0	4.0	8.0	Q2
TLV7111333DDSET	WSON	DSE	6	250	179.0	8.4	1.8	1.8	1.0	4.0	8.0	Q2
TLV7111518DDSER	WSON	DSE	6	3000	179.0	8.4	1.8	1.8	1.0	4.0	8.0	Q2
TLV7111518DDSER	WSON	DSE	6	3000	178.0	8.4	1.7	1.7	0.95	4.0	8.0	Q2
TLV7111518DDSET	WSON	DSE	6	250	179.0	8.4	1.8	1.8	1.0	4.0	8.0	Q2
TLV7111518DDSET	WSON	DSE	6	250	178.0	8.4	1.7	1.7	0.95	4.0	8.0	Q2
TLV7111533DDSER	WSON	DSE	6	3000	179.0	8.4	1.8	1.8	1.0	4.0	8.0	Q2
TLV7111533DDSET	WSON	DSE	6	250	179.0	8.4	1.8	1.8	1.0	4.0	8.0	Q2

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLV7111812DSER	WSON	DSE	6	3000	180.0	8.4	1.83	1.83	0.89	4.0	8.0	Q2
TLV7111812DSET	WSON	DSE	6	250	180.0	8.4	1.83	1.83	0.89	4.0	8.0	Q2
TLV7111830DSER	WSON	DSE	6	3000	180.0	8.4	1.83	1.83	0.89	4.0	8.0	Q2
TLV7111830DSET	WSON	DSE	6	250	180.0	8.4	1.83	1.83	0.89	4.0	8.0	Q2
TLV7111833DDSER	WSON	DSE	6	3000	179.0	8.4	1.8	1.8	1.0	4.0	8.0	Q2
TLV7111833DDSER	WSON	DSE	6	3000	178.0	8.4	1.7	1.7	0.95	4.0	8.0	Q2
TLV7111833DDSET	WSON	DSE	6	250	178.0	8.4	1.7	1.7	0.95	4.0	8.0	Q2
TLV7111833DDSET	WSON	DSE	6	250	179.0	8.4	1.8	1.8	1.0	4.0	8.0	Q2
TLV7111930DSER	WSON	DSE	6	3000	180.0	8.4	1.83	1.83	0.89	4.0	8.0	Q2
TLV7111930DSET	WSON	DSE	6	250	180.0	8.4	1.83	1.83	0.89	4.0	8.0	Q2
TLV71125125DSER	WSON	DSE	6	3000	180.0	8.4	1.83	1.83	0.89	4.0	8.0	Q2
TLV71125125DSET	WSON	DSE	6	250	180.0	8.4	1.83	1.83	0.89	4.0	8.0	Q2
TLV7112525DSER	WSON	DSE	6	3000	179.0	8.4	1.8	1.8	1.0	4.0	8.0	Q2
TLV7112525DSET	WSON	DSE	6	250	179.0	8.4	1.8	1.8	1.0	4.0	8.0	Q2
TLV71128512DSER	WSON	DSE	6	3000	180.0	8.4	1.83	1.83	0.89	4.0	8.0	Q2
TLV71128512DSET	WSON	DSE	6	250	180.0	8.4	1.83	1.83	0.89	4.0	8.0	Q2
TLV71128518DDSER	WSON	DSE	6	3000	179.0	8.4	1.8	1.8	1.0	4.0	8.0	Q2
TLV71128518DDSER	WSON	DSE	6	3000	178.0	8.4	1.7	1.7	0.95	4.0	8.0	Q2
TLV71128518DDSET	WSON	DSE	6	250	179.0	8.4	1.8	1.8	1.0	4.0	8.0	Q2
TLV71128518DDSET	WSON	DSE	6	250	178.0	8.4	1.7	1.7	0.95	4.0	8.0	Q2
TLV711285285DDSER	WSON	DSE	6	3000	179.0	8.4	1.8	1.8	1.0	4.0	8.0	Q2
TLV711285285DDSER	WSON	DSE	6	3000	178.0	8.4	1.7	1.7	0.95	4.0	8.0	Q2
TLV711285285DDSET	WSON	DSE	6	250	179.0	8.4	1.8	1.8	1.0	4.0	8.0	Q2
TLV711285285DDSET	WSON	DSE	6	250	178.0	8.4	1.7	1.7	0.95	4.0	8.0	Q2
TLV7113025DSER	WSON	DSE	6	3000	180.0	8.4	1.83	1.83	0.89	4.0	8.0	Q2
TLV7113025DSET	WSON	DSE	6	250	180.0	8.4	1.83	1.83	0.89	4.0	8.0	Q2
TLV7113030DDSER	WSON	DSE	6	3000	179.0	8.4	1.8	1.8	1.0	4.0	8.0	Q2
TLV7113030DDSET	WSON	DSE	6	250	179.0	8.4	1.8	1.8	1.0	4.0	8.0	Q2
TLV7113318DDSER	WSON	DSE	6	3000	178.0	8.4	1.7	1.7	0.95	4.0	8.0	Q2
TLV7113318DDSER	WSON	DSE	6	3000	179.0	8.4	1.8	1.8	1.0	4.0	8.0	Q2
TLV7113318DDSET	WSON	DSE	6	250	179.0	8.4	1.8	1.8	1.0	4.0	8.0	Q2
TLV7113318DDSET	WSON	DSE	6	250	178.0	8.4	1.7	1.7	0.95	4.0	8.0	Q2
TLV71133285DDSER	WSON	DSE	6	3000	178.0	8.4	1.7	1.7	0.95	4.0	8.0	Q2
TLV71133285DDSER	WSON	DSE	6	3000	179.0	8.4	1.8	1.8	1.0	4.0	8.0	Q2
TLV71133285DDSET	WSON	DSE	6	250	179.0	8.4	1.8	1.8	1.0	4.0	8.0	Q2
TLV71133285DDSET	WSON	DSE	6	250	178.0	8.4	1.7	1.7	0.95	4.0	8.0	Q2
TLV7113330DDSER	WSON	DSE	6	3000	178.0	8.4	1.7	1.7	0.95	4.0	8.0	Q2
TLV7113330DDSER	WSON	DSE	6	3000	179.0	8.4	1.8	1.8	1.0	4.0	8.0	Q2
TLV7113330DDSET	WSON	DSE	6	250	178.0	8.4	1.7	1.7	0.95	4.0	8.0	Q2
TLV7113330DDSET	WSON	DSE	6	250	179.0	8.4	1.8	1.8	1.0	4.0	8.0	Q2
TLV7113333DDSER	WSON	DSE	6	3000	179.0	8.4	1.8	1.8	1.0	4.0	8.0	Q2
TLV7113333DDSER	WSON	DSE	6	3000	178.0	8.4	1.7	1.7	0.95	4.0	8.0	Q2
TLV7113333DDSET	WSON	DSE	6	250	179.0	8.4	1.8	1.8	1.0	4.0	8.0	Q2

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLV7113333DDSET	WSON	DSE	6	250	178.0	8.4	1.7	1.7	0.95	4.0	8.0	Q2

TAPE AND REEL BOX DIMENSIONS



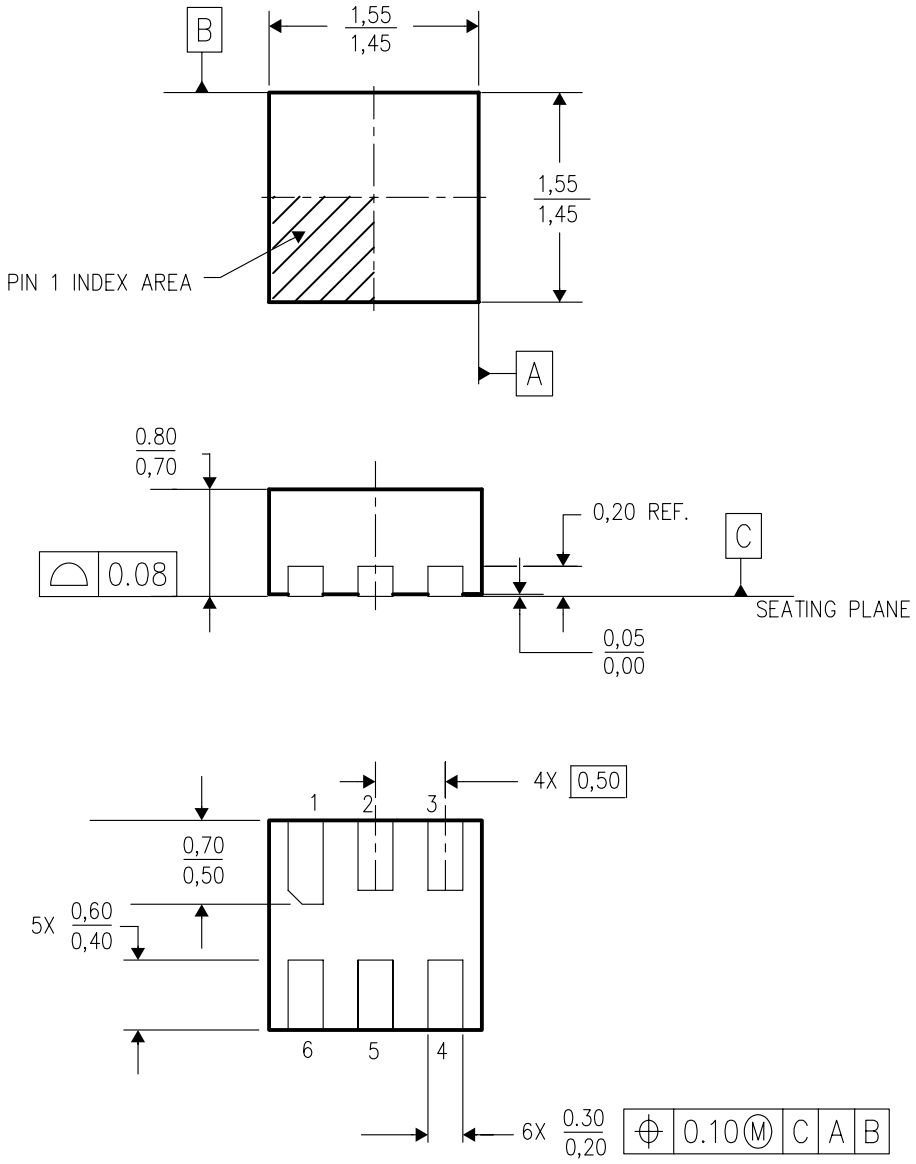
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLV7101828DSER	WSON	DSE	6	3000	203.0	203.0	35.0
TLV7101828DSET	WSON	DSE	6	250	203.0	203.0	35.0
TLV7103318DSER	WSON	DSE	6	3000	203.0	203.0	35.0
TLV7103318DSET	WSON	DSE	6	250	203.0	203.0	35.0
TLV7111225DSER	WSON	DSE	6	3000	202.0	201.0	28.0
TLV7111225DSET	WSON	DSE	6	250	202.0	201.0	28.0
TLV7111233DSER	WSON	DSE	6	3000	202.0	201.0	28.0
TLV7111233DSET	WSON	DSE	6	250	202.0	201.0	28.0
TLV7111323DDSER	WSON	DSE	6	3000	203.0	203.0	35.0
TLV7111323DDSET	WSON	DSE	6	250	203.0	203.0	35.0
TLV7111333DDSER	WSON	DSE	6	3000	203.0	203.0	35.0
TLV7111333DDSET	WSON	DSE	6	250	203.0	203.0	35.0
TLV7111518DDSER	WSON	DSE	6	3000	203.0	203.0	35.0
TLV7111518DDSER	WSON	DSE	6	3000	205.0	200.0	33.0
TLV7111518DDSET	WSON	DSE	6	250	203.0	203.0	35.0
TLV7111518DDSET	WSON	DSE	6	250	205.0	200.0	33.0

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLV7111533DDSER	WSON	DSE	6	3000	203.0	203.0	35.0
TLV7111533DDSET	WSON	DSE	6	250	203.0	203.0	35.0
TLV7111812DSER	WSON	DSE	6	3000	202.0	201.0	28.0
TLV7111812DSET	WSON	DSE	6	250	202.0	201.0	28.0
TLV7111830DSER	WSON	DSE	6	3000	202.0	201.0	28.0
TLV7111830DSET	WSON	DSE	6	250	202.0	201.0	28.0
TLV7111833DDSER	WSON	DSE	6	3000	203.0	203.0	35.0
TLV7111833DDSER	WSON	DSE	6	3000	205.0	200.0	33.0
TLV7111833DDSET	WSON	DSE	6	250	205.0	200.0	33.0
TLV7111833DDSET	WSON	DSE	6	250	203.0	203.0	35.0
TLV7111930DSER	WSON	DSE	6	3000	202.0	201.0	28.0
TLV7111930DSET	WSON	DSE	6	250	202.0	201.0	28.0
TLV71125125DSER	WSON	DSE	6	3000	202.0	201.0	28.0
TLV71125125DSET	WSON	DSE	6	250	202.0	201.0	28.0
TLV7112525DSER	WSON	DSE	6	3000	203.0	203.0	35.0
TLV7112525DSET	WSON	DSE	6	250	203.0	203.0	35.0
TLV71128512DSER	WSON	DSE	6	3000	183.0	183.0	20.0
TLV71128512DSET	WSON	DSE	6	250	183.0	183.0	20.0
TLV71128518DDSER	WSON	DSE	6	3000	203.0	203.0	35.0
TLV71128518DDSER	WSON	DSE	6	3000	205.0	200.0	33.0
TLV71128518DDSET	WSON	DSE	6	250	203.0	203.0	35.0
TLV71128518DDSET	WSON	DSE	6	250	205.0	200.0	33.0
TLV711285285DDSER	WSON	DSE	6	3000	203.0	203.0	35.0
TLV711285285DDSER	WSON	DSE	6	3000	205.0	200.0	33.0
TLV711285285DDSET	WSON	DSE	6	250	203.0	203.0	35.0
TLV711285285DDSET	WSON	DSE	6	250	205.0	200.0	33.0
TLV7113025DSER	WSON	DSE	6	3000	202.0	201.0	28.0
TLV7113025DSET	WSON	DSE	6	250	202.0	201.0	28.0
TLV7113030DDSER	WSON	DSE	6	3000	203.0	203.0	35.0
TLV7113030DDSET	WSON	DSE	6	250	203.0	203.0	35.0
TLV7113318DDSER	WSON	DSE	6	3000	205.0	200.0	33.0
TLV7113318DDSER	WSON	DSE	6	3000	203.0	203.0	35.0
TLV7113318DDSET	WSON	DSE	6	250	203.0	203.0	35.0
TLV7113318DDSET	WSON	DSE	6	250	205.0	200.0	33.0
TLV71133285DDSER	WSON	DSE	6	3000	205.0	200.0	33.0
TLV71133285DDSER	WSON	DSE	6	3000	203.0	203.0	35.0
TLV71133285DDSET	WSON	DSE	6	250	203.0	203.0	35.0
TLV71133285DDSET	WSON	DSE	6	250	205.0	200.0	33.0
TLV7113330DDSER	WSON	DSE	6	3000	205.0	200.0	33.0
TLV7113330DDSER	WSON	DSE	6	3000	203.0	203.0	35.0
TLV7113330DDSET	WSON	DSE	6	250	205.0	200.0	33.0
TLV7113330DDSET	WSON	DSE	6	250	203.0	203.0	35.0
TLV7113333DDSER	WSON	DSE	6	3000	203.0	203.0	35.0
TLV7113333DDSER	WSON	DSE	6	3000	205.0	200.0	33.0

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLV7113333DDSET	WSON	DSE	6	250	203.0	203.0	35.0
TLV7113333DDSET	WSON	DSE	6	250	205.0	200.0	33.0

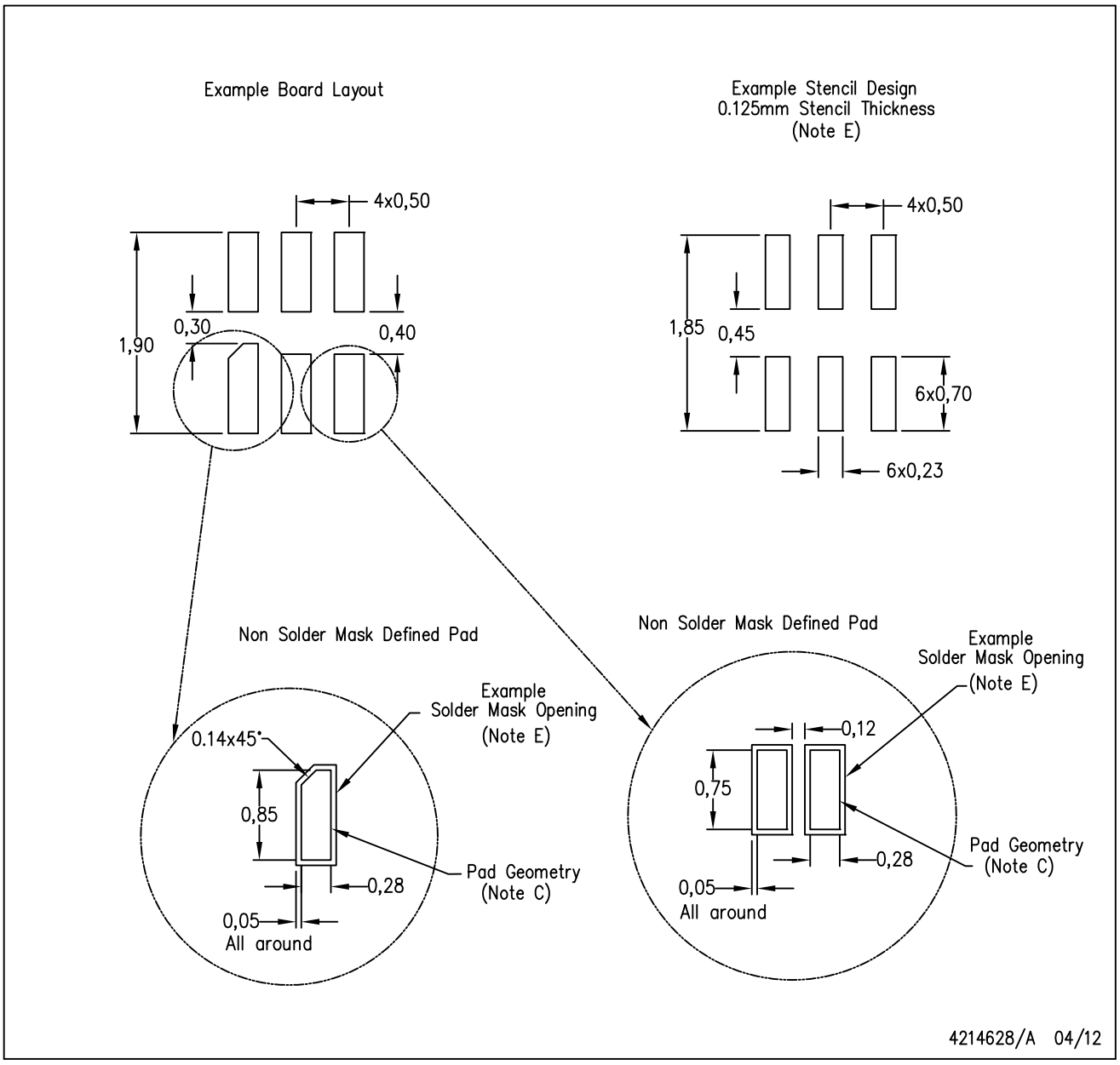
DSE (S–PDSO–N6) PLASTIC SMALL OUTLINE



4207810/A 03/06

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Small Outline No–Lead (SON) package configuration.
D. This package is lead–free.

DSE (S–PWSON–N6) PLASTIC SMALL OUTLINE NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
E. Customers should contact their board fabrication site for solder mask tolerances.

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